Future Technology Devices International Ltd.

VDIP1

Vinculum VNC1L Module

Datasheet

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1   Introduction

The VDIP1 module is an MCU to embedded USB host controller development module for the VNC1L IC device. The VDIP1 is supplied on a PCB designed to fit into a 24 pin DIP socket, and provides access to the UART, parallel FIFO, and SPI interface pins on the VNC1L device, via its AD and AC bus pins. Not only is it ideal for developing and rapid prototyping of VNC1L designs, but also an attractive quantity discount structure makes this module suitable for incorporation into low and medium volume finished product designs.

Figure 1.1- VDIP1

The Vinculum VNC1L is the first of FTDI's Vinculum family of Embedded USB host controller integrated circuit devices. Not only is it able to handle the USB Host Interface, and data transfer functions but owing to the inbuilt MCU and embedded Flash memory, Vinculum can encapsulate the USB device classes as well. When interfacing to mass storage devices such as USB Flash drives, Vinculum also transparently handles the FAT File structure communicating via UART, SPI or parallel FIFO interfaces via a simple to implement command set. Vinculum provides a new cost effective solution for providing USB Host capability into products that previously did not have the hardware resources available. The VNC1L is available in Pb-free (RoHS compliant) compact 48-Lead LQFP package.

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2   Features

The VDIP1 has the following features:

- Uses FTDI's VNC1L embedded dual USB host controller IC device

- USB single 'A' type USB socket to interface with USB peripheral devices

- Second USB interface port available via module pins if required

- Jumper selectable UART, parallel FIFO or SPI MCU interfaces

- Single 5V supply input from USB connection (no external supply necessary)

- Auxiliary 3.3 V / 200 mA power output to external logic.

- Program or update firmware via USB Flash disk or via UART/Parallel FIFO/SPI interface

- Power and traffic indicator LED's

- VNC1L firmware programming control pins PROG# and RESET# brought out onto jumper interface

- VDIP1 is a Pb-free, RoHS complaint development module.

- Schematics, and firmware files available for download from the Vinculum website

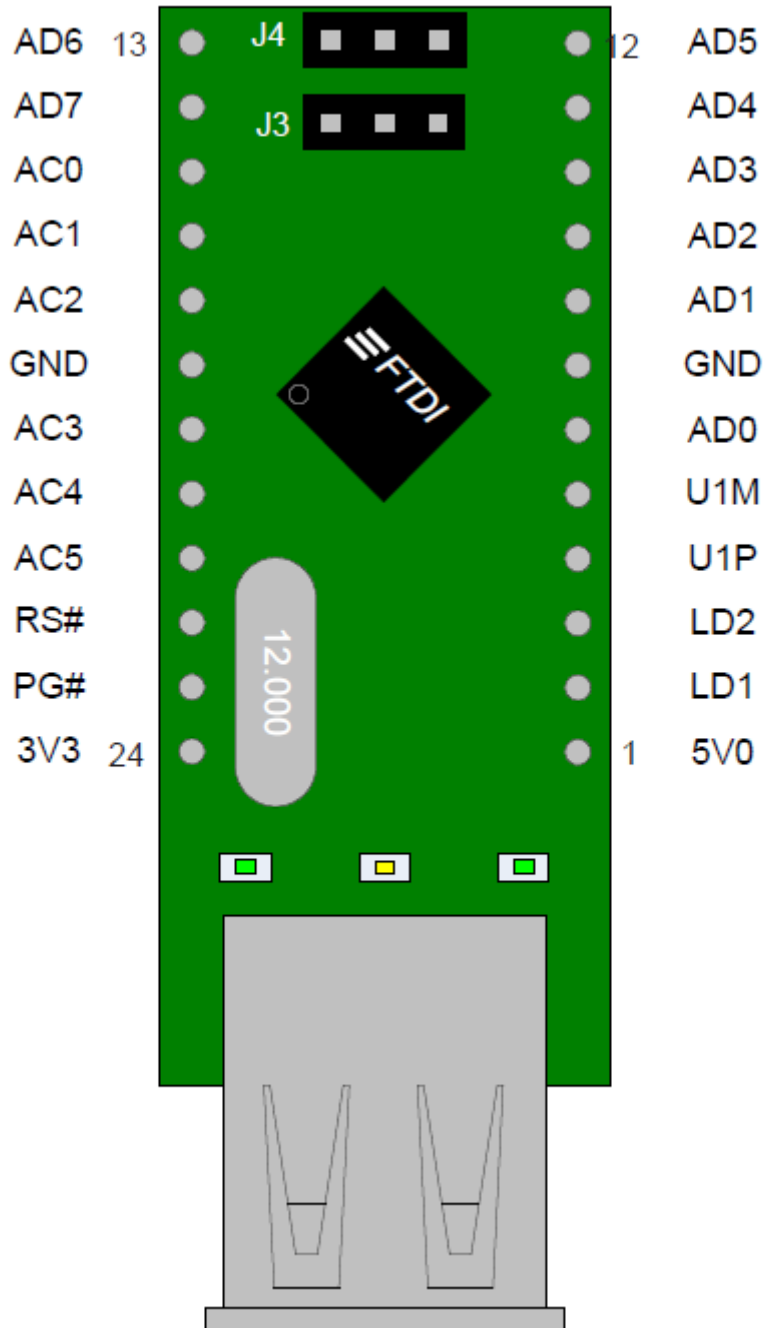# 3   Pin Out and Signal Description

3.1 Module Pin Out

Figure 3.1 - VDIP1 Module Pin Out (Top View)

3.2 Pin Signal Description

Pin No.	Name	Pin Name on PCB	Type	Description
1	5V0	5V0	PWR Input	5.0 V module supply pin. This pin provides the 5.0V output on the USB 'A' type socket, and also the 3.3V supply to VNCL2, via an on-board 3.3 V L.D.O.
2	LED1	LD1	Output	USB port 1 traffic activity indicator LED. This pin is hard wired to a green LED on board the PCB. It is also brought out onto this pin which allows for the possibility of bring- ing out an additional LED traffic indicator out of the VDIP1 board. For example, if the VDIP1 USB connector is brought out onto an instrument front panel, an activity LED could be mounted along side it.
3	LED2	LD2	Output	USB port 2 traffic activity indicator LED. This pin is hard wired to a green LED on board the PCB. It is also brought out onto this pin which allows for the possibility of bring- ing out an additional LED traffic indicator out of the VDIP1 board. For example, if the VDIP1 USB connector is brought out onto an instrument front panel, an activity LED could be mounted along side it.
4	USBD1P	U1P	I/O	USB host / slave port 1 - USB Data Signal Plus with integrated pull up / pull down resistor. Module has on board 27 Ω USB series resistor. This pin can be brought out along with pin 5 to provide a second USB port, if required
5	USBD1M	U1M	I/O	USB host / slave port 1 - USB Data Signal Minus with integrated pull up / pull down resistor. Module has on board 27 Ω USB series resistor. This pin can be brought out along with pin 4 to provide a second USB port, if required
6	ADBUS0	AD0	I/O	5V safe bidirectional data / control bus, AD bit 0
7	GND	GND	PWR	Module ground supply pin
8	ADBUS1	AD1	I/O	5V safe bidirectional data / control bus, AD bit 1
9	ADBUS2	AD2	I/O	5V safe bidirectional data / control bus, AD bit 2
10	ADBUS3	AD3	I/O	5V safe bidirectional data / control bus, AD bit 3
11	ADBUS4	AD4	I/O	5V safe bidirectional data / control bus, AD bit 4
12	ADBUS5	AD5	I/O	5V safe bidirectional data / control bus, AD bit 5
13	ADBUS6	AD6	I/O	5V safe bidirectional data / control bus, AD bit 6
14	ADBUS7	AD7	I/O	5V safe bidirectional data / control bus, AD bit 7
15	ACBUS0	AC0	I/O	5V safe bidirectional data / control bus, AC bit 0
16	ACBUS1	AC1	I/O	5V safe bidirectional data / control bus, AC bit 1
17	ACBUS2	AC2	I/O	5V safe bidirectional data / control bus, AC bit 2
18	GND	GND	PWR	Module Ground Supply Pin
19	ACBUS3	AC3	I/O	5V safe bidirectional data / control bus, AC bit 3
20	ACBUS4	AC4	I/O	5V safe bidirectional data / control bus, AC bit 4
21	ACBUS5	AC5	I/O	5V safe bidirectional data / control bus, AC bit 5
22	RESET#	RS#	Input	Can be used by an external device to reset the VNC1L. This pin can be used in combination with PROG# and the UART / parallel FIFO / SPI interface to program firmware into the Vinculum
23	PROG#	PG#	Input	This pin is used in combination with the RESET# pin and the UART / parallel FIFO / SPI interface to pro gra m fir mware into t he VNC1L.
24	3V3	3V3	PWR	3.3V output from VDIP1's on board 3.3V L.D.O.

Table 3.1 - Pin Signal Descriptions

3.3 I/O Configuration Using The Jumper Pin Header

Two three way jumper pin headers are provided to allow for simple configuration of the I/O on data and control bus pins of the VDIP1. This is done by a combination of pulling up or pulling down the VNC1L ACBUS5 (pin 46) and ACBUS6 (pin 47). The relevant portion of the VDIP1 module schematic is shown in **Figure 3.2**
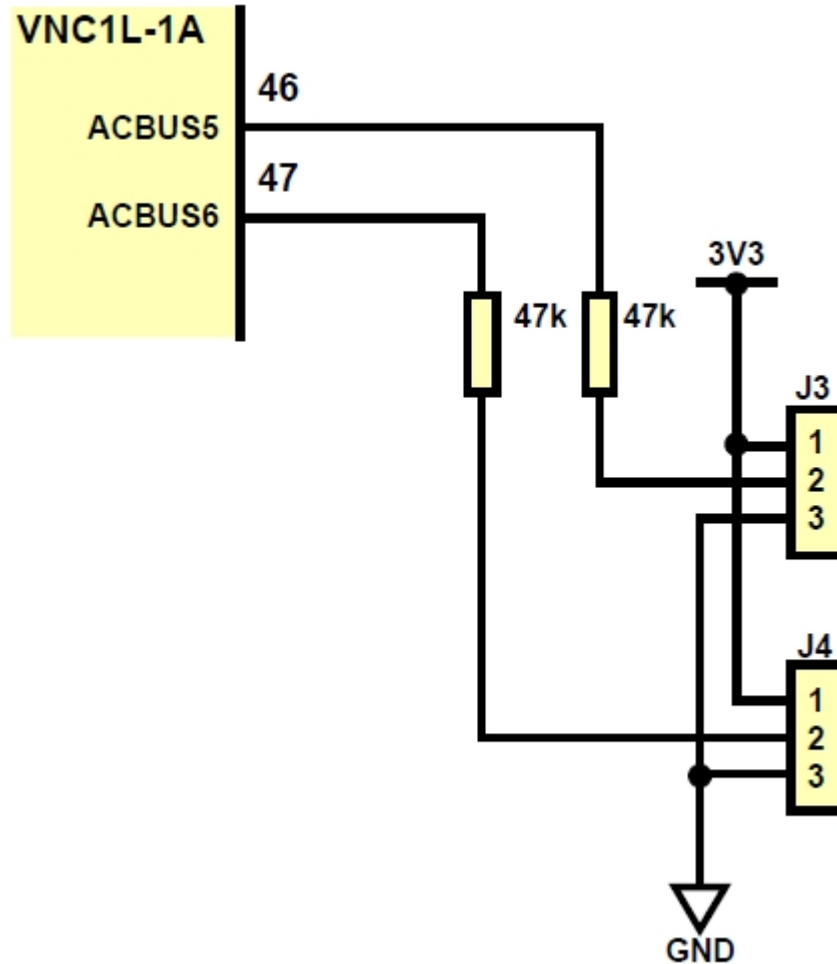
 Figure 3.2 – VDIP1 On-Board Jumper Pin Configuration.

ACBUS6 (VNC1L pin 47)	ACBUS5 (VNC1L pin 46)	I/O Mode
Pull-Up	Pull-Up	Serial UART
Pull-Up	Pull-Down	SPI
Pull-Down	Pull-Up	Parallel FIFO
Pull-Down	Pull-Down	Serial UART

 Table 3.2 - VDIP1 Port Selection Jumper Pins

3.4 Default Interface I/O Pin Configuration

The VNC1L device is pre-programmed with default settings for the I/O pins however they can be easily changed to suit a designers needs. The default interface I/O pin configuration of the VNC1L device are shown in **Table 3.3**

Pin No.	Name	Pin Name on PCB	Type	Description	Data and Control Bus Configuration Options			
					UART Interface	Parallel FIFO Interface	SPI Slave Interface	I/O Port
6	ADBUS0	AD0	I/O	5V safe bidirectional data / control bus, AD bit 0	TXD	D0	SCLK	PortAD0
8	ADBUS1	AD1	I/O	5V safe bidirectional data / control bus, AD bit 1	RXD	D1	SDI	PortAD1
9	ADBUS2	AD2	I/O	5V safe bidirectional data / control bus, AD bit 2	RTS#	D2	SDO	PortAD2
10	ADBUS3	AD3	I/O	5V safe bidirectional data / control bus, AD bit 3	CTS#	D3	CS	PortAD3
11	ADBUS4	AD4	I/O	5V safe bidirectional data / control bus, AD bit 4	DTR#	D4		PortAD4
12	ADBUS5	AD5	I/O	5V safe bidirectional data / control bus, AD bit 5	DSR#	D5		PortAD5
13	ADBUS6	AD6	I/O	5V safe bidirectional data / control bus, AD bit 6	DCD#	D6		PortAD6
14	ADBUS7	AD7	I/O	5V safe bidirectional data / control bus, AD bit 7	RI#	D7		PortAD7
15	ACBUS0	AC0	I/O	5V safe bidirectional data / control bus, AC bit 0	TXDEN#	RXF#		PortAC0
16	ACBUS1	AC1	I/O	5V safe bidirectional data / control bus, AC bit 1		TXE#		PortAC1
17	ACBUS2	AC2	I/O	5V safe bidirectional data / control bus, AC bit 2		RD#		PortAC2
19	ACBUS3	AC3	I/O	5V safe bidirectional data / control bus, AC bit 3		WR		PortAC3
20	ACBUS4	AC4	I/O	5V safe bidirectional data / control bus, AC bit 4				PortAC4

Table 3.3 - Default Interface I/O Pin Configuration

3.5 Signal Descriptions - UART Interface

The UART interface I/O pin description of the VNC1L device are shown in **Table 3.4**

Pin No.	Name	Type	Description
6	TXD	Output	Transmit asynchronous data output
8	RXD	Input	Receive asynchronous data input
9	RTS#	Output	Request To Send Control Output / Handshake signal
10	CTS#	Input	Clear To Send Control Input / Handshake signal
11	DTR#	Output	Data Terminal Ready Control Output / Handshake signal
12	DSR#	Input	Data Set Ready Control Input / Handshake signal
13	DCD#	Input	Data Carrier Detect Control Input
14	RI#	Input	Ring Indicator Contro l Input. When the RemoteakeW up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend
15	TXDEN#	Input	Enable Transmit Data for RS485 designs

Table 3.4 - Default I/O Pin Configuration – UART Interface

3.6 Signal Descriptions – Serial Peripheral Interface (SPI)

The SPI I/O pin description of the VNC1L device are shown in **Table 3.5**

Pins No	Name	Type	Description
6	SCLK	Input	SPI Clock input, 12MHz maximum.
8	SDI	Input	SPI Serial Data Input
9	SDO	Output	SPI Serial Data Output
10	CS	Input	SPI Chip Select Input

Table 3.5 - Data and Control Bus Signal Mode Options – SPI Slave Interface

3.6.1 SPI Slave Data Read Cycle

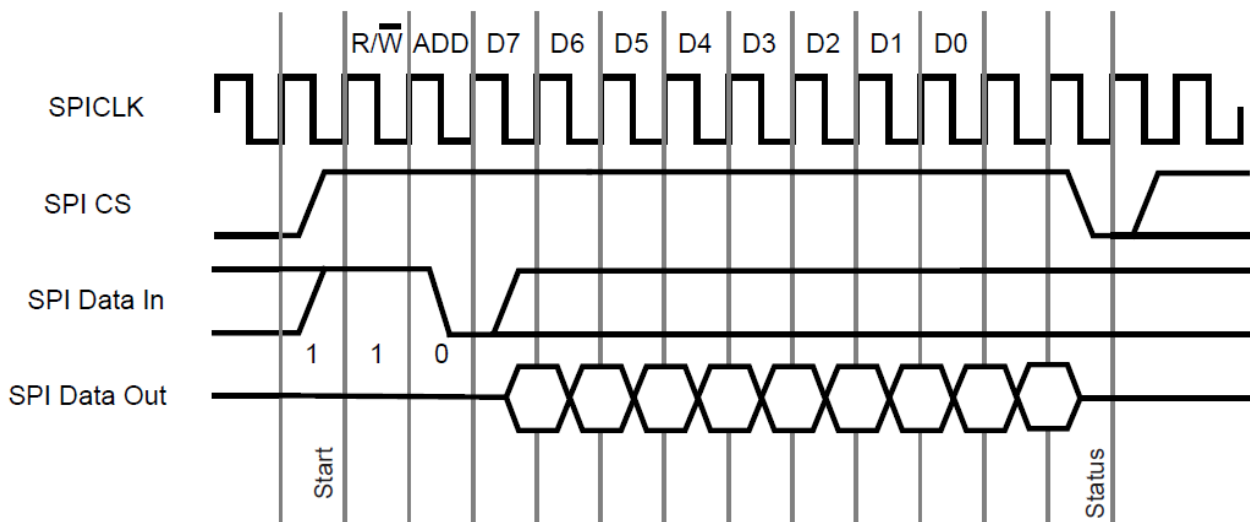When in SPI mode, the timing of a read operation is shown in Figure 3.3

Figure 3.3 – SPI Slave Data Read Cycle.

From Start - SPI CS must be held high for the entire read cycle, and must be taken low for at least one clock period after t he read is co mpleted. The first bit on SPI Data In is the R/W bit - inputting a '1' here a llows data to be read fro m the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status register ('1') is read from. During the SPI read cycle a byte of data will start being output on SPI Data Out on the next clock cycle after t he address bit, MSBAfterfirst.t he data has been clocked out of the chip, t he status of SPI Data. Out should be checked to see if the data read is new data. A '0' level here on SPI Data Out means that the data read is new data. A '1' indicates that the data read is old data, and the read cycle should be repeated to get new data. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

3.6.2 SPI Slave Data Write Cycle

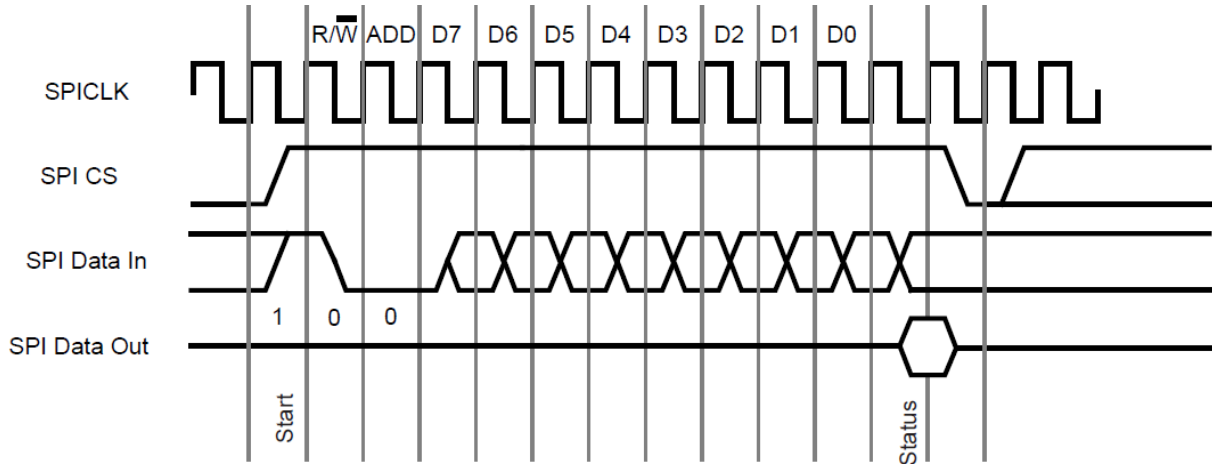When in SPI mode, the timing of a write operation is shown in

Figure 3.4 – SPI Slave Data Write Cycle.

From Start - SPI CS must be held high for the entire write cycle, and must be taken low for at least one clock period after t he write is co mpletedThe. first bit on SPI Data In is the R/W bit - inputting a '0' here a llows data to be written to the chip. The next bit is the address bit, ADD, which is used to indicate whether the data register ('0') or the status register ('1') is written to. During the SPI write cycle a byte of data can be input to SPI Data In on the next clock cycle after t he address bit, MSBAfterfirst.t he data has been clocked in to the chip, t he status of SPI Data Out should be checked to see if the data read was accepted. A '0' level on SPI Data Out means that the data write was accepted. A '1' indicates that the internal buffer is full, and the write should be repeated. Remember that CS must be held low for at least one clock period before being taken high again to continue with the next read or write cycle.

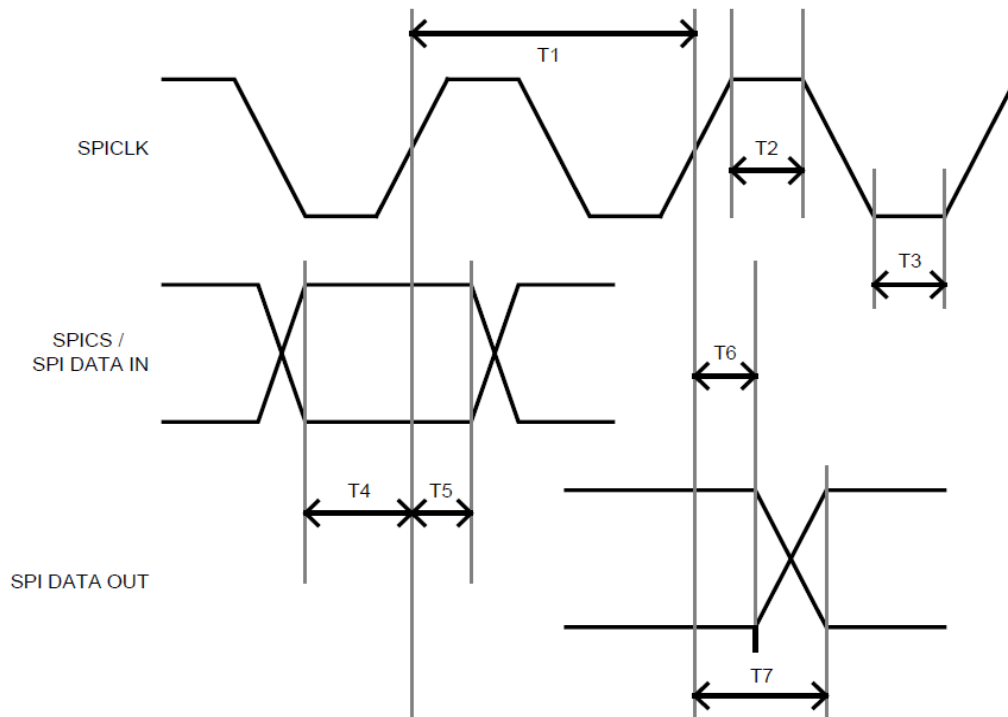### 3.6.3 SPI Slave Data Timing Diagrams

Figure 3.5 – SPI Slave Data Timing Diagrams.

Time	Description	Min	Typical	Max	Unit
T1	SPICLK Period	83	-	-	ns
T2	SPICLK High	20	-	-	ns
T3	SPICLK Low	20	-	-	ns
T4	Input Setup Time	10	-	-	ns
T5	Input Hold Time	10	-	-	ns
T6	Output Hold Time	2	-	-	ns
T7	Output Valid Time	-	-	20	ns

Table 3.6 - SPI Slave Data Timing

Time	Description
T1	RXF#
T2	TXE#
T3	-
T4	-
T5	RXF IRQEn
T6	TXE IRQEn
T7	-

Table 3.7 - SPI Slave Status Register (ADD='1')

3.7 Signal Descriptions - Parallel FIFO Interface

The Parallel FIFO interface I/O pin description of the VNC1L device is shown in **Table 3.8**

Pin No.	Name	Type	Description
6	D0	I/O	FIFO Data Bus Bit 0
8	D1	I/O	FIFO Data Bus Bit 1
9	D2	I/O	FIFO Data Bus Bit 2
10	D3	I/O	FIFO Data Bus Bit 3
11	D4	I/O	FIFO Data Bus Bit 4
12	D5	I/O	FIFO Data Bus Bit 5
13	D6	I/O	FIFO Data Bus Bit 6
14	D7	I/O	FIFO Data Bus Bit 7
15	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by stro bing RD# low, t hen high again.
16	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low.
17	RD#	INPUT	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if avail- able) fro m the recei ve FIFO buffer w hen RD# goes fro m high to low
19	WR	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low.

Table 3.8 - Default Interface I/O Pin Configuration Option – Paralle FIFO Interface

3.7.1 Timing Diagram – Parallel FIFO Read Transaction

When in parallel FIFO interface mode, the timing of a read is shown in **Figure 3.6** and **Table 3.9**
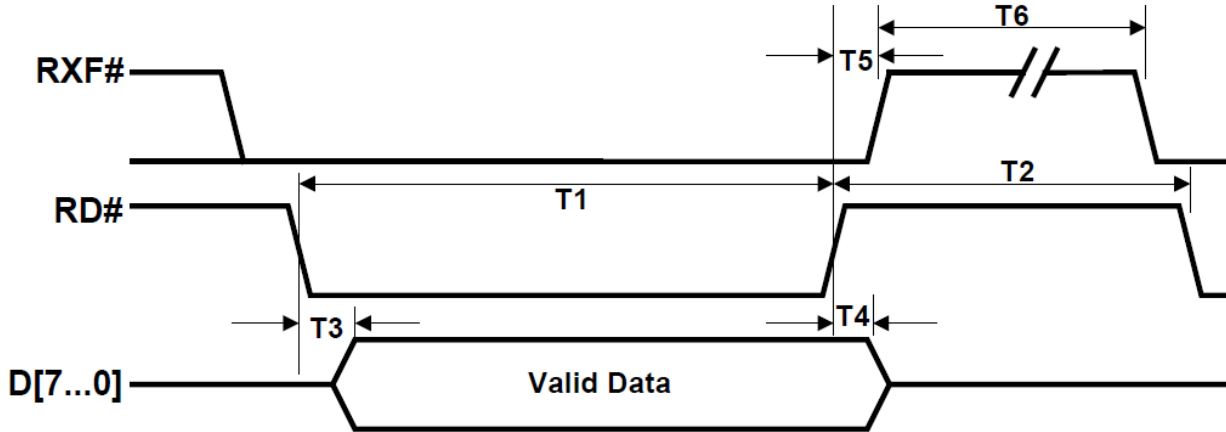

Figure 3.6 - FIFO Read Cycle.

Time	Description	Min	Max	Unit
T1	RD# Active Pulse Width	50	-	ns
T2	RD# to RD# Pre-Charge Time	50 + T6	-	ns
T3	RD# Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD#	0	-	ns
T5	RD# Inactive to RXF#	0	25	ns
T6	RXF# Inactive After RD# Cycle	80	-	ns

Table 3.9 FIFO Read Cycle Timing

* Load = 30pF

3.7.2 Timing Diagram - Parallel FIFO Write Transaction

When in parallel FIFO interface mode, the timing of a write operation is shown in **Figure 3.7** and **Table 3.10**
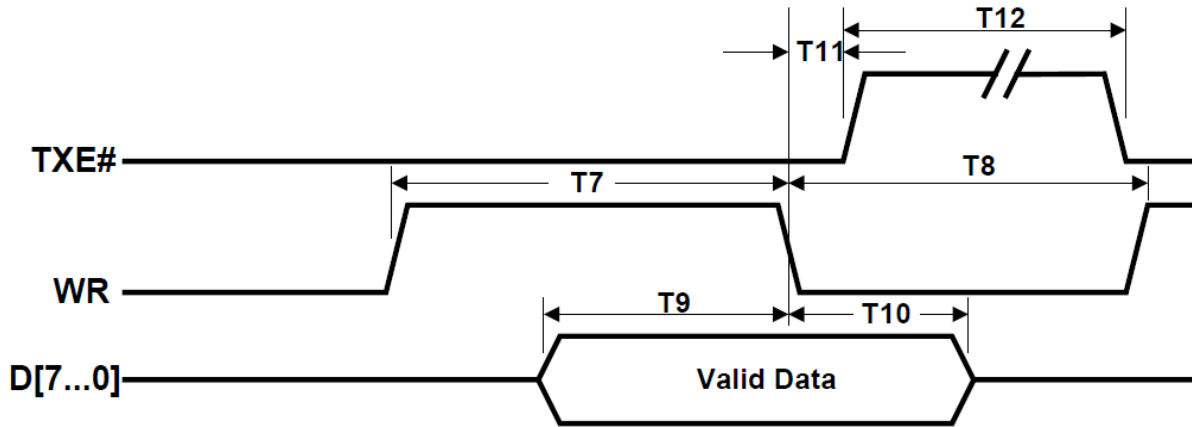

Figure 3.7 - FIFO Write Cycle.

Time	Description	Min	Max	Unit
T7	WR Active Pulse Width	50	-	ns
T8	WR to WR Pre-Charge Time	50	-	ns
T9	WR Active to Valid Data	20	-	ns
T10	Data Hold Time from WR	0	-	ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE# Inactive After WR Cycle	80	-	ns

Table 3.10 - FIFO Write Cycle Timing

4 Firmware

4.1.1 Firmware Support

There are currently 6 standard firmware versions available for VDIP1 module which can be downloaded from the [FTDI website](#).

- VDAP Firmware: USB Host for single Flash Disk and General Purpose USB peripherals. Selectable UART, FIFO or SPI interface command monitor.

- VDPS Firmware: USB Host for single Flash Disk and General Purpose USB peripherals. USB Slave port connection for connecting to host PC. Selectable UART, FIFO or SPI interface command monitor.

- VDFC Firmware: USB Host for two Flash Disks, Selectable UART, FIFO or SPI interface command monitor.

- VCDC Firmware: USB Host for automatic connection to USB Communications Class Devices. UART interface command monitor.

- VDIF Firmware: USB Host for single Flash Disk and General Purpose USB peripherals. Selectable UART, FIFO, SPI or USB interface command monitor.

4.1.2 Firmware Upgrades

The VDIP1 module is supplied pre-loaded with the VDAP firmware.

There are two methods of upgrading the firmware on the VDIP1. These methods are described in a Vinculum Firmware manual please refer to:-

http://www.vinculum.com/documents/fwspecs/UM_VinculumFirmware_V205.pdf
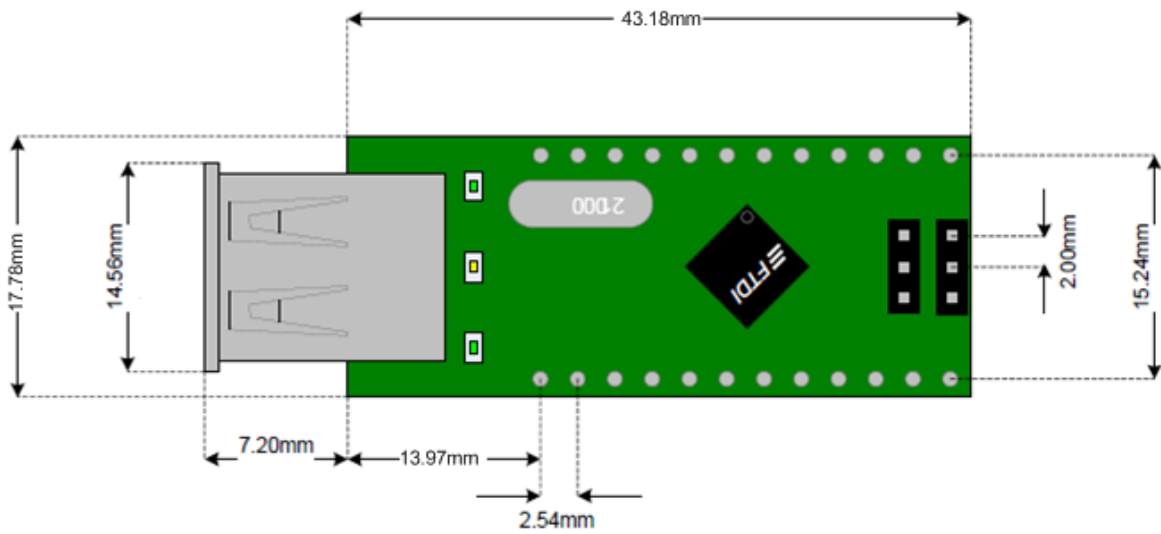
5   Mechanical Dimensions

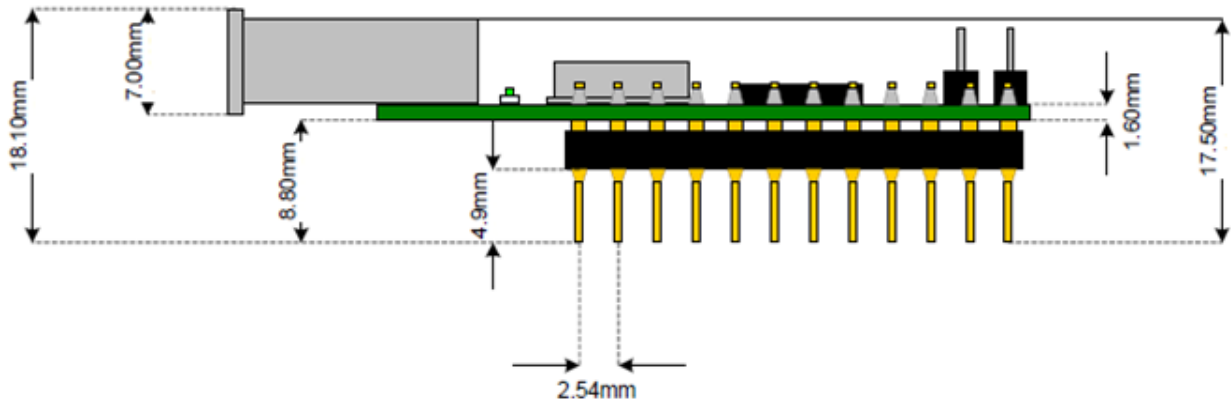**Figure 5.1 VDIP1 Dimensions (Top View)**

Figure 5.2 VDIP1 Dimensions (Side View)

6   External circuit Configuration

6.1 Adding a second USB Port

The external circuit configuration for adding second USB host port, with the USB activity LED, is shown below in Figure 6.1
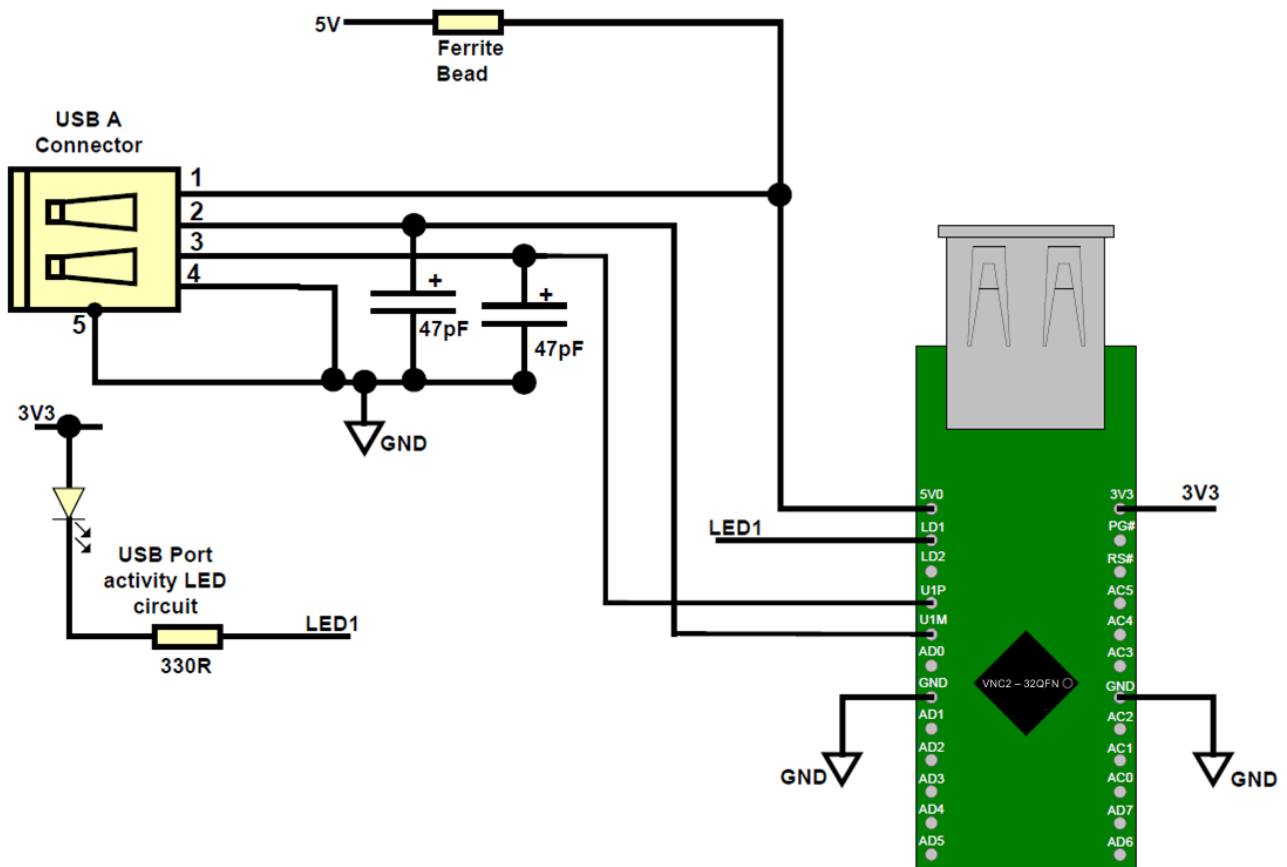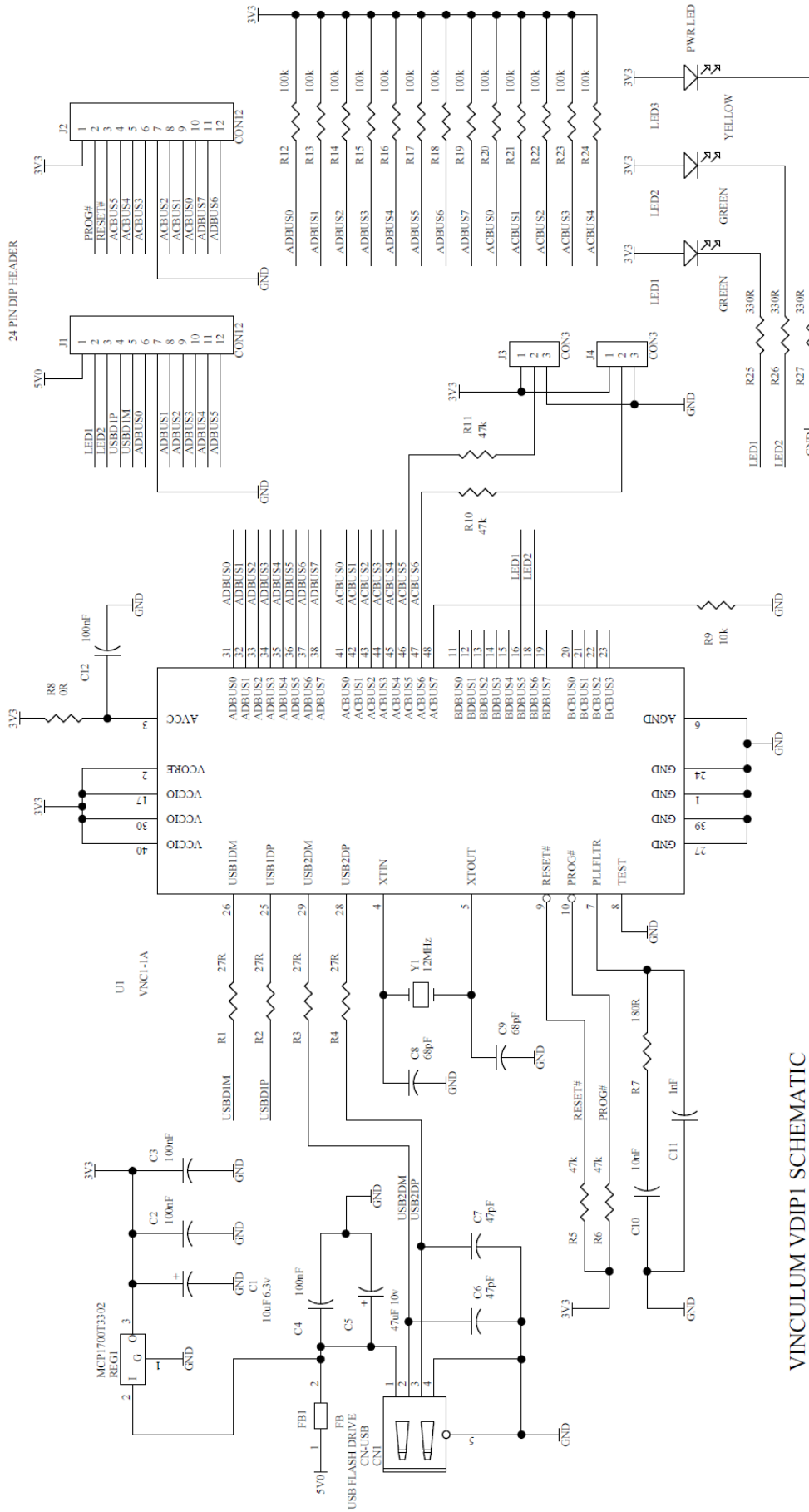

Figure 6.1 Additional USB Port Configuration

7   Schematic Diagram

Figure 7.1 - Schematic Diagram

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

http://www.vinculum.com/documents/fwspecs/UM_VinculumFirmware_V205.pdf

Appendix B – List of Figures and Tables

List of Figures

List of Tables

Appendix C – Revision History

Version 0.91	Initial Datasheet Created	August 2006
Version 0.92	Datasheet Updated	March 2007
Version 1.0	Datasheet Updated (Reformatted)	10th December 2009
	Datasheet Updated (Mechanical Drawings)	
	Added Appendix A	
	Added schematic	
Version 1.01	Corrected Table 3.1 (pin 18, 19, 20, 21)	31st May 2010
Version 1.02	Corrected figure 7.1 (C8 & C9 changed to 68pF)	14th June 2011