Design of a 3-bit Flash ADC circuit using a Double-Tail Dynamic Comparator

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Abstract—In this paper, a 3-bit Flash type Analog to Digital Circuit is implemented. The circuit is used in comparing an input analog voltage with a set of reference voltages, thereby converting the analog input signal into it's digital counterparts. The Flash ADC is constructed using a set of comparators arranged in a particular fashion, along with a voltage divider circuit and a coding circuit that produces the binary digits. First, the double-tail dynamic comparator is studied. It is a faster and more efficient comparator design, which can be used to produce digital signals in real-time. The coding circuit implemented here, is an 8:3 Priority Encoder, which is used to produce the 3-bit binary output. The analog block comprises of seven comparator circuits, and the digital block comprises of the 8:3 Priority Encoder, realized using Verilog Hardware Description Language.

I. CIRCUIT DETAILS

Analog to Digital Converters (ADCs) are circuits that are used in converting analog signals into an n-bit binary coded digital signals. One such ADC, is the Flash or Parallel type ADC which is an open-loop ADC that is used in radar systems, wideband radio receivers and optical communication systems. The Flash type ADC consists of three important circuits - Comparators, voltage dividers and coding circuit. The comparator is used to compare the input analog voltage with a certain voltage that is obtained from the reference voltage. An n-bit Flash type ADC is designed using $2^n - 1$ comparators, 2^n resistors and an n bit coding circuit. Thus, a 3-bit multiplier is required to have 7 comparators, 8 resistors and a 3-bit coding circuit. An important parameter that is required to be defined for all ADC circuits, is the resolution, which denotes the minimum change for conversion. For an n-bit Flash ADC, the resolution, is given as $V_{ref}/2^n$. For a 3-bit Flash ADC, the resolution is given as $V_{ref}/8$. First, a Double-Tail Dynamic Comparator is implemented, to see how it fits for using it in Flash ADC. It is one of the comparators that comes with lesser area, delay and power comsumption. The output of the comparators is sent to the coding circuit. Since we have 8 inputs that needs to be encoded to 3-bit outputs, an 8:3 priority encoder is implemented, and the output obtained is a 3-bit binary representation of the analog signal. The analog block comprises of the comparators built using lm741 Operational Amplifiers, which along with the voltage dividers, aid to decrease simulation time and the 8:3 priority encoder constitutes the digital block, thus making the design a mixed-signal one. Figure 1 highlights the mixed-signal Flash ADC circuit, and Figure 2 shows the output waveform of the same.
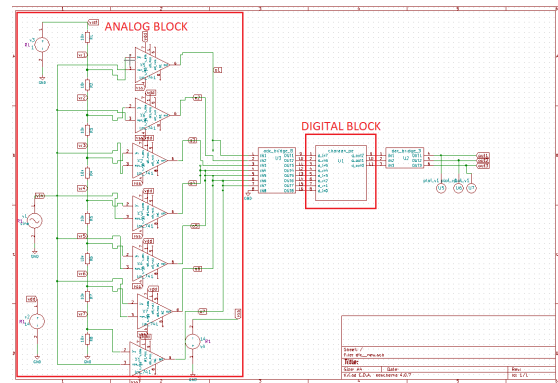
II. IMPLEMENTED CIRCUIT

Figure 1. 3-bit Flash ADC circuit
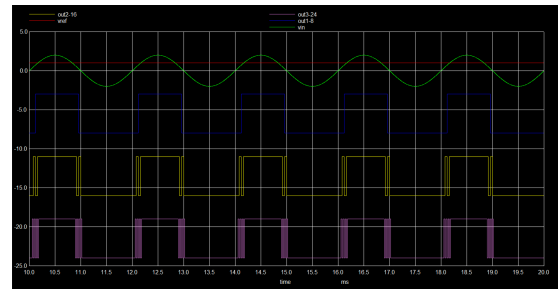
III. IMPLEMENTED WAVEFORM

Figure 2. Resultant Waveform containing the input and output

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