Design of an Area Efficient Braun Multiplier using High Speed Parallel Prefix Adder in Cadence

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***Abstract*— Matrix multiplication is one of the most fundamental part of digital signal processing systems and is also used as a recursive routine in many signal processing and computational problems. The circuit complexity mainly depends on the multiplication count required for developing the system. Parallel array multiplier is the solution for achieving high execution speed demands. A conventional Braun multiplier includes an array of 16 AND gates, 9 Full Adders, and a ripple carry adder (RCA) in the final stage. A new design of Braun replaces RCA with Kogge-Stone Adder (KSA) for performing faster multiplication. Two designs of KSA are proposed using 14T XOR and 12T XOR gates. A conventional Braun multiplier and Braun multiplier with KSA are designed in cadence Virtuoso tool for 180nm technology with 1.8V source. It is observed that the area reduces by 258 transistors and delay is decreased by 4.65 ns**.

Keywords—Digital Signal Processors (DSP), Ripple carry adder (RCA), Kogge-Stone adder (KSA).

I. INTRODUCTION

The advances made in VLSI technology both in terms of speed and size, have made possible the hardware implementation of parallel multipliers. The growth of technology further ensures enhanced performance characteristics and widespread use in DSP systems. It performs such operations as accumulating the sum of multiple products much faster than an ordinary microprocessor. The DSP architecture is so designed that it performs parallel operation and thus reduces the computational complexity and enhances the speed for repetitive signal processing required for such applications.[1]. These features are designed in the programmable DSP to higher speed and throughput. For a given application, there is a large number of programmable DSPs to choose from, based on such factors as speed, throughput, arithmetic capability, precision, size, cost and power consumption [2]. The advent of single-chip multipliers and their integration into microprocessor architecture is the most important reasons for the availability of commercial VLSI chips capable of DSP functions. These multipliers are called parallel or array multipliers [3]. Generation of product of two binary numbers requires a single processor cycle. Earlier, either a software based shift and add algorithm or one using micro-coded controllers, which implement same algorithm in hardware were used as popular multiplication schemes. Both these options require several processor cycles to complete multiplication. Kogge-Stone Adder (KSA) is a design of parallel prefix adders using XOR and AND gates [5],[6]. Conventional multipliers designed with 22T XOR or 16T XOR gates. 3T XOR, 6T XOR and 10T XOR models are already available but these have the problem of threshold loss [7],[8].12T XOR gate is preferred for current design of KSA, that gives full swing output[9]. In this work, Braun Multiplier with Kogge-Stone Adder is used for decreasing the area and delay.

II. CONVENTIONAL BRAUN MULTIPLIER

Braun multiplier is built conventionally in CMOS technology. All the basic building blocks that form the multiplier use CMOS technology. It has 16 AND gates and 12 FULL ADDERS FA1 to FA12 .

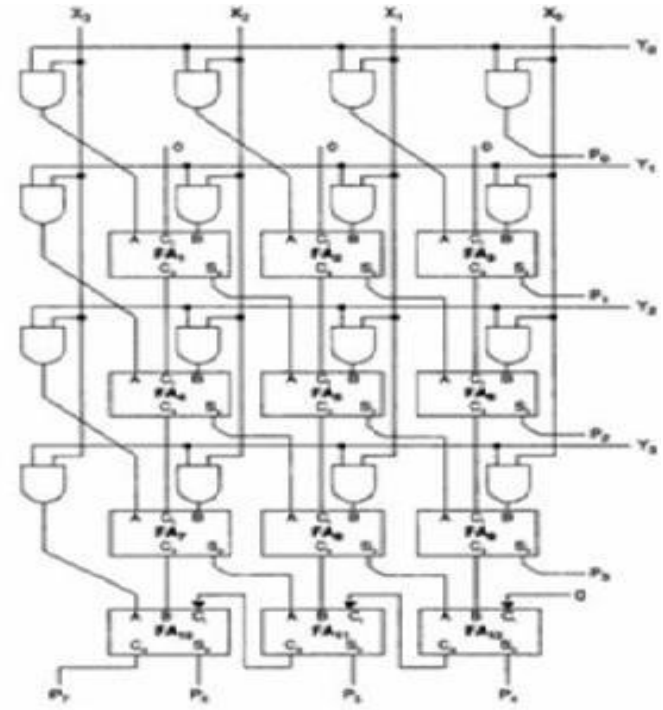

Fig. 1. Circuit diagram of 4×4 Braun multiplier

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Consider the multiplication of two unsigned numbers A and B. Let number A be represented using 'm' bits (Am-1Am-2……A0) in(1) and number B using 'n' bits (Bn-1Bn-2…..B0) in (2). The multiplicand A, the multiplier B, and the product P are given by (3)

$$A=\Sigma A_i 2^j \quad (1)$$

$$B=\Sigma B_i 2^j \quad (2)$$

$$P=\Sigma[\Sigma A_i B_j 2^{i+j}] \quad (3)$$

and can have maximum of (m+n) bits.

III. SIMULATION RESULTS OF CONVENTIONAL 4-BIT BRAUN MULTIPLIER

The schematic shown in the Fig. 2 is Braun multiplier with 4×4 input and 8 output pins. Fig.3 is the test bench for Braun multiplier made using CMOS technology. For all the inputs (a_0-a_3 , b_0-b_3), V_{pulse} of 1.8V are given. And outputs are connected P_o to P_7 pins. The output of conventional Braun multiplier depicted in Fig. 4. The below schematic has total 696 transistors. It is found that conventional Braun multiplier has an overall delay of 5.117nsec.

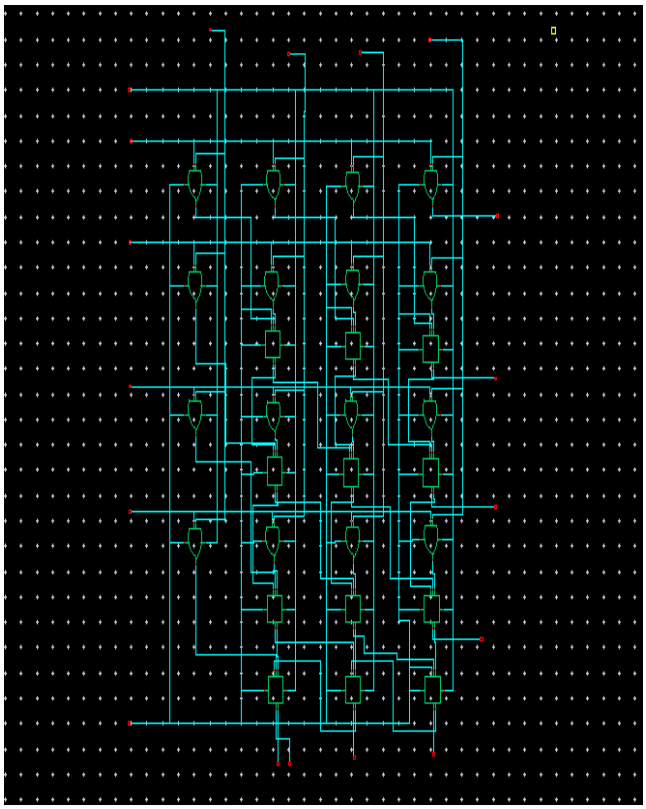

Fig. 2. Schematic of Braun multiplier

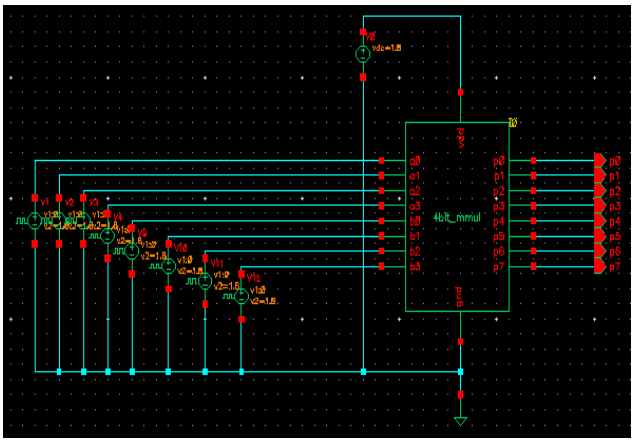

Fig. 3.Testbench of conventional braun multiplier

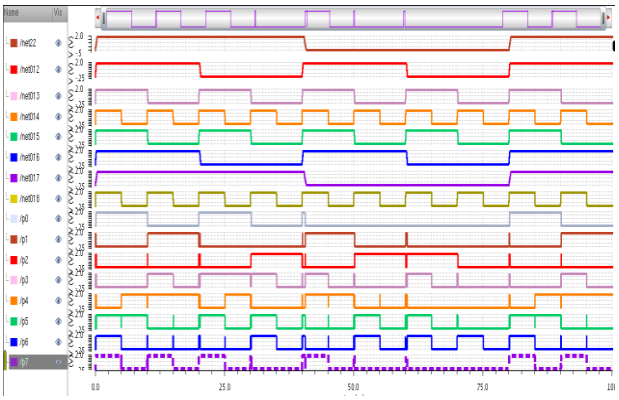

Fig. 4. Output waveforms of conventional Braun multiplier

The Table I. shows the list of inputs that are given to the test bench. The inputs are given in the form of pulse with a given pulse width, ON time and OFF time.

TABLE I. INPUTS FOR CONVENTIONAL BRAUN MULTIPLIER

Inputs	***Pulse Width(µs)***	***On Time(µs)***	***Off time(µs)***
A0	100	50	50
A1	50	25	25
A3	25	12.5	12.5
A4	12.5	6.25	6.25
B0	80	40	40
B1	40	20	20
B2	20	10	10
B3	10	5	5

IV. KOGGE-STONE ADDER

Kogge-Stone Adder is a parallel prefix adder. There are 3 stages for computing the sum bits. The computation of carry is as fast as it takes O(log n) time to generate carry. Braun

multiplier is designed with Kogge-Stone adder for reducing area and increasing its speed compared to conventional Braun multiplier which is used in most of the modern DSPs. In [6], 4-bit Braun Multiplier with KSA is implemented on FPGA using verilog HDL in which delay is reduced. The delay of whole multiplier depends mostly on the delay of Full adders array in the last stage, where its functionality is similar to RCA. The Delay produced from the RCA can be reduced by using one of the Parallel Prefix Adders "KOGGE STONE ADDER"[4].

A. Illustration of KSA using an example of 3 bit

A=011 and B = 100 are inputs

a) I Step: Pre processing

Computation of generate and propagate signals

Pi = Ai **XOR** Bi and Gi = Ai **AND Bi**

P3 = 0 XOR 1=1;

P2 = 1 XOR 0 = 1;

P1 = 1 XOR 0 = 1;

G3 = 0 AND 1=0;

G2 = 1 AND 0 =0;

G1 = 1 AND 0 = 0;

b) II Step: Carry look ahead network

Computation of carries corresponding to each bit

Pi:j= Pi:k+1 **AND** Pk:j and Gi:j = Gi:k+1 **OR** (Pi:k+1 **AND** Gk:j)

P3:2 = P3 AND P2; 1 AND 1 = 1;

G3:2 = G3 OR (P3 AND G2); 0 OR (1 AND 0) = 0;

P2:1 = P2 AND P1; 1 AND 1 = 1;

G2:1 = G2 OR (P2 AND G1); 0 OR (1 AND 0) = 0;

P3:1 = P3:2 AND P1; 1 AND 1= 1;

G3:1 = G3:2 OR (P3:2 AND G1); 0 OR (1 AND 0) = 0;

c) III Step: Post processing

Computation of sum bits

Si = Pi **XOR** Ci-1

S1 = P1XOR 0; 1 XOR 0 = 1;

S2 = P2 XOR G1; 1 XOR 0 = 1;

S3 = P3 XOR G2; 1 XOR 0 = 0;

Cout = G3:1; 0;

Sum Bits :Cout S3 S2 S1 : 0111;

B. Kogge-Stone Adder with 14T XOR gates

The circuit shown in the Fig. 5 is a 3-input Kogge-Stone adder made using CMOS technology. It has a total of 102 transistors, consisting of 6 XOR gates(6* 14) and 3 AND gates(3*6). The output of above example is depicted in Fig. 6.

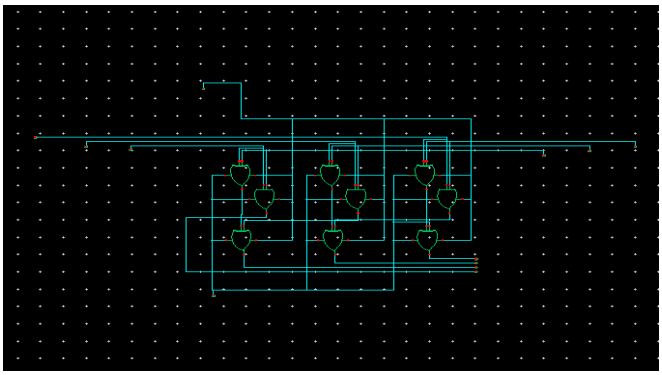

Fig. 5. Schematic of KSA with 14T XOR gates

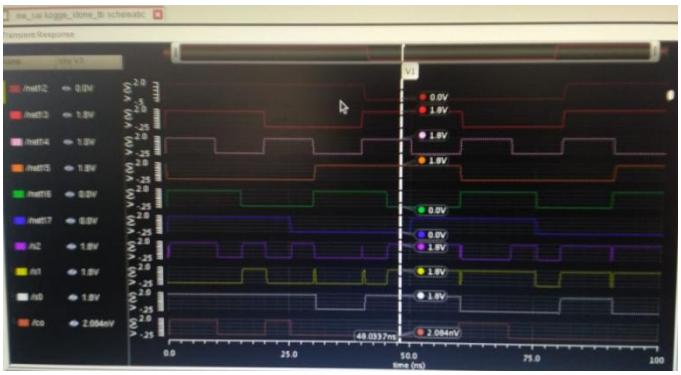

Fig. 6. Output waveform of KSA with14T XOR

C. Kogge-Stone Adder with 12T XOR gates

Fig. 7 is 12T XOR gate design and output results are presented in Fig. 8. The output shown in the Fig. 9 is 3-input Kogge-Stone adder made using 12T XOR gates[6]. It requires a total of 90 transistors, consisting of 6 XOR gates (6* 12) and 3 AND gates(3*6).

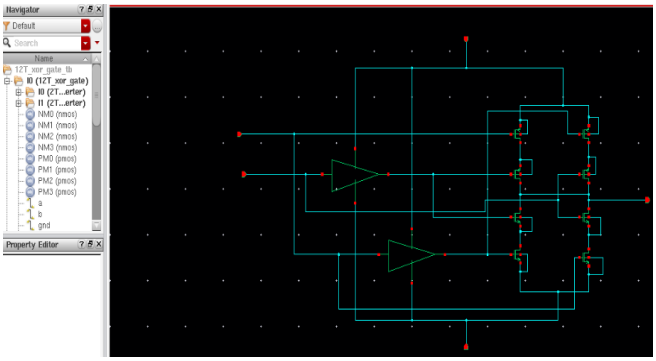

Fig. 7. Schematic of 12T XOR gate

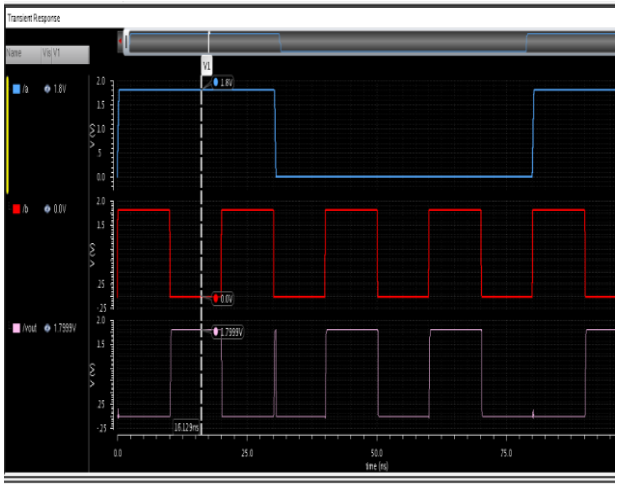

Fig. 8. Output of 12T XOR gate

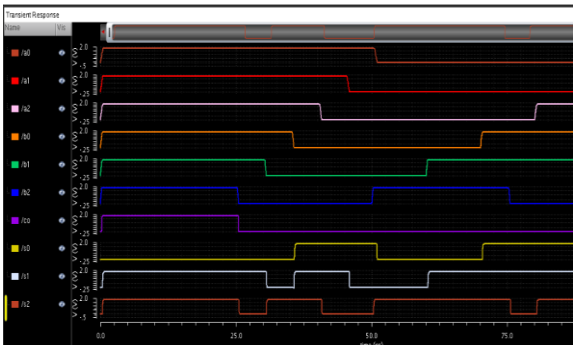

Fig. 9. Output waveform of KSA with 12T XOR

D. Comparison of results of KSA

For KSA with14T XOR design delay, power requirement and transistor count is less compared to 22T XOR KSA design. From Table II it is observed that KSA with 12T XOR design has less power and area efficient model.

TABLE II. COMPARISON RESULTS OF KSA

Kogge-Stone adder	***Delay in (ns)***	***Power in (µW)***	***Number of transistors***
22T -XOR	7.737	128	150
14T-XOR	7.47	68	102
12 T-XOR	25..24	29.9	90

V. SIMULATION RESULTS OF BRAUN MULTIFLIER WITH KOGGE-STONE ADDER

The proposed multiplier's block diagram uses a 3 bit KSA in 4th stage of Braun multiplier. This proposed multiplier is implemented using cadence 180nm technology. To design 4 bit (n bit)Braun, it needs 3bit (n-1 bit) KSA. KSA is designed with 14T XOR and 12T XOR gates. The circuit shown in the Fig. 10 is modified Braun multiplier with 4×4 input and 8 output pins. Out of 8 outputs pins, P_4-P_7 pins cause more delay in the output. Because delay is mainly due to these bits, this stage is replaced with KSA. Not only P_4-P_7 pins stage but also other stages can be designed using KSA. But the area increases and glitches create problem for multiple stages.

The circuit shown in the Fig. 11 is testbench for proposed Braun multiplier made using CMOS technology. The output of Braun multiplier with Kogge-Stone adder is represented in Fig. 12. It is observed that the delay is reduced to 188.4psec for the Braun multiplier with KSA of 14T XOR design from Table III. Braun multiplier with 12T XOR gates based KSA has low power and less area among the designs.

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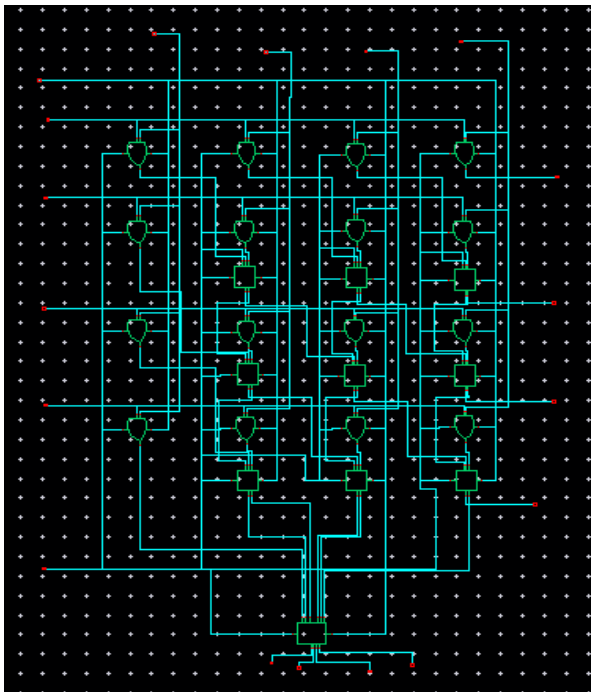

Fig. 10 Schematic of proposed Braun multiplier

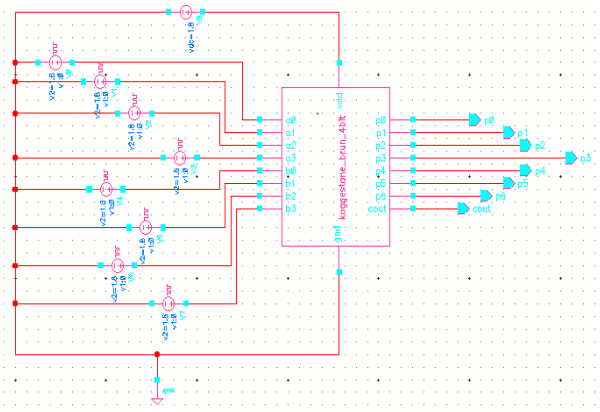

Fig. 11. Testbench of proposed Braun multiplier

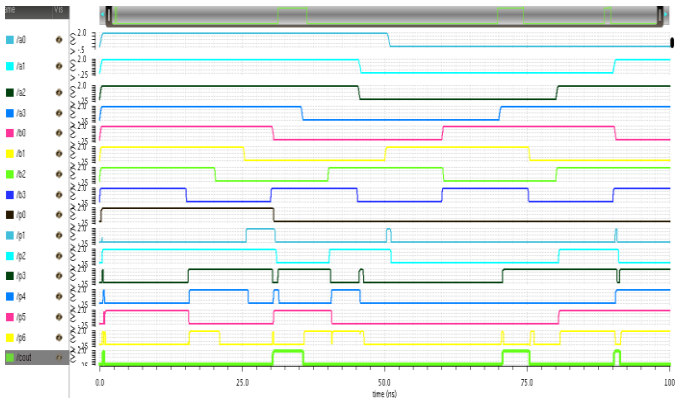

Fig. 12. Output of proposed Braun multiplier with KSA of 12T XOR

TABLE III. COMPARISON OF CONVENTIONAL AND PROPOSED DESIGNS OF BRAUN MULTIPLIER

4 bit Braun Mutiplier	***Delay(ps)***	***Power in (µW)***	***Number of transistors***
Conventional design	5117	816.8	696
Proposed design with KSA of 14T XOR	188.4	552.4	450
Proposed design with KSA of 12T XOR	467.2	202.7	438

VI. CONCLUSION

A conventional Braun multiplier and Braun multiplier with KSA is developed and compared in terms of area, speed and power. Conventional Braun multiplier logic is designed with Full adder comprising of 50 transistors and XOR logic having 22 transistors built in CMOS technology. It is observed that area, power and delay are very high. This is reduced by designing Braun multiplier logic with Full adder logic consisting of 28 transistors and XOR logic having of 14 transistor built with KSA. The area is reduced by 246 transistors and delay is decreased by 4.9286 ns. Braun multiplier with of 12T XOR has a total of 450 transistors, in which transistor count is reduced by 258 and delay is also decreased by 4.650ns compared to conventional Braun multiplier. Power consumption also very less for final design.

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