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A Novel Approach to Design Braun Array Multiplier Using Parallel Prefix Adders for Parallel Processing Architectures

- A VLSI Based Approach

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Abstract. Multipliers play a important role in current signal processing chips like DSP and general purpose processors and applications. In such high performance systems addition and multiplication operations are fundamental and most used arithmetic operations. Some case study shows that more than 70% of DSP algorithms and in microprocessor operations perform addition and multiplication. Hence these operations dominate the execution time. To meet the processing speed demand, the design of multipliers and adders plays a vital role. Low power consumption has consumption has became a major issue in design of multiplier. To reduce the power consumption, the components used in the design must be drastically reduced and in parallel it should not degrade the other performance metric. In this paper we are proposing a new architecture to design multiplier using parallel prefix adders. The Parallel Prefix Adder (PPA) have fast carry generation network and hence they are the fastest types of adder that had been created and developed. Most common types of parallel prefix adder are Brent Kung and Kogge Stone adders. The performances of these two adders in terms of worst case delay and transistor count and power consumption studied and an analysis of the same is presented. Utilizing the same to design and implement the multiplier using PPA is performed in this paper.

Keywords: Array multiplier · Braun multiplier · Parallel prefix adder
High speed adders · Parallel processing · Kogge Stone Adder (KSA)
Brunt Kung Adder (BKA) · Cadence design suite · GPDK 180 nm technology
CMOS design · GDI design

1 Introduction

A multiplierais one of the key hardware blocksain most digital signal processing (DSP) systems. Typical DSP applications, where aamultiplier plays an important role in digital filtering, digital communications and spectral analysis. In low power VLSI applications, it is desirable that theamultiplier should consume less power and less area

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in the design while achieving higher execution speed, combination of all these in a single multiplier is rarely found in several designs and hence a novel approach is proposed in this paper to meet the computational needs. The system's performanceais usually determined by the performance of the multiplier because the multiplier used in the design generally contributes significant amount of delay and consumes most of the area in the design. Statics shows that more than 70% instructions in microprocessor and most of DSP algorithms perform addition and multiplication. Power dissipation becomes one of the primary design constraints. Reducing the delay of a multiplier is an essential part of satisfying the overall design. Multiplication is very expensive and slows the overall operation. The performance of many computational problems is often dominated by the speed at which a multiplication operation can be executed. In order to achieve high execution speed and to meet performance demands in DSP applications, parallel array multipliers are widely used. One such widely used parallel array multiplier is the Braun Array Multiplier. The adderaunit is very important for designing any multiplier. Multiplication can be done serially or parallel. Theoretically multiplication can be done by repetitive addition.

In this paper we are proposing a new architecture and a novel approach to design braun multiplier using parallel prefix adder. The Parallel Prefix Adder (PPA) is one of the fastest types of adder that had been created and developed to achive a greater speed in the calculation of intermediate carries, carry and sum for the applied inputs. The two common types of parallel prefix adder are Brent Kung and Kogge Stone adder which will be used in this paper to increase the performance of the multiplier with the proposed architecture of the multiplier.

2 Literature Survey

The following are some of the references that we have gone thought for the design and analysis of various parallel prefix adders and multiplier design. The [8] is one of our paper which describes the modeling of parallel prefix adders used in this paper. In [1, 2] the authors have designed and simulated various adders like RCA, CSA, CLA and KSA using Cadence design suite at GPDK 45 nm technology and front end verification is performed on Xilinx ISE tool, these work is carried out for precision of 8-bit addition and have coated a comparative statement. In [2] the FPGA implementation of 8bit adders like RCA, CSA, CLA, and KSA is performed using Braun Multiplier. In [3] the detail investigation of the performances of different multipliers in terms of computational delay and design areas are studied. In [4] the authors have studied digital principles and designs. In [5] the authors have design and made a comparative analysis of various 8-bit adders for embedded application. In [8] we have analyzed the working and behaviors of various adders that could be used for the design of multipliers. From the analysis coated by us in [8] helps to select a adder in this paper.

3 Design of Array Multiplier

In this paper we are proposing a new architecture and a novel approach to design and implement Braun array multiplier using parallel prefix adders and the modeling of the same is performed. Several design styles were referred and few of them are used in the design, In this paper we have considered the braun multiplier with precession of 4-bit and 8-bit for design and implementation. It includes the proposed methodology of Braun's multiplier and various parallel prefix adders like Kogge Stone Adder, Brent kung Adder.

To design high performance Braun multiplier, the all stages of multiplier consisting of full adder array structure and last stage is also a set of full adder which seems like with ripple carry adder structure, most of the researchers and designers concentrate on the modification of the last stage of the multiplier structure and try to replaced with other conventional adder or some Parallel Prefix Adders like Kogge Stone Adder, Brent Kung Adder. Figure 2 shows the conventional Braun multiplier with array of full adders and the highlighted group of full adders form a ripple carry structure, this frames a worst case delay for the multiplier with theadelay incorporated from the upper full adder stages and as the precession of multiplier increases the delay increases proportionally, various other methods are framed to reduce this delay which involves the replacement of the last stage of ripple carry structure with carry look ahead adder or carry save adder or carry skip adders, or high speed adders, with those variations also the performance is having the limit, as the last stage computation is valid only when all the inputs are computed by stages above it, hence the proposed structure of Braun multiplier is shown in Fig. 3, here we are not only replacing the last stage of ripple carry structure with high speed parallel prefix adder but we are increasing the speed of the computation of stages above the last stage by observing the ripple stages and grouping those set of full adders into similar behavior of a ripple like structure and replacing those structures with the high speed adders as shown in the proposed architecture for the multiplier using parallel prefix adder, from the structure of the Braun array multiplier we can see the ripple structure excluding last stage which is indicated in Fig. 3 with dotted circles, these are now forming a ripple carry structure and limiting the performance of the multiplier, here in this paper we are replacing this indicated circle with any of high speed adder hence the new architecture and a novel approach to design the Braun multiplier with parallel prefix adder, the processing of the information from individual block to stages and then to several intermediate level give the new techniques to design and test its performance.

Figure 1 shows the general blockadiagram of Multiplier with internal component as adder, the adders of various sizes have been developed and these adders are used in different sized multipliers. To reduce the dynamic power dissipation and to increase the execution speed of multiplier. To build 4×4 Braun multiplier, a parallel prefix adders are designed and added at all the stages of the multiplier replacing 3 bit ripple carry adders. Similarly for 8×8 Braun multiplier we are replacing 7-bit Ripple Carry Adder by PPA. we are using Cadence Design Suite for designing and to perform functional verification of the adders and multiplier used in this paper. While designing we have set the following parameters.

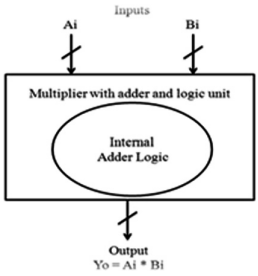

Fig. 1. General block diagram of multiplier.

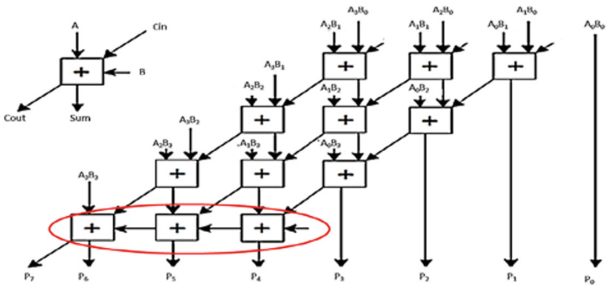

Fig. 2. Conventional Braun multiplier design.

- The precision of the multiplier is set, maximum up to the length of 8-bits.
- The design of multiplier will be performed in the conventional way and methods.
- Design of one conventional adder (like Ripple carry adder or Carry look ahead adder) and parallel prefix adder (Kogge Stone Adder, Brent Kung Adder).

Here we are using these adders for implement of multiplier as multiplication is done by successive addition. The performance can be measured and check for power consumption, computational delay and area utilized.

The propagation of signal in Braun multiplier is from one full adder to the other and hence the ripple like structure can be observed in the architecture of the Braun multiplier, this structure accounts to the delay in the result. And at the final stage also such structure can be observed. In conventional design of Braun multiplier, ripple carry adder is used at the last stage. The ripple carry adder at the all stage introduces significant amount of delay as the number of bits to be added increases.

The multiplier delay can be reduced by replacing the ripple carry adder with fast adder like parallel prefix adders. The proposed multiplier's design is shown in Fig. 3 where the Ripple Carry Adder at the last stage is replaced with parallel prefix adders like Kogge Stone Adder and Brent Kung adder at all the stages and we observed a similar ripple carry structure preceding to the final stage of the addition, in the proposed multiplier design these ripple stages are also replaced by the fast adders like Kogge Stone Adder and Brunt Kung Adder. To build 8 * 8 Braun multiplier, the bit size of inputs A and B is 8 bit wide and produces product of width 16 bit wide, partial products

are generated at 7 stages using parallel prefix adders which are replaced in place of Rippleacarry structure and to perform faster multiplication of binary numbers.

Design of Various Adders used for multiplier

i. *Ripple Carry Adder*

It is the basic adder structure which is implemented by cascading full adders in series. This structure is important for us to study as the Braun multiplier uses 1-bit full adder in a specific patter, the pattern in multiplier resembles the ripple structure of a ripple carry adder which is indicated in Figs. 2 and 3. The drawback of such structure is that the performance of multiplier is degraded due to the ripple of result from first to last. [1, 2] (Figs. 4 and 5).

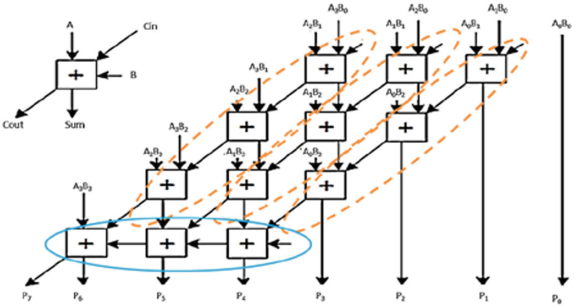

Fig. 3. Proposed Braun array multiplier design (Note: with reference to Fig. 3: A new architecture and novel approach, dotted circles form a ripple structure which are replaced by high speed adders like Kogge Stone or Brunt Kung Adder and also replacing the last stage of computation by high speed adder)

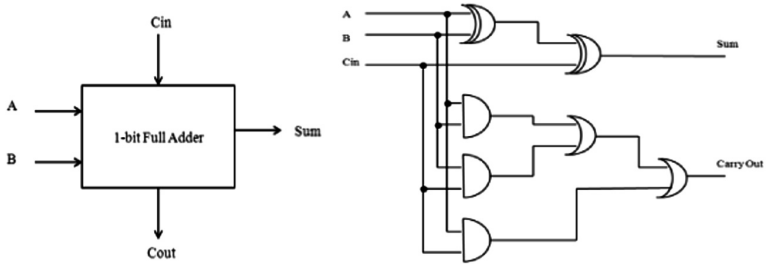

Fig. 4. Block diagram and schematic of 1-bit Full adder. [1, 2]

Equation of Ripple Carry Adder [8]

$$S_i = A_i \text{ XOR } B_i \text{ XOR } C_{i-1} \tag{1}$$

$$C_{i+1} = (A_i \text{ AND } B_i) \text{ OR } (B_i \text{ AND } C_i) \text{ OR } (C_i \text{ AND } A_i) \tag{2}$$

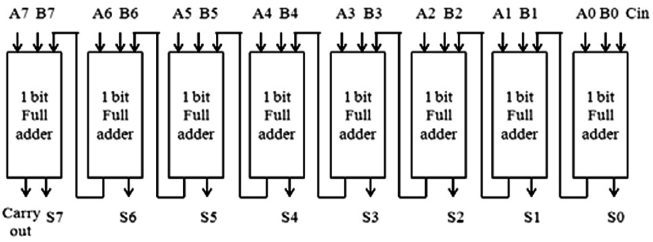

Fig. 5. Block diagram of 8-bit ripple carry adder

ii. *Parallel Prefix Adders*

Parallel prefix adders are most popular adder design used to speed up the binary addition. Parallel prefix adder, the acquirement of the parallel prefix adder carry bit differentiates the parallel prefix adder from other types of adders. In these adders, the carry bit is obtained in parallel form which makes the addition operation faster. Adders are derived from the family of Carry Look Ahead adder structure. The parallel prefix adders are represented in tree structure form to increase the speed of arithmetic operation. These adders are considered as the fastest adders and used in the high performance arithmetic circuits in the industries. Figure 6 shows the structured diagram of parallel prefix adder.

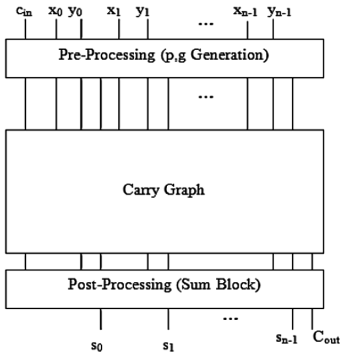

Fig. 6. Block diagram of parallel prefix adder structure. [1, 8]

Three stages involved in the design of parallel prefix adders are Pre-processing Stage, Carry generation and Post processing.

1. *Pre-processing:*

It computation a pair of signals in this phase namely generate and propagate signals, which corresponds to each ith state of A and B input sets. Propagate and generate signal are represent as shown below [8]:

$$\mathrm{Pi} = \mathrm{Ai}\,\mathrm{XOR}\,\mathrm{Bi} \tag{3}$$

$$\mathrm{Gi} = \mathrm{Ai}\,\mathrm{AND}\,\mathrm{Bi} \tag{4}$$

2. *Carry generation tree [8]*
Carry tree differentiates the various parallel prefix adders and it can be thought as the prime force for high performance in PPA Adders. In this phase the carries are computed much earlier using the two cells described below [8]:

Black Cell. It consumes two pairs of generate and propagate signals (Gi, Pi) and (Gj, Pj) as input and computes a pair of signals as generate and propagate signals (G, P) as output for the current stage [8].

$$\mathrm{G} = \mathrm{Gi}\,\mathrm{OR}(\mathrm{Pi}\,\mathrm{AND}\,\mathrm{Pj}) \tag{5}$$

$$\mathrm{P} = \mathrm{Pi}\,\mathrm{AND}\,\mathrm{Pj} \tag{6}$$

Grey Cell. It consumes two pairs of generate and propagate signals (Gi, Pi) and (Gj, Pj) as inputs and Computes a single generate signal G as output for the current stage [8]

$$\mathrm{G} = \mathrm{Gi}\,\mathrm{OR}(\mathrm{Pi}\,\mathrm{AND}\,\mathrm{Pj}) \tag{7}$$

3. *Post processing*
The last phase to compute sum which is common to all adders of PPA adder family. This stage involves the computation of sum bits which is given by [8]:

$$\mathrm{Si} = \mathrm{pi}\,\mathrm{XOR}\,\mathrm{Ci} - 1. \tag{8}$$

A. *Kogge Stone Adder:*
It is one of the parallel prefix adder, which has fastest carry tree to compute carries. It produces the carry signal in O (log n) time [1].

B. *Brent Kung Adder:*
Brent Kung Adder tree structure is similar to the Kogge Stone structure but the structure has a low fan-outs from each prefix cell and also has a large critical path which limits the high speed addition operation. Looking at the carry tree structure the design consumes less gates, uses less fan-outs and wiring compared to KS Adder [8].

4 Results and Analysis

In this section we have discuss the impact of different adders with various precision on the multiplier design. This section provides the simulation and comparative analysis with performance metric for various parallel prefix adder and conventional adder. We have also gives the impact of these adders, when used in the Braun Array Multiplier structure. The design of various blocks used in adders and multiplier is performed using CMOS technique and GDI technique, Cadence tool of version 6.1.6 to perform the schematic entry and Generic Process Design Kit of 180 nm technology to define the MOS device. In the first part schematic and simulation of various adder and Braun multiplier is depicted and in the second part a performance based comparative statement is presented (Figs. 7, 8, 9, 10, 11, 12, 13, 14, 15, 16).

A. *Multiplier Schematics and Simulations.*

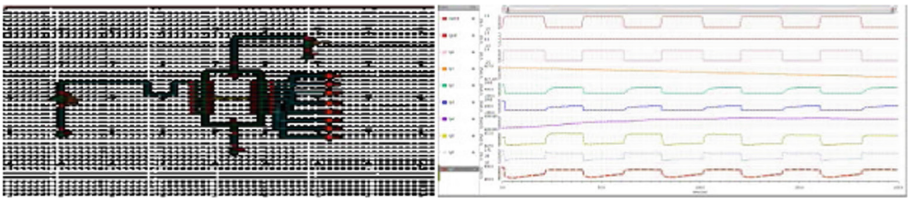

Fig. 7. Simulation of 4 bit multiplier in CMOS design using RC adder

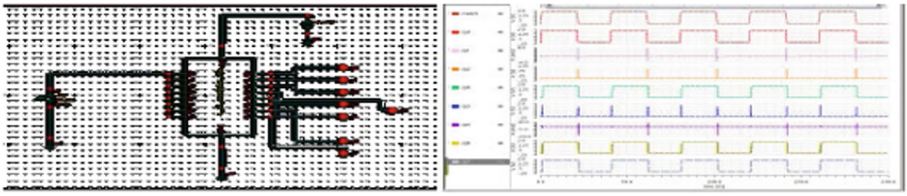

Fig. 8. Simulation of 4 bit multiplier in CMOS design using KS adder

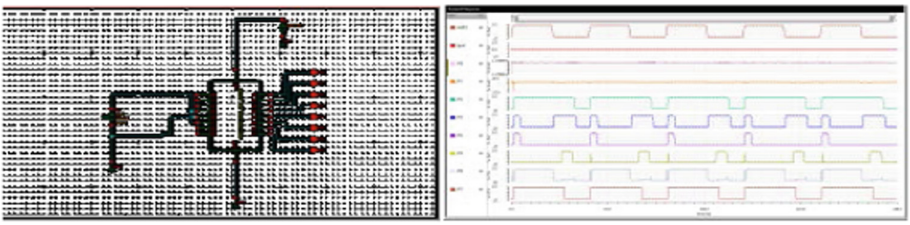

Fig. 9. Simulation of 4 bit multiplier in GDI design using KS adder

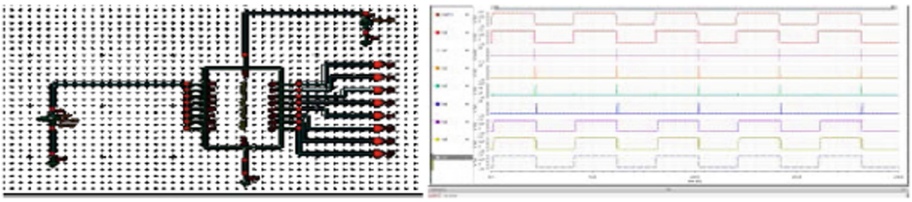

Fig. 10. Simulation of 4 bit multiplier in CMOS design using BK adder

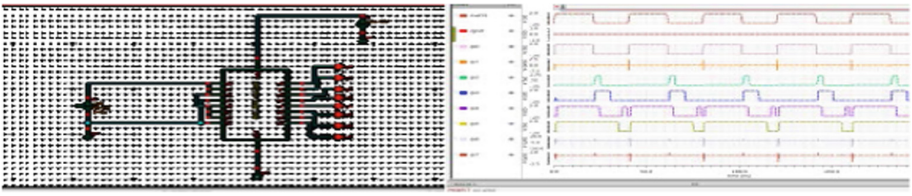

Fig. 11. Simulation of 4 bit multiplier in GDI design using BK adder

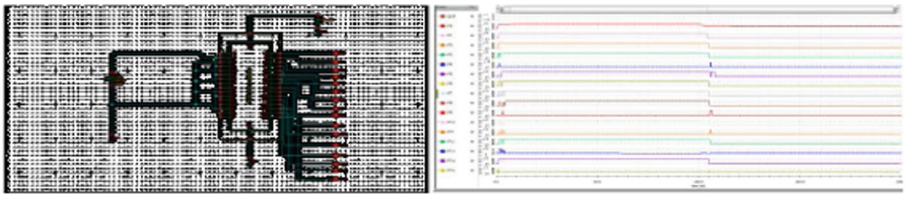

Fig. 12. Simulation of 8 bit multiplier in CMOS design using RC adder

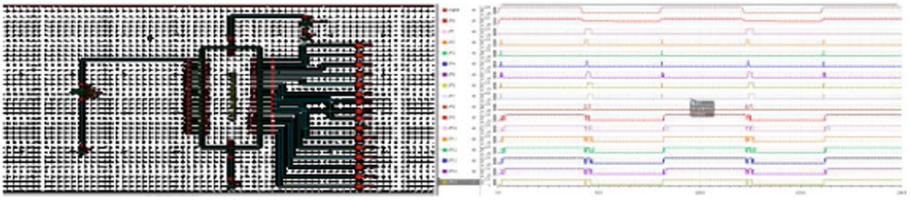

Fig. 13. Simulation of 8 bit multiplier in CMOS design using KS adder

Fig. 14. Simulation of 8 bit multiplier in GDI design using KS adder

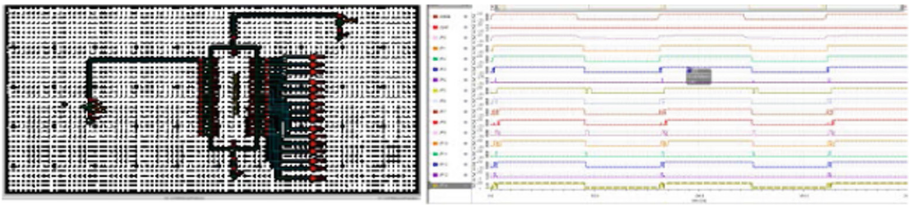

Fig. 15. Simulation of 8 bit multiplier in CMOS design using BK adder

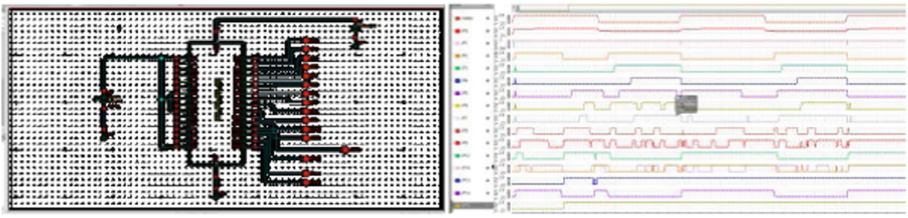

Fig. 16. Simulation of 8 bit multiplier in GDI design using BK adder

Table 1. Adder performance with 3-bit precession, CMOS and GDI technique [8]

Parameter		RCA CMOS	RCA GDI	KSA CMOS	KSA GDI	BKA CMOS	BKA GDI
Worst case delay	S0	11.36e-9	283.8e-12	11.24e-9	11.24e-9	11.32e-9	6.278e-9
	S1	21.38e-9	283.9e-12	21.46e-9	11.35e-9	11.32e-9	11.33e-9
	S2	**41.38e-9**	**285.5e-12**	**41.46e-9**	**21.37e-9**	**31.46e-9**	**21.34e-9**
	Cout	**151.3e-9**	**21.06e-9**	**61.51e-9**	**31.42e-9**	**71.48e-9**	**71.24e-9**
No. of transistors		**144T**	**42T**	**156T**	**60T**	**106T**	**38T**
Power		**20.35e-6**	**55.97e-6**	**35.42e-6**	**198.4e-6**	**5.387e-6**	**181.1e-6**

B. *Comparative analysis*

Multiplier designed using CMOS technique consumes low power in computing the result when compared with GDI Technique. Whereas the GDI technique utilizes less number of transistors to implement the given block and generates the results faster compared with CMOS technique. When a multiplier is to be designed using adder block, a care has to be taken in which adder itself is simplex and designed with optimal characteristics which is coated in this paper. In the initial stages the Gate Diffused Input

Table 2. Adder performance with 7-bit precession, CMOS and GDI technique [8]

Parameters		RCA CMOS	RCA GDI	KSA CMOS	KSA GDI	BKA CMOS	BKA GDI
Worst case delay	S0	392.9e-12	203.0e-12	556.8e-12	43.87e-9	518.9e-12	23.84e-9
	S1	392.9e-12	208.0e-12	556.7e-12	43.88e-9	518.9e-12	23.84e-9
	S2	593.0e-12	208.0e-12	556.9e-12	43.98e-9	518.9e-12	23.97e-9
	S3	779.0e-12	235.9e-12	565.2e-12	43.99e-9	518.8e-12	24.43e-9
	S4	964.0e-12	282.9e-12	649.2e-12	44.66e-9	566.9e-12	24.44e-9
	S5	1.150e-09	282.9e-12	653.8e-12	44.66e-9	681.2e-12	24.64e-9
	S6	1.340e-09	546.9e-12	671.1e-12	45.76e-9	695.8e-12	24.86e-9
	Cout	**101.4e-9**	**21.6e-9**	**21.57e-9**	**53.61e-9**	**41.39e-9**	**101.6e-9**
No. of transistors		**336T**	**98T**	**420T**	**164T**	**286T**	**106T**
Power		**15.4e-6**	**4.0447e-6**	**91.87e-6**	**293.1e-6**	**33.7e-6**	**360.0e-6**

Table 3. Multiplier performance with 4-bit precession, CMOS and GDI technique

Parameter		RC A CMOS	KS A CMOS	KS A GDI	BK A CMOS	BK A GDI
Worst case delay	P0	136.6E-12	136.6E-12	136.5E-12	136.6E-12	136.6E-12
	P1	596.0E-12	532.4E-12	408.6E-12	477.2E-12	393.7E-12
	P2	998.1E-12	580.1E-12	410.3E-12	555.6E-12	507.0E-12
	P3	1.051E-12	600.0E-12	777.3E-12	835.1E-12	717.5E-12
	P4	1.326E-9	771.6E-12	792.7E-12	965.1E-12	980.8E-12
	P5	1.50E-9	1.035E-9	797.3E-12	1.296E-9	1.171E-9
	P6	1.83E-9	1.481E-9	1.155E-9	21.36E-9	21.85E-9
	P7	**21.63E-9**	**21.33E-9**	**1.163E-9**	**21.64E-9**	**21.94E-9**
No. of transistors		**222**	**564**	**212**	**414**	**146**
Power		**8.22383E-5**	**9.2954E-5**	**0.002355**	**3.7741E-5**	**0.0016089E-6**

Table 4. Multiplier performance with 8-bit precession, CMOS and GDI technique

Parameter		RC A CMOS	KS A CMOS	KS A GDI	BK A CMOS	BK A GDI
Worst case delay	P0	136.6E-12	136.6E-12	136.5E-12	136.5E-12	136.5E-12
	P1	507.8E-12	136.6E-12	136.5E-12	136.5E-12	136.5E-12
	P2	507.8E-12	533.1E-12	400.1E-12	341.4E-12	341.4E-12
	P3	554.2E-12	533.1E-12	400.1E-12	341.4E-12	341.4E-12
	P4	507.8E-12	533.1E-12	400.1E-12	477.9E-12	477.9E-12
	P5	507.8E-12	533.1E-12	400.1E-12	477.9E-12	477.9E-12
	P6	920.2E-12	533.1E-12	400.1E-12	477.9E-12	477.9E-12
	P7	968.6E-12	533.1E-12	400.1E-12	481.2E-12	481.2E-12
	P8	968.6E-12	533.1E-12	1.069E-9	507.0E-12	507.0E-12
	P9	1.041E-9	905.8E-12	1.104E-9	866.5E-12	866.5E-12
	P10	1.015E-9	1.189E-9	1.105E-9	1.059E-9	1.059E-9
	P11	1.04E-9	1.259E-9	1.302E-9	1.088E-9	1.088E-9
	P12	1.11E-9	1.295E-9	1.151E-9	1.151E-9	1.151E-9
	P13	1.122E-9	1.295E-9	1.151E-9	1.194E-9	1.194E-9
	P14	1.122E-9	1.312E-9	1.315E-9	1.194E-9	1.194E-9
	P15	**1.978E-9**	**1.338E-9**	**1.519E-9**	**1.455E-9**	**1.445E-9**
No. of transistors		**678**	**3324**	**1276**	**2386**	**870**
Power		**7.43509E-05**	**0.000961**	**0.00116312**	**0.00011783**	**0.0084047**

technique is used to optimization of area & delay of adder blocks, whereas the CMOS technique can be used at the final stage to generate a full swing output (Tables 1, 2, 3 and 4).

5 Conclusion

Multipliers in Signal Processing and processors are core and important block. Hence the design of high speed multiplier is essential, In order to meet such needs the proposed architecture gives a novel approach to design and implement the multipliers using conventional adders and parallel prefix adders which is presented in paper and as

the performance (like speed, area and delay) is prime concern in the design which is increased (reduction in number of transistors required to design, increasing speed and reducing delay). In this paper provided a new architecture and novel method to design a multiplier, and we have designed, modeled and implemented the same on cadence design suite and verified its behavior for the same. The multipliers designed are of 4-bit and 8-bit precession Braun multipliers using parallel prefix adders and coated comparative analysis obtained. From the analysis and comparative statement, we observe that the blocks and multiplier designed using Gate Diffused Input technique provides less delay in generating results and also uses few transistors to implement the structure; CMOS technique uses less power but uses more number of transistors to implement the logic. Designer can opt the proposed method where the initial stages are designed using GDI technique and final stage with CMOS technique, the circled up blocks in Fig. 3 are redefined with advance adder structure and thereby improving the result of multiplier.

References

1. Shinde, K.D., Jayashree, C.N.: Modeling, design and performance analysis of various 8-bit adders for embedded applications. In: Elsevier International Conference on Emerging Research in Computing, Information, Communication and Applications at NMIT, Bangalore, Karnataka, India, pp. 823–831, August 2014. ISBN 9789351072621
2. Shinde, K.D., Nidagundi, J.C.: Design of fast and efficient 1-bit full adder and its performance analysis. In: IEEE International Conference on "Control, Instrumentation, Communication and Computational Technologies (ICCICCT-2014)" at NIU, Tamilnadu, India, pp. 1275–1279, July 2014. ISBN 978-1-4799-4191-9
3. Shinde, K.D., Nidagundi, J.C.: Comparative analysis of 8-bit adders for embedded applications. In: IJERT in NC on "Real Time System". City Engineering College Bangalore, Karnataka, India, pp. 682–687, May 2014. ISSN 2278-0181
4. Zamhari, N., Voon, P., Kipli, K., et al.: Comparison of parallel prefix adder (PPA). In: Proceedings of the World Congress on Engineering 2012, WCE 2012, vol 2, 4–6 July 2012, London, U.K (2012)
5. Thakur, M., Ashraf, J.: Design of Braun multiplier with Kogge stone adder & it's implementation on FPGA. Int. J. Sci. Eng. Res. **3**(10) (2012). ISSN 2229-5518
6. Prakash, M., Karthick, S.: Simulation and comparative analysis of different types of multipliers. IJAICT **1**(7) (2014)
7. Givone, D.D.: Digital Principles and Design, chap. 5, pp. 231– 240. Tata McGraw-Hill (2002)
8. Shinde, K.D., et al.: Modeling of adders using CMOS and GDI logic for multiplier application: a VLSI based approach. In: Proceedings of the IEEE International Conference on Circuit, Power and Computing Technologies (ICCPCT). https://doi.org/10.1109/iccpct.2016.7530213