Designing ibex RISC-V Cores using OpenROAD Flow Script

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***Abstract*—This paper describes the steps involved in initiating Physical Design for an ibex RISC-V core using ORFS. OpenROAD Flow is a complete RTL-to-GDS flow created exclusively with open-source technologies. The project's goal is to achieve automated, no-human-in-the-loop digital circuit design in 24 hours. The many features that tool brings to the physical design methodology is discussed along with few implementation challenges**

Keywords—component, formatting, style, styling, insert (*key words****)***

I. Introduction

OpenROAD is the industry's most popular open-source fundamental application for semiconductor digital design. It lowers the obstacles of cost, risk and uncertainty in hardware design to enable open access, knowledge, quick innovation, and faster design turnaround. The OpenROAD program provides customizable flow control via an API with Tcl and Python bindings.

II. ORFS For Physical Design

OpenROAD-flow-scripts (ORFS) is a flow controller that provides a set of open-source tools for automated digital ASIC design, from synthesis through layout. It contains tests for Synthesis, Placement and Routing (PnR), STA (Static Timing Analysis), DRC (Design Rule Check), and LVS (Layout Versus Schematic) in a completely automated RTL-to-GDSII design path. ORFS promises to provide a versatile and adaptable environment for digital ASIC design, allowing users to select and combine various tools as needed.

OpenROAD is utilized as a physical design plugin in ORFS, and it may be adjusted and adapted to match the unique demands of the design project. ORFS's OpenROAD plugin gives you access to sophisticated capabilities including hierarchical placement, global routing, and comprehensive routing optimization. ORFS supports a variety of public and private PDKs such as GF180, Skywater130, ASAP7, and other public PDKs.

III. ORFS For RISC-V CPU Design

The RTL to GDSII Flow is started by bringing the Verilog RTL script of ibex RISC-V Core design loading it onto ORFS. The program then generates the necessary files for each stage of the design cycle. This entire procedure is automated; thus, no human participation is required. Each stage is carried out progressively, and the procedure concludes with the creation of the GDSII file. Together with the GDSII file creation, the Design Rule Checking (DRC) and Layout Versus Schematic (LVS) findings are shown. The retrieved GDSII file format is the industry standard for Integrated Circuit layout and manufacturing, and it may be inspected using Magic or Klayout. For the RTL Design of the RISC-V Core, the appropriate GDSII file was generated successfully as a result of the automated process of ORFS and its underlying components.

IV. Implementation Challenges

Some implementation strategies for alleviating interconnect resistances are needed, in order to yield high performance designs. There has to be workarounds for intensive wire and via scaling issues. The implementation of metal layer promotion and multiple-width configurable wires need to be feasible. The fully automated via pillar design flow reduces the impact of high resistance and becomes essential in high performance designs for modern process technologies.

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