Main Assignment

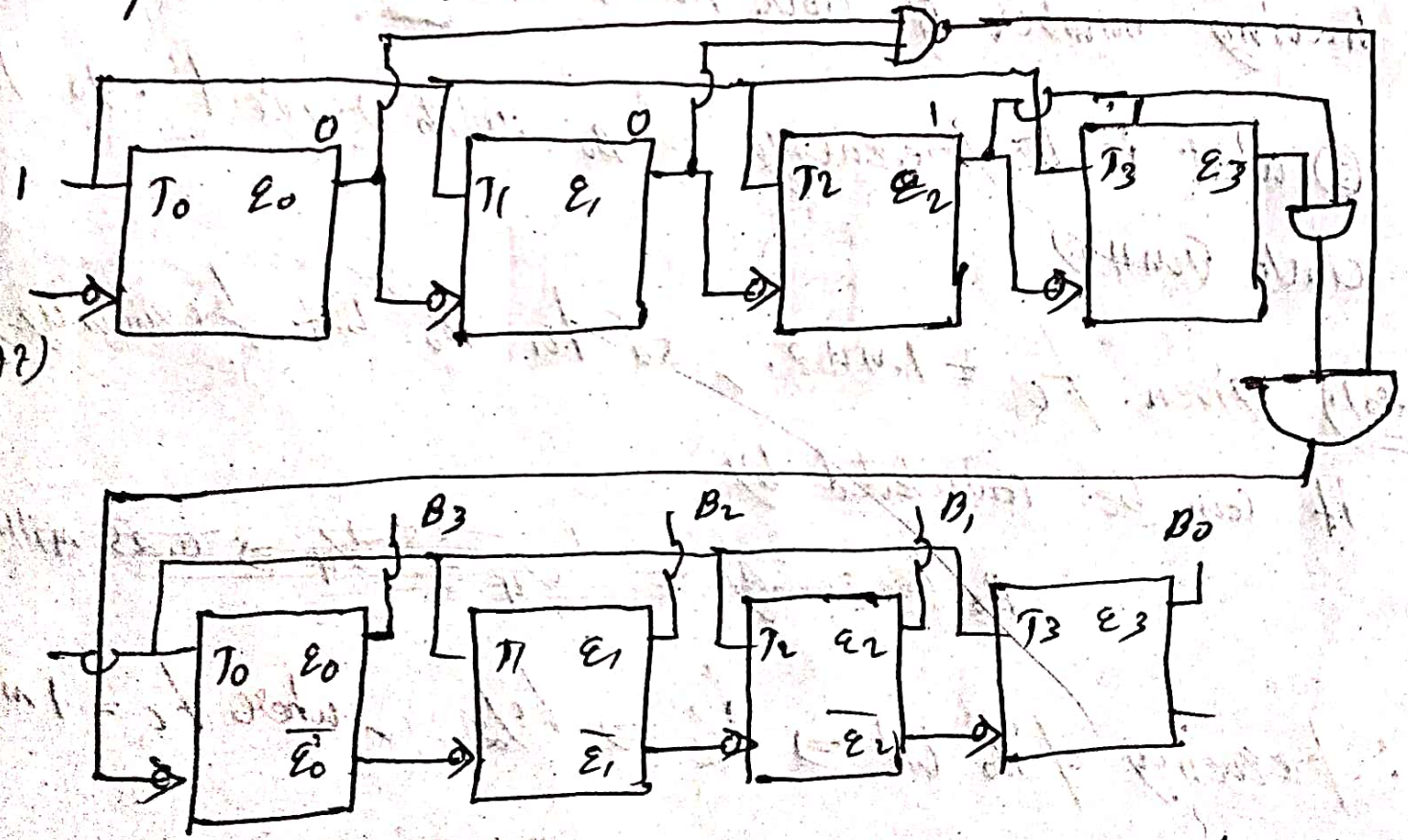
8/12/23

Venkat Vatturi

*there are 2 counters, "Counter A" being a Asynchronous up counter & "Counter B" is an asynchronous down counter and at T=0, 0000 & 1111 are loaded respectively as shown. Clock source (clk) available is 1MHz.

① Complete the design such that Counter B decrements by one value each time when decimal "12" appears at output of counter A (A_0 being LSB)?

Sol):



From the question given data, when $A_3 A_2 A_1 A_0 = 1100$ then clk should be '1'; so, when it triggers down Counter., & the block diagram is shown above.

(2) What is the decimal value at outputs of U/D counter A & B at T = 0.2 milliseconds?

Sol: given that $f_c = 1MHz$

$$T = 1/f \Rightarrow 1/10^6$$

$$\boxed{T = 1\mu sec}$$

we know that the point for counting 0000 to 1111 we have total up to 16 clock pluses., so for remaining clock pluses are 3 which from (0000 to 0011).

for the up counter and for the down counter having that total number of clock and subtraction to the overall clock pluses i.e 15-12 ⇒ 3., for down-counter having number of clock pluses are 3 (0011).

(3) what is the frequency of B_0 with respect to the clock (1MHz).

Sol: given $f_c = 1MHz$., so for B_0 bit frequency, it can be calculated by

~~B_0 frequency = $f_c/4$ ⇒ 0.25 milliseconds~~

∴ frequency of B_0 bit ⇒ $f/2$ ⇒ $f_c/2$ - where $f_c = 1MHz$.

$$\therefore \frac{1MHz}{2} \Rightarrow 0.5MHz.$$

*The above answer based on the previous ~~cod~~ classes out come.