

3 bit multiplier

EDA playground

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Tools & Simulators

Icarus Verilog 0.10.0 11/23/14

Compile Options

-Wall -g2012

Run Options

Run Options

☐ Open EPWave after run

☐ Show output file after run

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Examples

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testbench.sv

SV/Verilog Testbench

```
1 // Code your testbench here
2 // or browse Examples
3 module tb();
4   reg[2:0] a,b;
5   wire[5:0] p;
6
7   mul_3bit m1(a,b,p);
8   initial begin
9     a=3'b100; b=3'b101;
10    #2 a=3'b110; b=3'b001;
11    #2 a=3'b101; b=3'b011;
12    #2 a=3'b111; b=3'b001;
13  end
14  initial
15    $monitor("time=%0d a=%b b=%b p=%b", $time, a, b, p);
16 endmodule
```

design.sv

SV/Verilog Design

```
1 // Code your design here
2 module mul_3bit(a,b,p);
3   input[2:0] a,b;
4   output reg[5:0] p;
5   wire[1:11] w;
6
7   and a1(p[0],a[0],b[0]);
8   and a2(w[1],a[0],b[1]);
9   and a3(w[2],a[1],b[0]);
10  xor x1(p[1],w[1],w[2]);
11  and a4(w[3],w[1],w[2]);
12
13  and a5(w[4],a[0],b[2]);
14  and a6(w[5],a[1],b[1]);
15  and a7(w[6],a[2],b[0]);
16  xor x2(p[2],w[4],w[5],w[6],w[3]);
17  and a8(w[7],w[4],w[5],w[6],w[3]);
18
19  and a9(w[8],a[1],b[2]);
20  and a10(w[9],a[2],b[1]);
21  xor x3(p[3],w[7],w[8],w[9]);
22  and a11(w[10],w[7],w[8],w[9]);
23
24  and a12(w[11],a[2],b[2]);
25  xor x4(p[4],w[10],w[11]);
26  and a13(p[5],w[10],w[11]);
27 endmodule
```

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```

Log

Share

```
[2024-01-22 04:55:17 UTC] iVerilog '-ka11' '-g2012' design.sv testbench.sv && unbuffer vvp a.out
time=0 a=100 b=101 p=010100
time=2 a=110 b=001 p=000110
time=4 a=101 b=011 p=001111
time=6 a=111 b=001 p=000111
Done
```

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EPWave

From: 0s To: 6s

Get Signals Radix 100% 2s

a[2:0]	4	0	6	0
b[2:0]	5	1	5	0
p[5:0]	14	6	0	0
a[2:0]	4	6	6	0
b[2:0]	5	1	5	0
p[5:0]	14	6	0	0
w[1:11]	220	21	220	424

Note: To revert to EPWave opening in a new browser window, set that option on your user page.