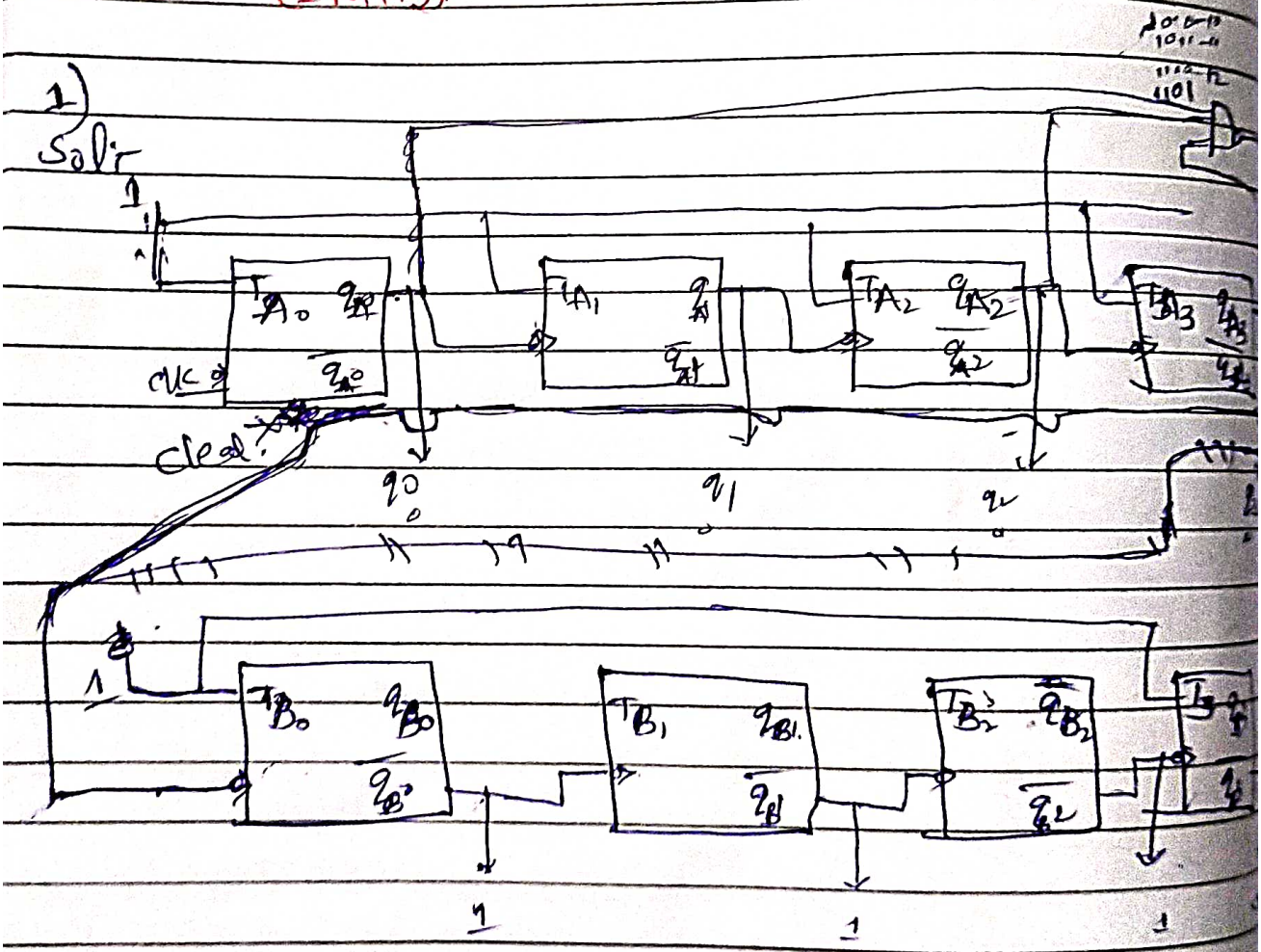
Assignment:-

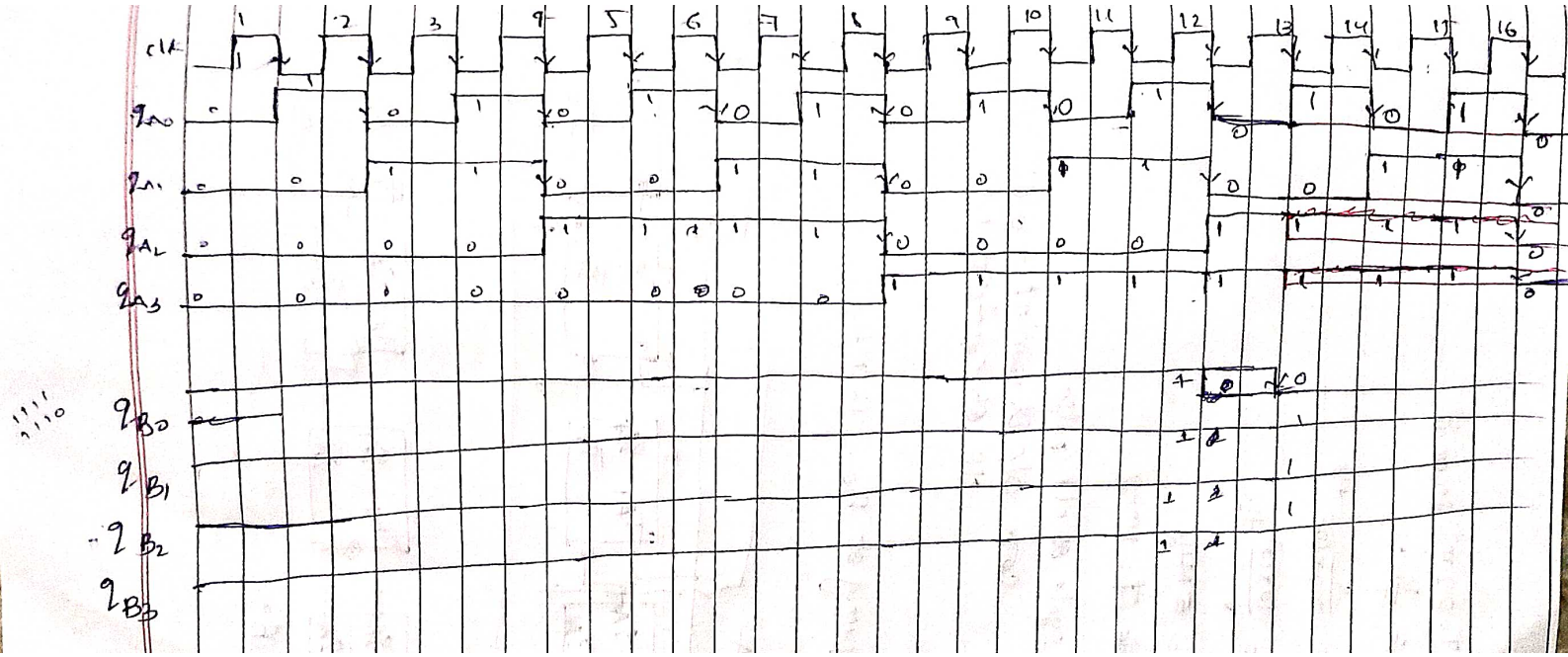
There are 2 counters. "Counter A" being asynchronous up Counter & "Counter B" is an asynchronous down Counter and at T=0, 0000 & 1111 are loaded respectively as shown. clock source (clk) available is 1 MHz.

1. Complete the design such that counter B decrements by one value each time when decimal "10" appears at o/p of counter A (A0 acts as LSB)?

2. what is the decimal value at o/p of both Counter A & Counter B at T = 0.2 milliseconds?

3. what is the frequency of B_0 with respect to clk (1 MHz).




1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
clk
q_{A0}
q_{A1}
q_{AL}
q_{A3}
q_{B0}
q_{B1}
q_{B2}
q_{B3}

2)

Sol:-

$dt = T = 0.2$ mili seconds

$f = \frac{1}{T}$ Hz

$f = \frac{1}{0.2 \times 10^{-3}}$ Hz

$f = \frac{10 \times 10^{3}}{2}$ Hz

$f = 5$ MHz.

1 cycle of $f = 1$ MHz

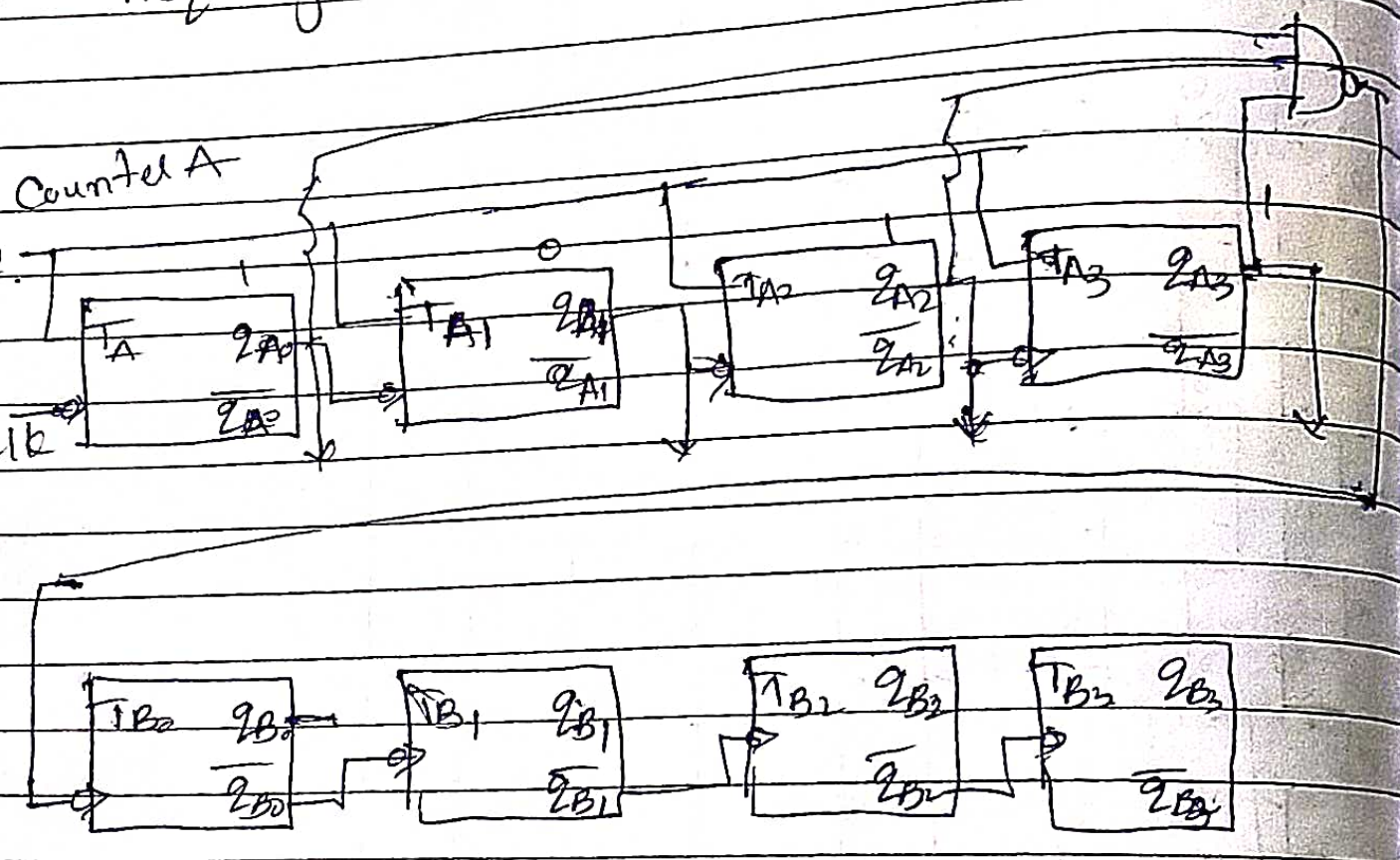
at 5th cycle of clk pulse

o/p of counter A = 0101

o/p of counter B = 1111

3)

Sol: frequency of $B_0 = 13$ MHz,



counter B.