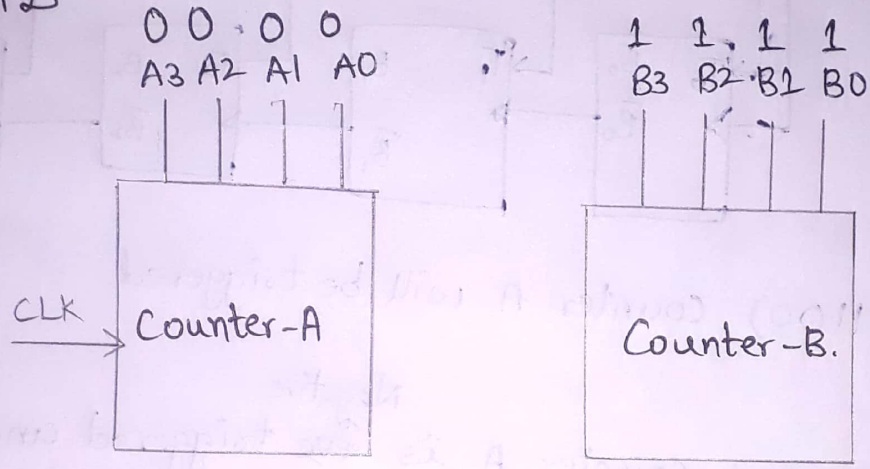
Assignment.

There are: 2 Counters, "Counter-A" being asynchronous up counter & "Counter-B" is an asynchronous down counter and at T=0, 0000 & 1111 are loaded respectively as shown. clock source (CLK) available is 1MHz

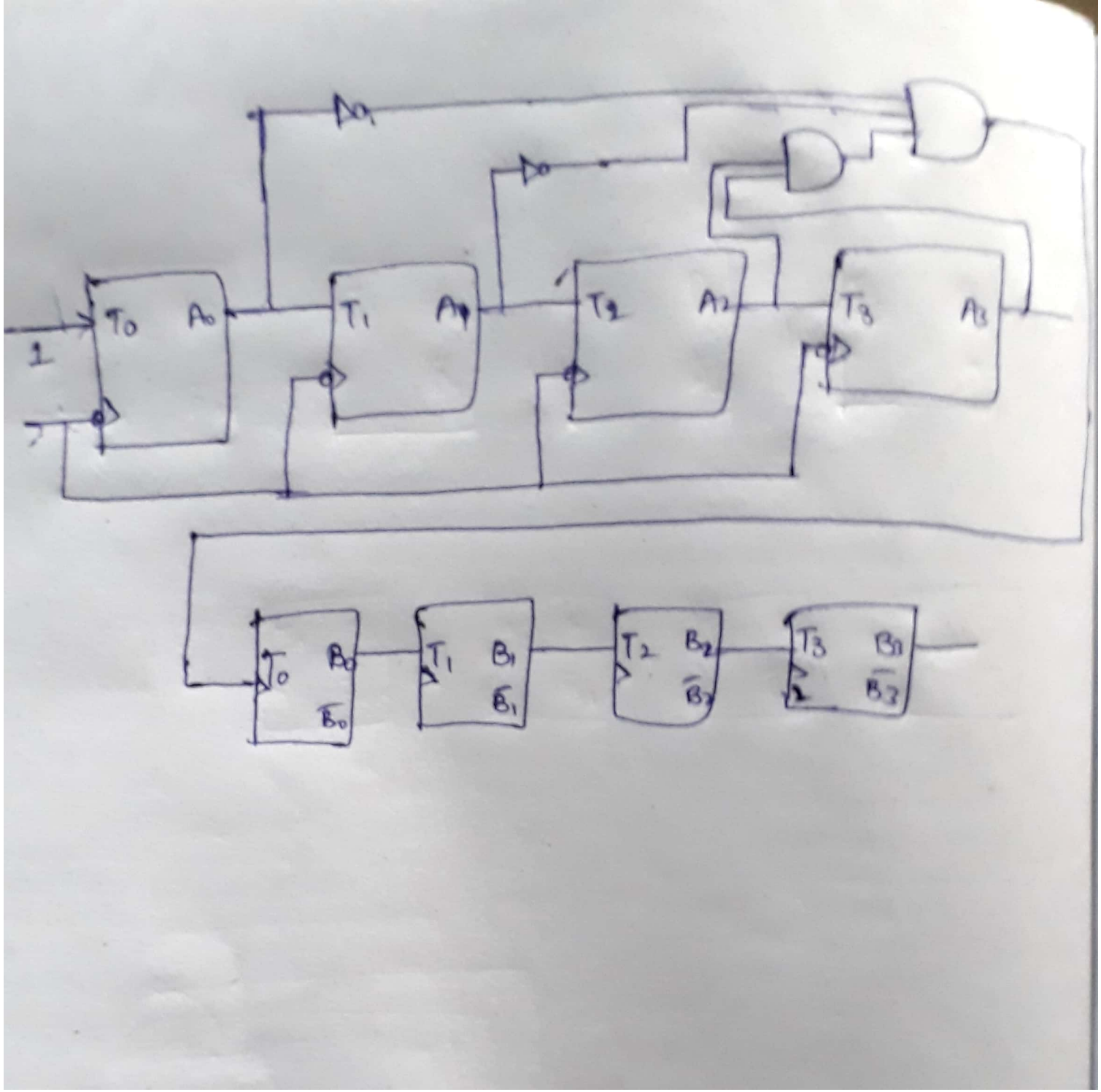


1. Complete the design such that Counter B decrements by One value each time when decimal "12" appears at output of Counter A (A0 being LSB)?

a) Find the no. of flipflops required

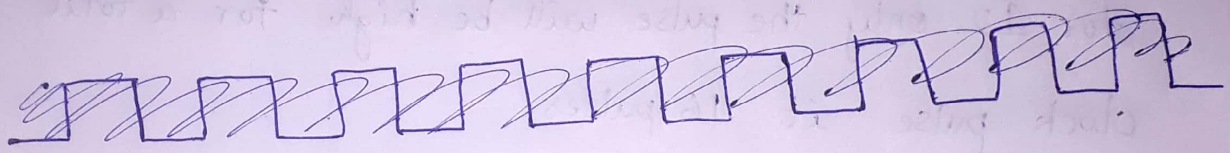
$$\log_2 16 = 4$$

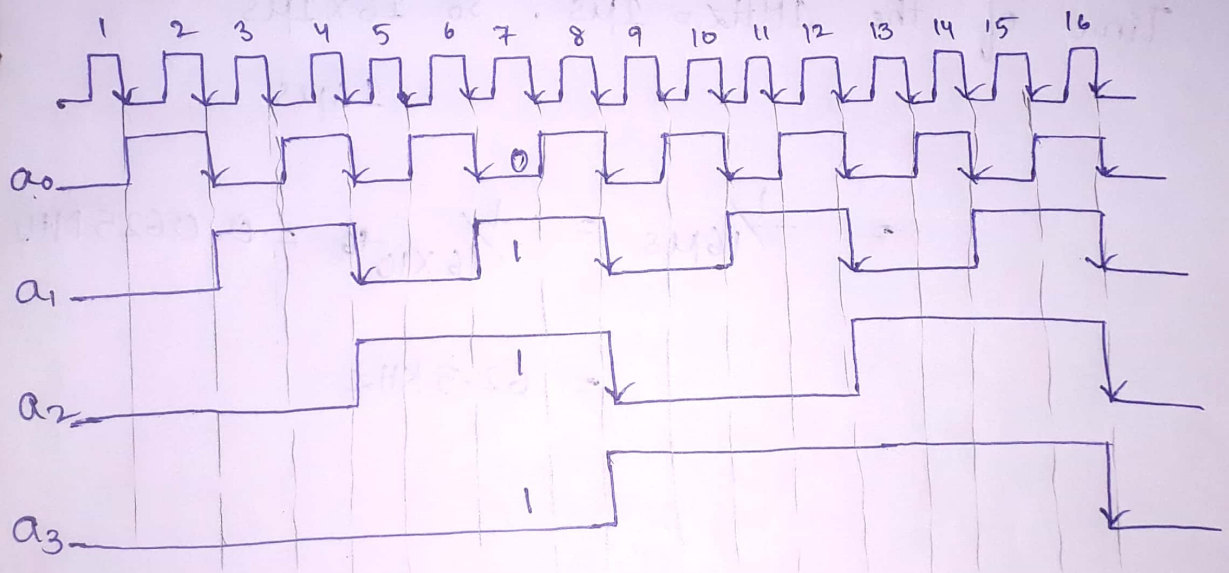
b) Consider any type of flipflop here I am considering T- flipflop.



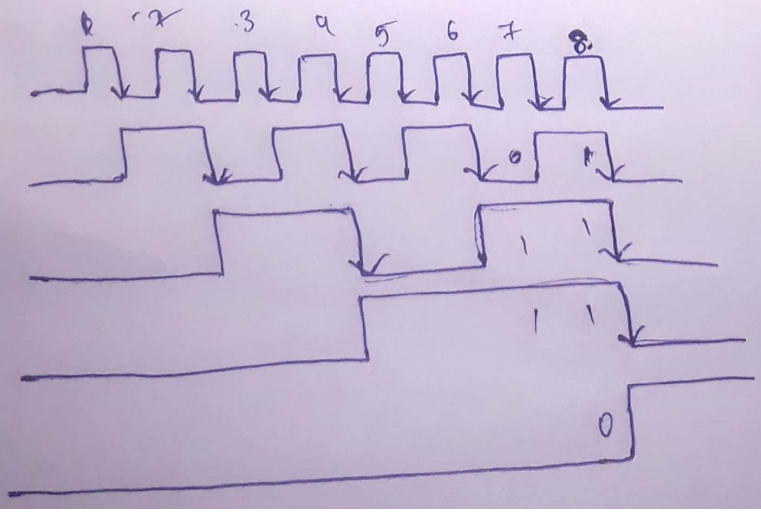
approximately Counter B repeats 12 times. So In counter B when a value decrements 12 times then it is equal 0011 (3)

The counter A is a up counter so the decimal value of that 7 (0111)

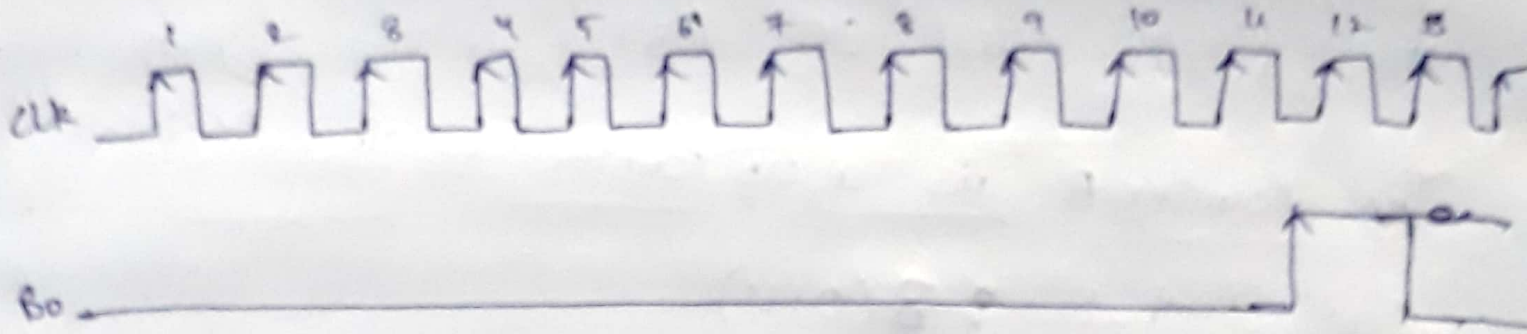




Clock pulses of Counter A



3. What is the frequency of B0 with respect to CLK (1MHz)?



For 12 only the pulse will be high for a total clock pulse it 16 pulses

Time of the 1MHz = 1μs .. So 16 x 1μs

= 16μs

= $1/16\mu s$ = $1/16 \times 10^{-6}$ = 0.0.625 MHz

= 62.5 KHz

= $\frac{62.5}{2}$ = 31.25.