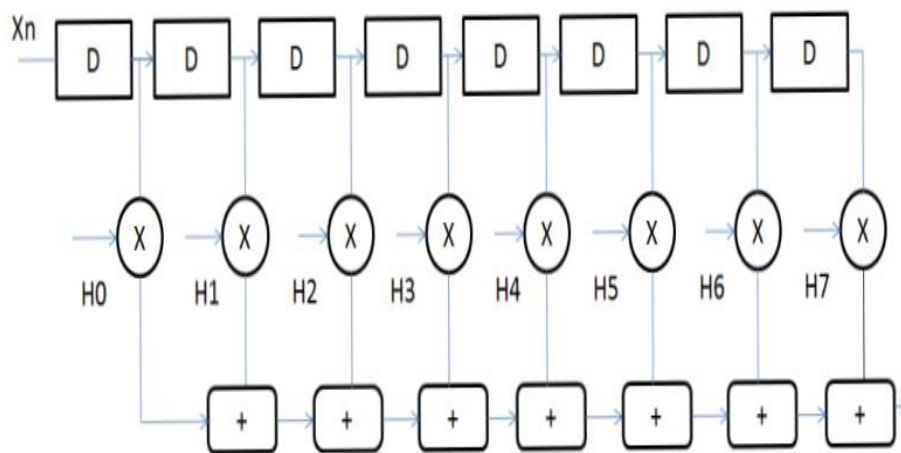


IMPLEMENTATION OF OPTIMIZED DIGITAL FILTER USING HAN CARSLON ADDER

A filter is a device or process that removes some unwanted components or features from a signal. For processing of signal filter can be divided into two types. Finite Impulse Response (FIR) filter, Infinite Impulse Response (IIR) filter.

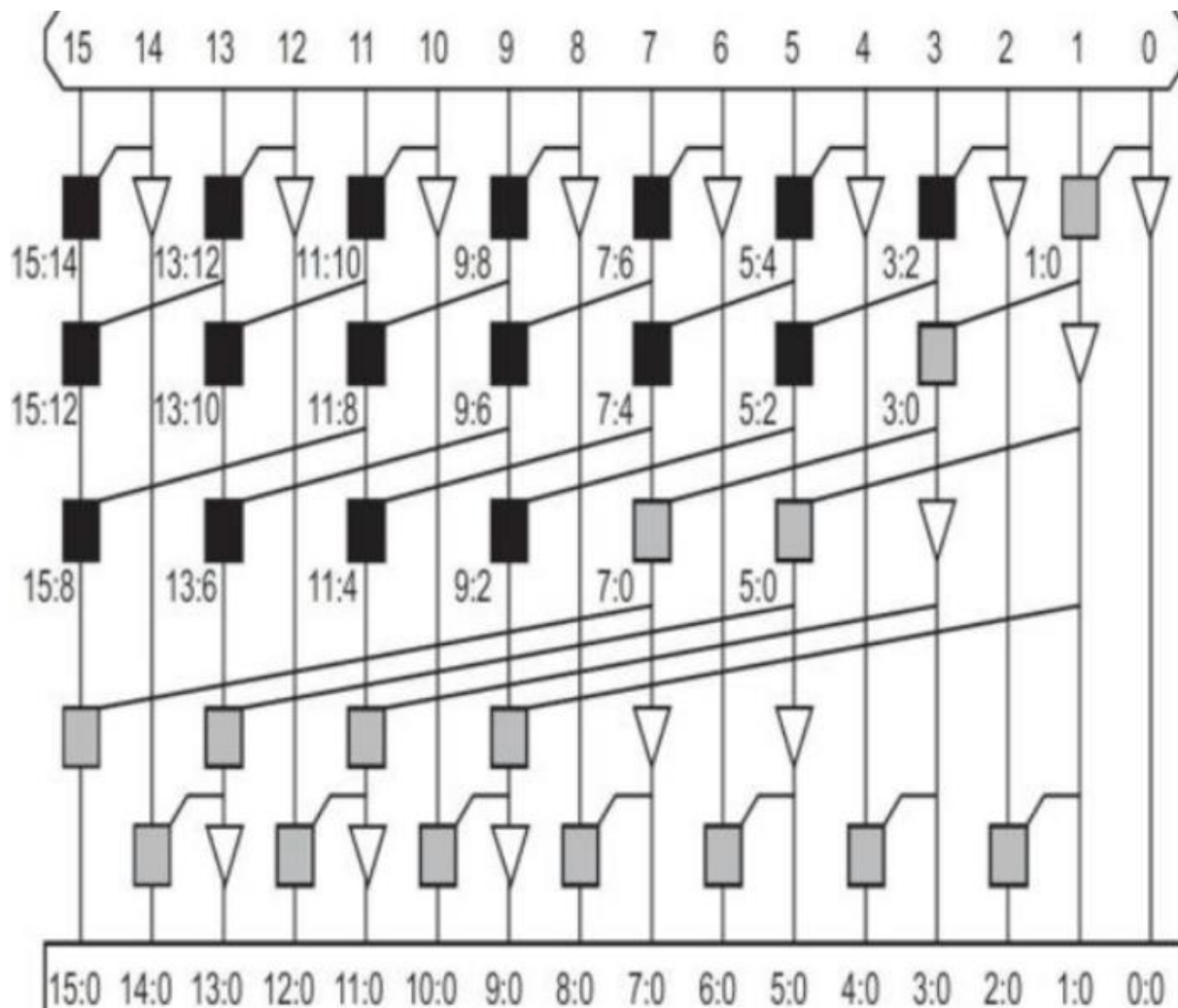
In these project I am using FIR digital filter with Han Carselon adder. Han Carselon adder is one of the adder from Parallel Prefix adder (PPA). Han-Carlson adder contains a good trade-off between fan out, number of logic levels and number of black cells. because of this, Han-Carlson adder can achieve equal to speed execution admiration to KoggeStone adder, at lower power utilization and territory . In this manner it is fascinating to execute a speculative HanCarlson adder. the Han-Carlson adder in which the two Brent-Kung rows at the initial and toward the end of the graph are unaltered, while the last Kogge-Stone row is pruned.



It is FIR 8-bit digital filter to construct these digital filter here we are using

8 D-flipflops, 8 multipliers and 7 adders.

For N- bit digital filter it requires N D-flipflops, N multipliers and N-1 adders.



It is circuit diagram of Han Carlson adder by using gray cells and black cells. Han carlson adder consists of 17 black cells and 15 gray cells.

1. Pre processing

This step involves computation of generate and propagate signals corresponding too each pair of bits in A and B.

$$p_i = A_i \text{ xor } B_i$$

$$g_i = A_i \text{ and } B_i$$

2 . Carry look ahead network

This block differentiates KSA from other adders and is the main force behind its high performance. This step involves computation of carries corresponding to each bit . It uses group propagate and generate as intermediate signals .

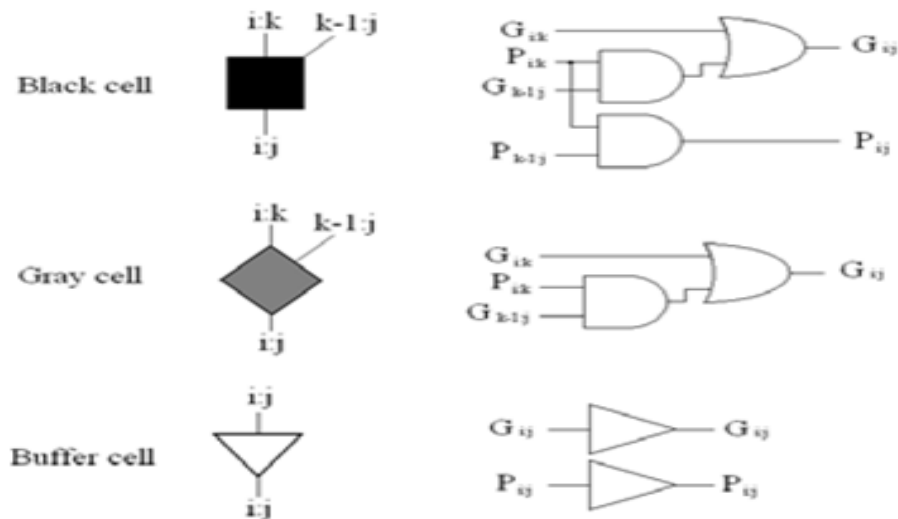
$$P_{i:j} = P_{i:k+1} \text{ and } P_{k:j}$$

$G_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j})$

3. Post processing

This is the final step and is common to all adders of this family (carry look ahead). It involves computation of sum bits.

$S_i = p_i \text{ xor } C_{i-1}$

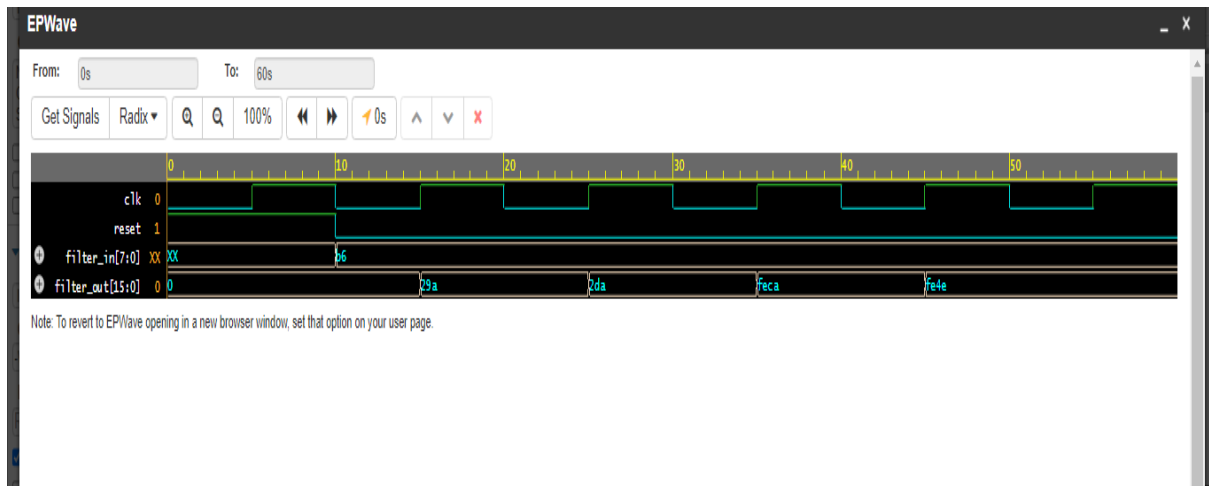


Gray Cells, Black Cell and buffer

The screenshot shows the EDA Playground interface with the following components:

- Top Bar:** Includes buttons for Run, Save, Copy, and a link to support email. It also features a banner for a free webinar on February 16.
- Left Panel (testbench.v):** Contains Verilog testbench code for an FIR filter. It instantiates the unit under test (UUT) and sets up a clock and reset signal.
- Right Panel (design.v):** Contains the Verilog code for the FIR filter. It defines coefficients and implements the filter logic using a delay register, multipliers, and adders.
- Bottom Panel:** Includes a log window showing simulation results and a button to open the EPWave window.

Verilog code in eda playground



EP Wave of digital filter

Advantages of Han Carslon adder

High Speed

Parallel Processing

Efficiency

Reduced Power Consumption

Applications of Han Carslon adder

Arithmetic Logic Units (ALUs)

Digital Signal Processing (DSP)

Graphics Processing Units (GPUs)