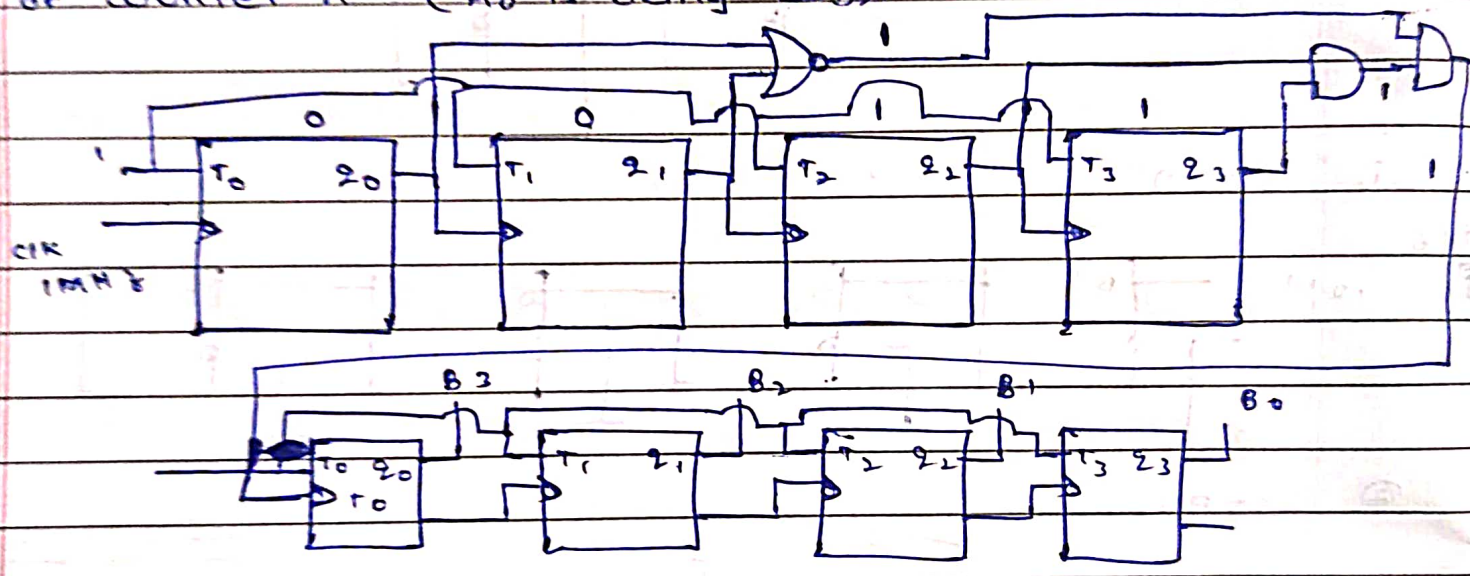
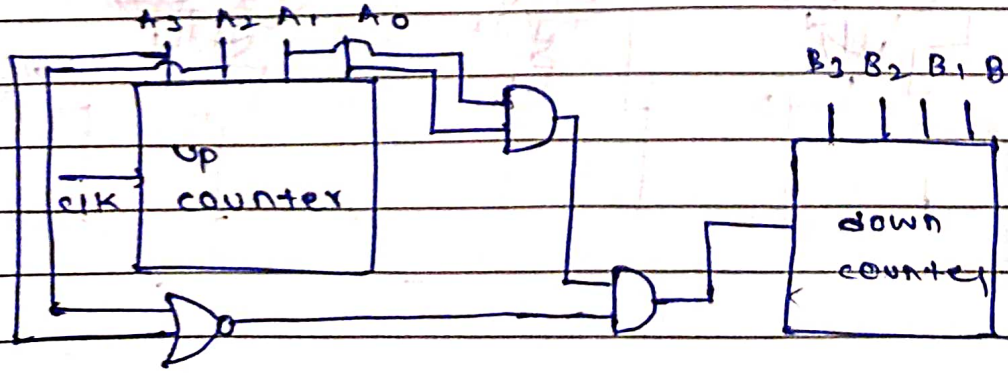
Assignment:

- Given 2 counters, "counter A" being asynchronous up counter and "counter B" is an asynchronous down counter and T=0, 0000 & 1111 are loaded respectively. Given clock frequency is 1MHz.

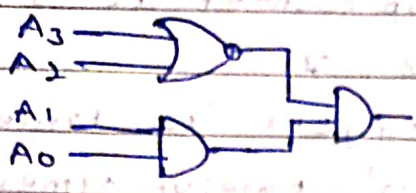
1. complete the design such that counter B decrements by one value each time when decimal "12" appears at o/p of counter 'A' (A_0 is being LSB).



Hence the down counter triggers when up counter counts '12' i.e when up counter has value 1100 i.e, when $A_3 A_2 A_1 A_0 = 1100$ the o/p should be '1' so that it triggers down counter.



The combinational logic used between two counters is



2. What is the decimal value at outputs of both counters A & B at T = 0.2 milli seconds?

Given,

clock frequency, F = 1MHz.

Time period of one clock pulse is

$$T = 1/F$$

$$= \frac{1}{10^6} \text{ sec}$$

$$\boxed{T = 1 \mu\text{sec}}$$

We need to find counter value at 0.2 msec i.e

0.2×10^3 μsec = 200 μs.

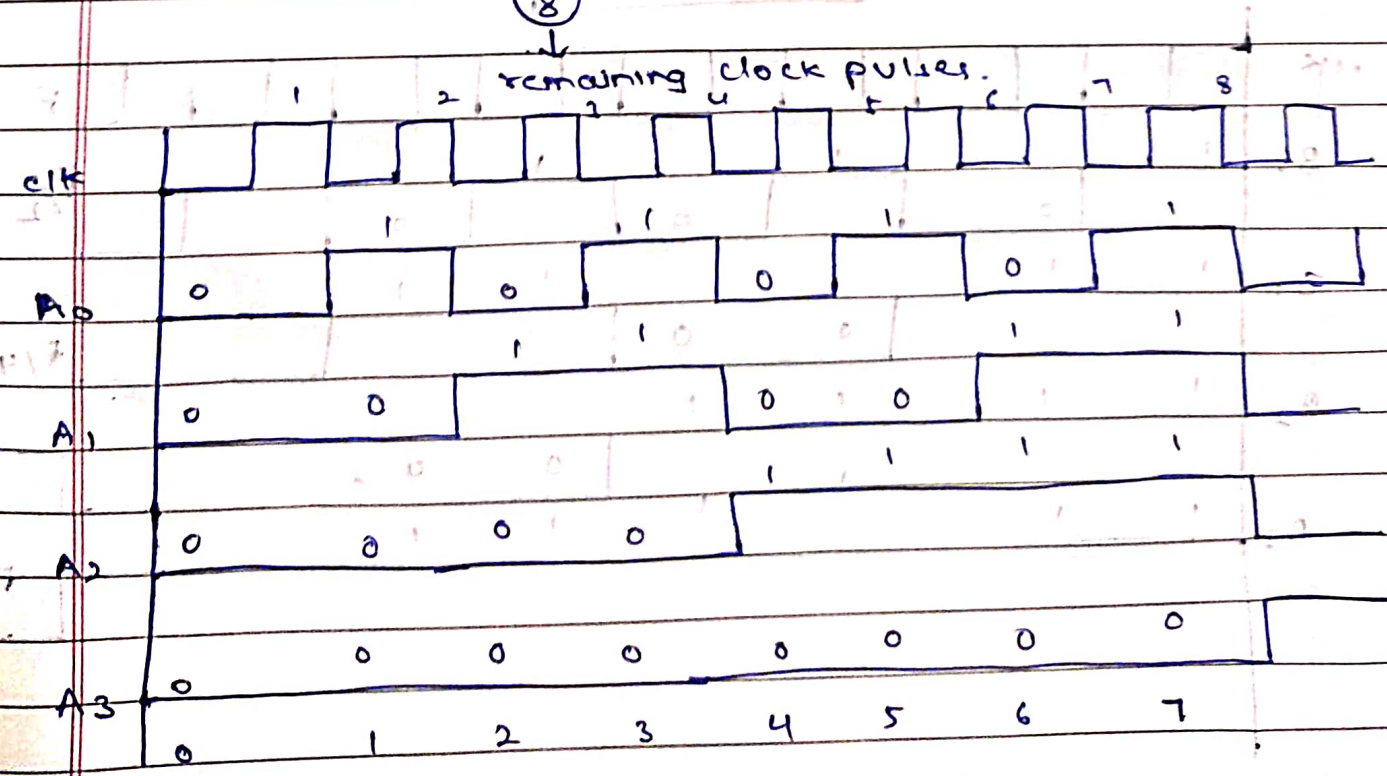
We know that, "For an up counter to count from 0000 to 1111 we need 16 clock pulses.

Hence, 16) 200 ((12) → total complete cycles that count from zero to 15.

192

(8)

↓ remaining clock pulses.



→ Hence, the output of the up counter at 0.2 msec i.e at loops is '0111' i.e, 7.

→ Now, the down counter triggers '12' times as the up counter counts value '12' twelve times. Hence, the down counters counts down '12' values from '1111'.

So, 15 − 12 = 3.

So, the down counter has value of '3'.

So, finally the upcounter has the value of '0111' and down counter contains the value of '0011'.

3. What is the Frequency of B_0 with respect to CLK (1MHz)?

Given, clock Frequency = 1MHz

For LSB : (B_0) = F/2

= 1MHz / 2

= 0.5 MHz.

B_0 = 0.5 MHz