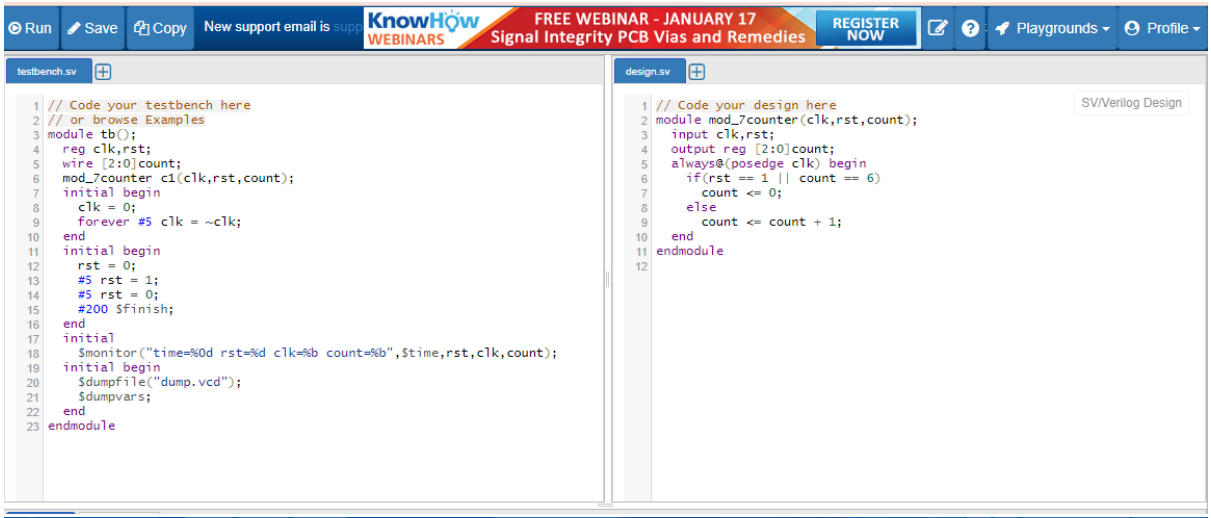
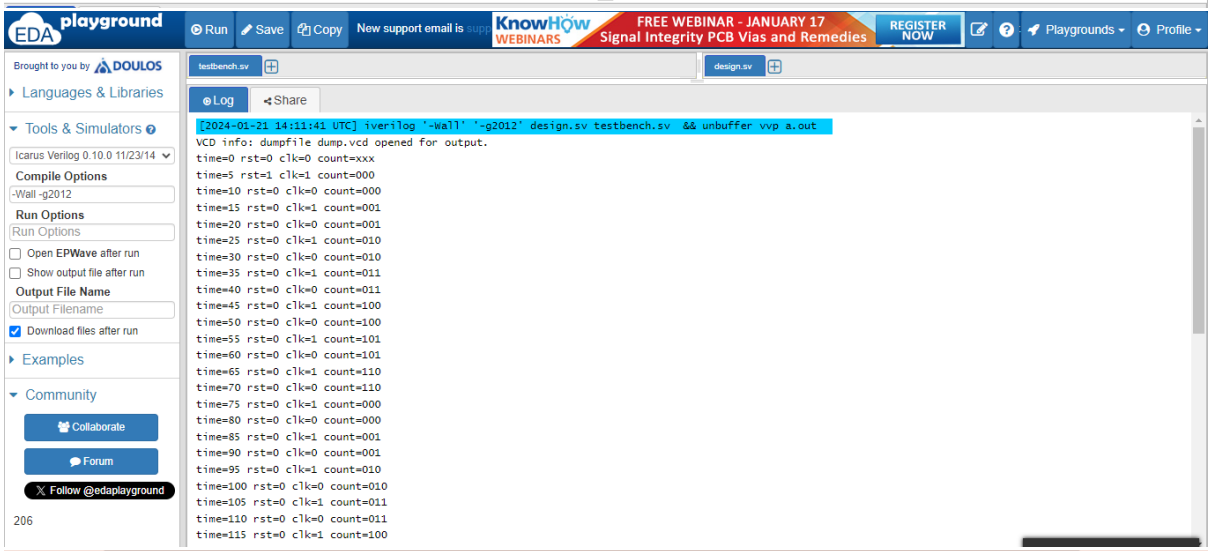
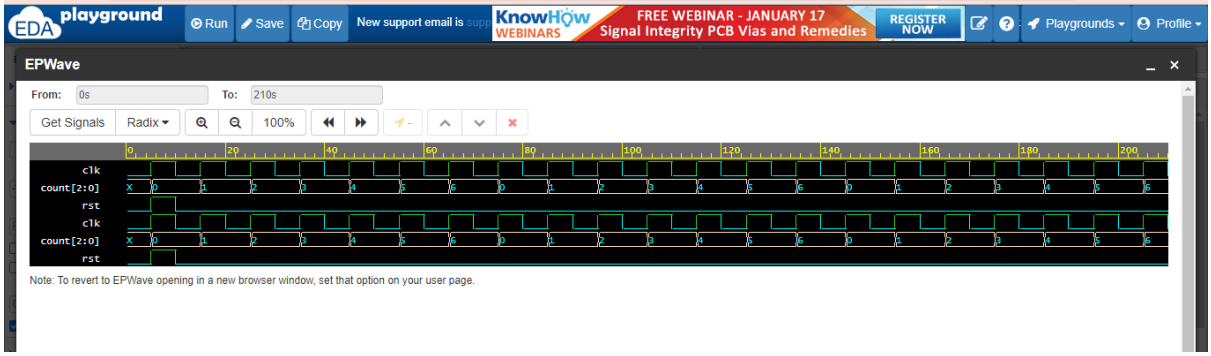

Run
Save
Copy
New support email is
KnowHOW WEBINARS
FREE WEBINAR - JANUARY 17
Signal Integrity PCB Vias and Remedies
REGISTER NOW
Playgrounds
Profile
testbench.sv
// Code your testbench here
// or browse Examples
module tb();
reg clk,rst;
wire [2:0]count;
mod_7counter c1(clk,rst,count);
initial begin
clk = 0;
forever #5 clk = ~clk;
end
initial begin
rst = 0;
#5 rst = 1;
#5 rst = 0;
#200 $finish;
end
initial
$monitor("time=%0d rst=%d clk=%b count=%b",$time,rst,clk,count);
initial begin
$dumpfile("dump.vcd");
$dumpvars;
end
endmodule
design.sv
SV/Verilog Design
// Code your design here
module mod_7counter(clk,rst,count);
input clk,rst;
output reg [2:0]count;
always@(posedge clk) begin
if(rst == 1 || count == 6)
count <= 0;
else
count <= count + 1;
end
endmodule


EDA playground
Run
Save
Copy
New support email is
KnowHOW WEBINARS
FREE WEBINAR - JANUARY 17
Signal Integrity PCB Vias and Remedies
REGISTER NOW
Playgrounds
Profile
Brought to you by DOULOS
Languages & Libraries
Tools & Simulators
Icarus Verilog 0.10.0 11/23/14
Compile Options
-Wall -g2012
Run Options
Run Options
Open EPWave after run
Show output file after run
Output File Name
Output Filename
Download files after run
Examples
Community
Collaborate
Forum
Follow @edaplayground
206
testbench.sv
design.sv
Log
Share
[2024-01-21 14:11:41 UTC] iverilog '-Wall' '-g2012' design.sv testbench.sv && unbuffer vvp a.out
VCD info: dumpfile dump.vcd opened for output.
time=0 rst=0 clk=0 count=xxx
time=5 rst=1 clk=1 count=000
time=10 rst=0 clk=0 count=000
time=15 rst=0 clk=1 count=001
time=20 rst=0 clk=0 count=001
time=25 rst=0 clk=1 count=010
time=30 rst=0 clk=0 count=010
time=35 rst=0 clk=1 count=011
time=40 rst=0 clk=0 count=011
time=45 rst=0 clk=1 count=100
time=50 rst=0 clk=0 count=100
time=55 rst=0 clk=1 count=101
time=60 rst=0 clk=0 count=101
time=65 rst=0 clk=1 count=110
time=70 rst=0 clk=0 count=110
time=75 rst=0 clk=1 count=000
time=80 rst=0 clk=0 count=000
time=85 rst=0 clk=1 count=001
time=90 rst=0 clk=0 count=001
time=95 rst=0 clk=1 count=010
time=100 rst=0 clk=0 count=010
time=105 rst=0 clk=1 count=011
time=110 rst=0 clk=0 count=011
time=115 rst=0 clk=1 count=100


EDA playground
Run
Save
Copy
New support email is
KnowHOW WEBINARS
FREE WEBINAR - JANUARY 17
Signal Integrity PCB Vias and Remedies
REGISTER NOW
Playgrounds
Profile
EPWave
From:
0s
To:
210s
Get Signals
Radix
100%
clk
count[2:0]
rst
clk
count[2:0]
rst
Note: To revert to EPWave opening in a new browser window, set that option on your user page.