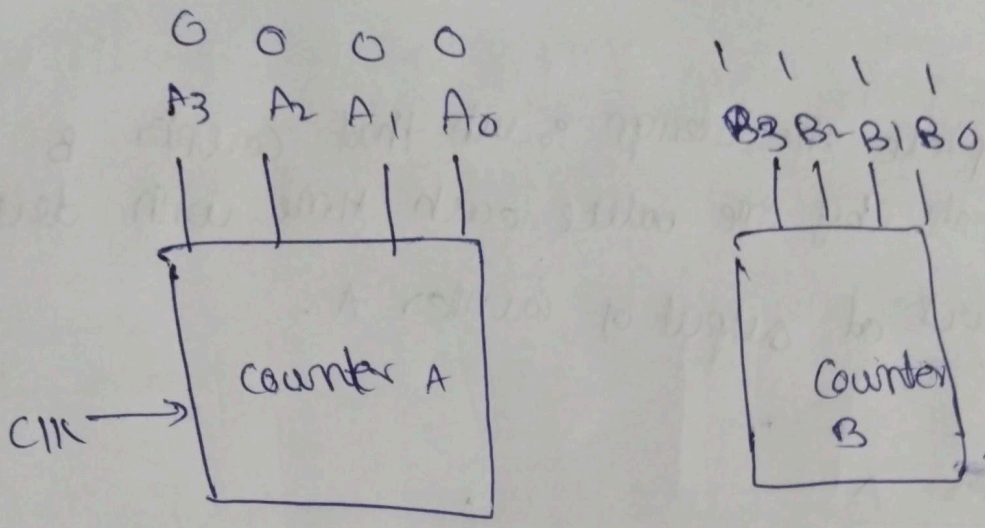
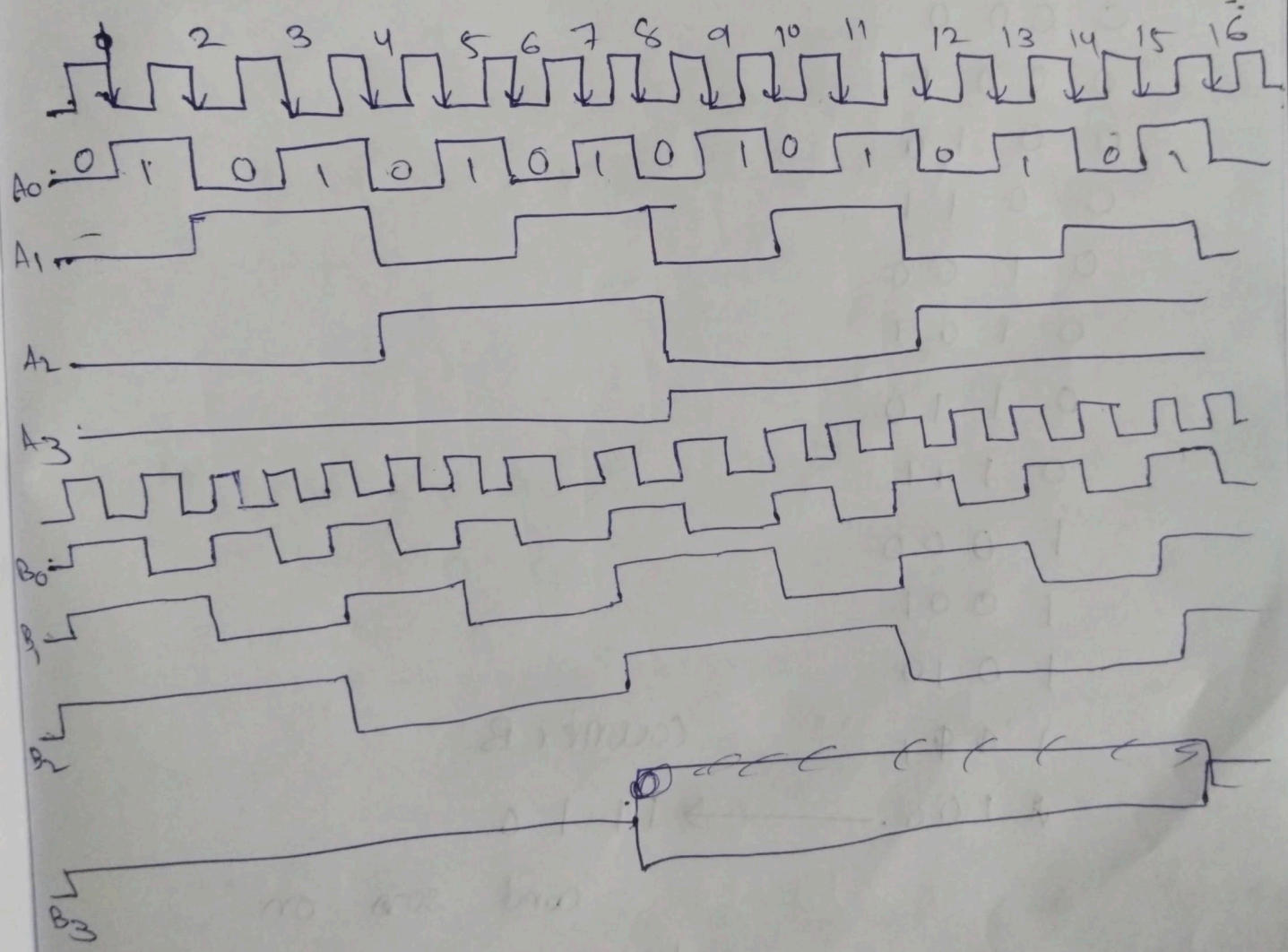




16 clock cycles = to count 16 states

① complete the design such that counter B decrements by one value each time with decimal 12) appears at output of counter A.

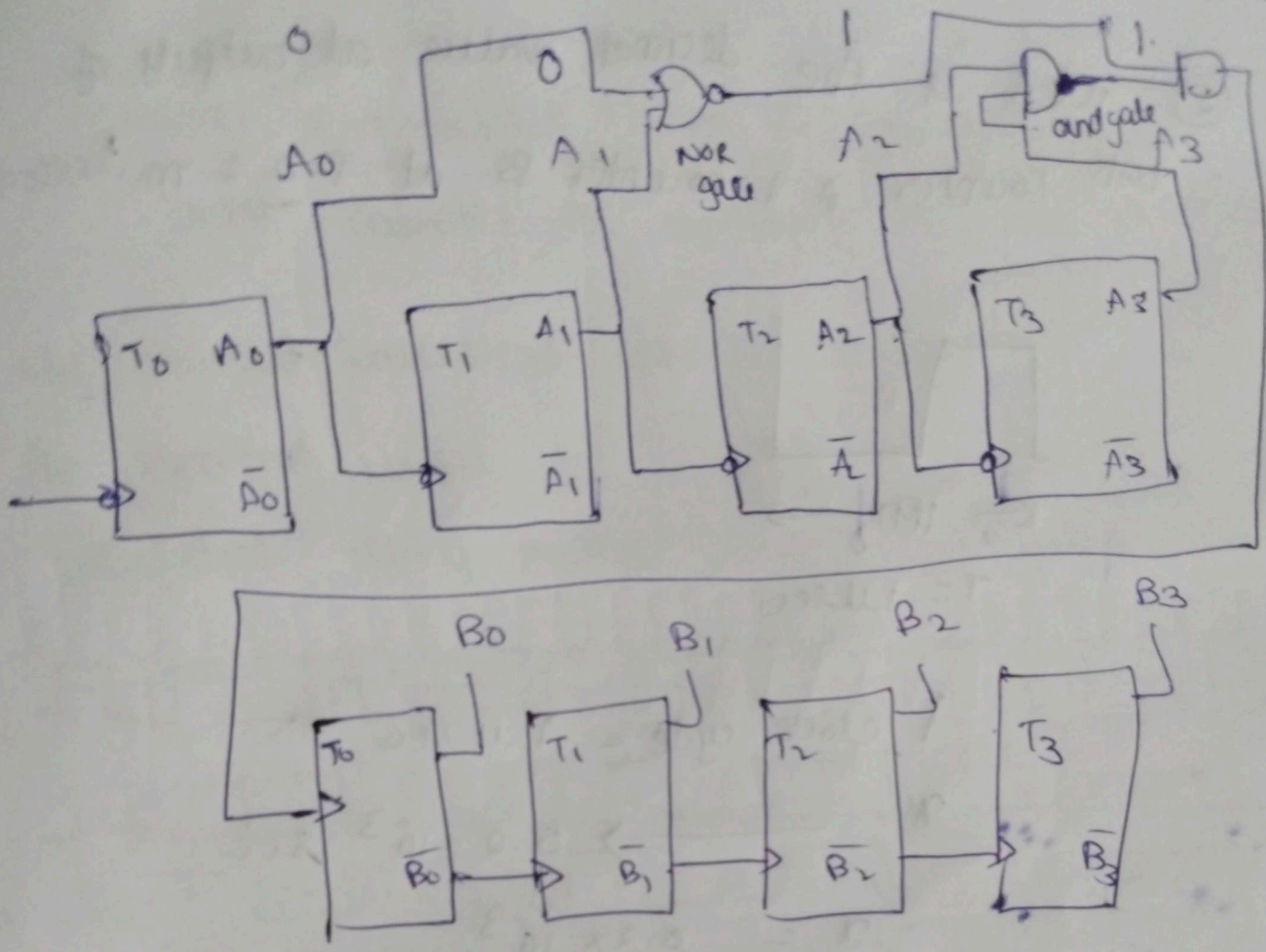
counter A

0 0 0 0
0 0 0 1
0 0 1 0
0 0 1 1
0 1 0 0
0 1 0 1
0 1 1 0
0 1 1 1
1 0 0 0
1 0 0 1
1 0 1 0
1 0 1 1
1 1 0 0 ⟶ 1 1 1 0

counter B

and so on

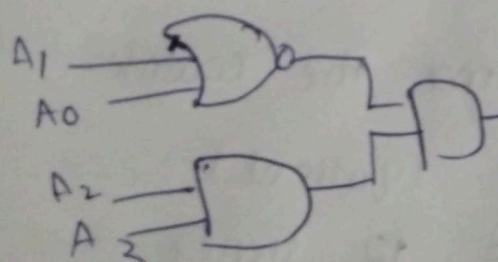
when counter A knocks 1100 (12)
then counter B decrements.



A3	A2	A1	A0
1	1	0	0

counter A → negedge triggered

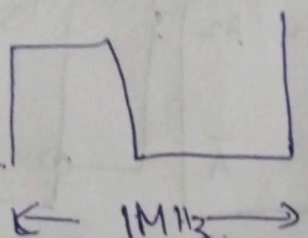
Counter B → posedge triggered.



clk for counter B } combinational logic added

when A0 = 0, A1 = 0, A2 = 1, A3 = 1
then only output = 1

(2) what is the decimal value at outputs of both counter A & counter B at T=0.2 milliseconds



T = 1μsec

1 clock cycle = 1 μ sec

x ⟶ 0.2×10^{-3} sec

$$x = \frac{0.2 \times 10^{-3}}{10^{-6}}$$

$\Rightarrow 0.2 \times 10^{3}$.

= 200 clock cycles.

for complete counter to counter 16 states 16 clock cycles required.

for 200 clock cycles no of times the counter completed all states (quotient)

200/16 = 12 times

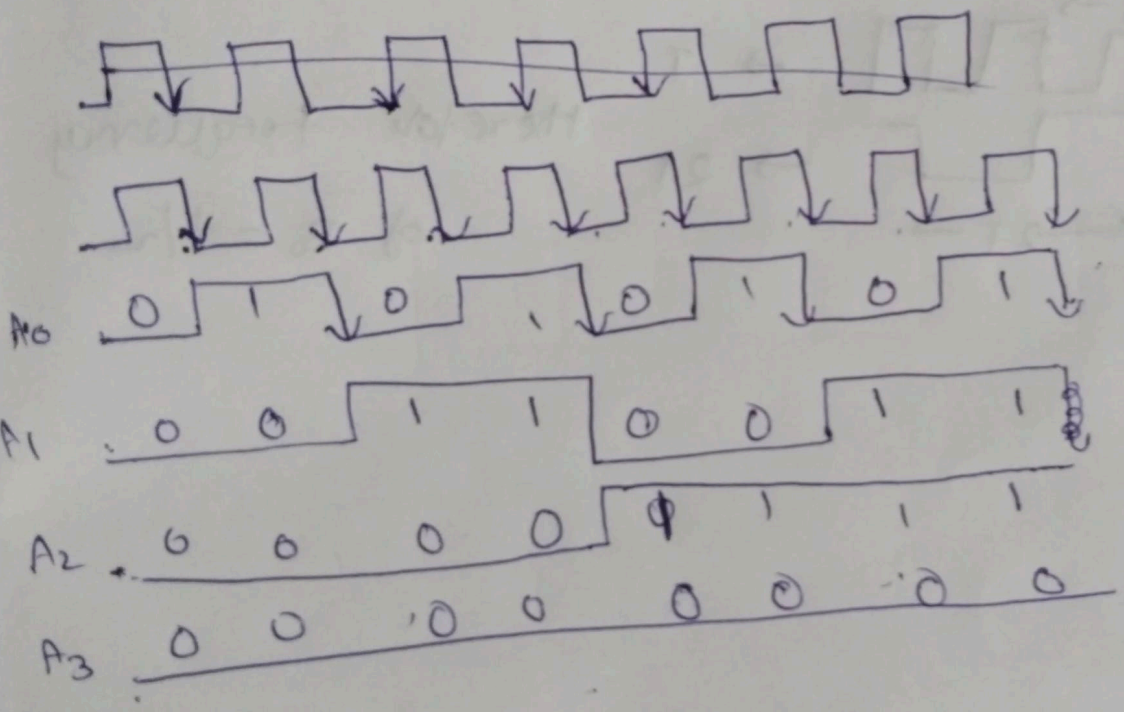
-8 remainder

counter A → counted 0 to 15, 12 times

and counter B decreamented by 12 values

the decimal value at counter B is 3.

the decimal value at counter A is to be calculated using remaing 8 clock cycles



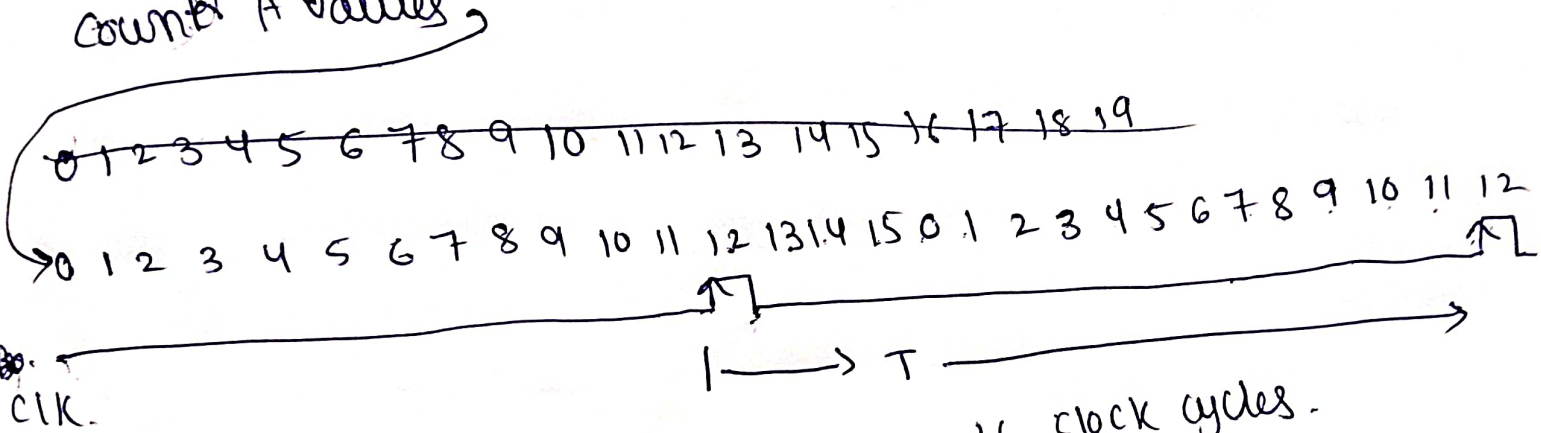
the counter A has 0111 at for 8 clock cycles

A = 0111 = 7

∴ counter A has decimal value 7

and counter B has decimal value 3

③ what is the frequency of B_0 with respect to CLK.



$t = 16 \times 1 \times 10^{-6}$ sec

$f_{CLK} = \frac{1}{16 \times 10^{-6}} = 0.0625$ MHz

$f_{CLK} = 0.0625$ MHz.

$f_{B0} = \frac{0.0625 \text{ MHz}}{2} = 0.03125$ MHz.