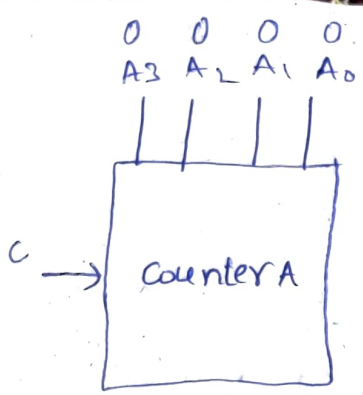
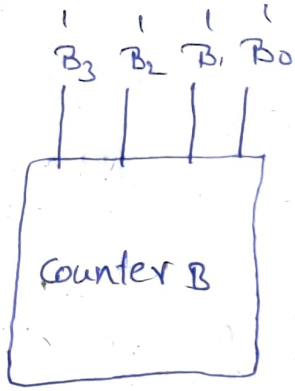
Pb:





⇒ Both Asynchronous

⇒ T=0, 0000
1111

⇒ clock source
1MHz

1) Complete the design such that Counter B decrements by one value each time when decimal "12" appears at output of Counter A.

2) what is the decimal value at outputs of both Counter A & Counter B at T=0.2 milli sec.

3) what is the freq. of B0 with respect to ~~Clk~~ Clk (1MHz) ?

Soln

Here, the inputs are 4 bits (0-15) and Counter A → up counter, Counter B → down Counter

① Counter-A

A3 A2 A1 A0

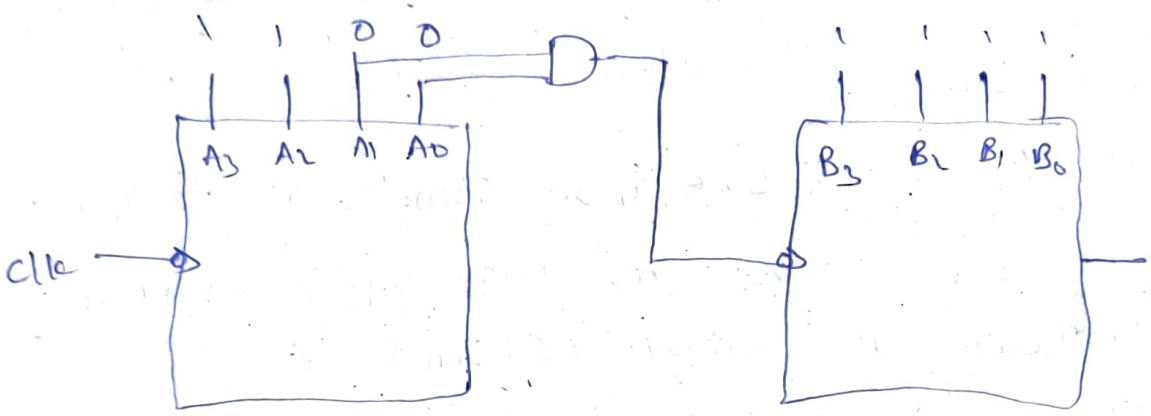
0 0 0 0 → 0
0 0 0 1 → 1
0 0 1 0 → 2
0 0 1 1 → 3
0 1 0 0 → 4
0 1 0 1 → 5
0 1 1 0 → 6
0 1 1 1 → 7
1 0 0 0 → 8
1 0 0 1 → 9
1 0 1 0 → 10
1 0 1 1 → 11
1 1 0 0 → 12

When counter-A reach 12 then Counter B decrements 1.

It means clock of B triggered.

Counter A Counter B

1100 ⟶ 1110



(2) Given,

Freq = 1 MHz

T = 1 μ sec

Pulses = $\frac{0.2 \times 10^{-3}}{1 \times 10^{-6}}$

for T = 0.2 msec
= 0.2×10^{-3}

= 200 Pulses

Decimal value for Counter A

16) 200 (12
16
40
32
8

for 8th clock Pules
(0-7)
decimal value = 7

Decimal value for Counter B

Pulses = 200 - 12

= 188

and change occured at 16 Pulses

$$16)\overline{188}(11$$

16

28

16

12

Decimal Value = 3

(3) After 12 cycles of A, B will be changed then

$$\text{Clock} = \frac{F_{clk}}{12}$$

$$= \frac{1\,MHz}{12}$$

$$\text{Freq. of } B_0 = \frac{\frac{1\times10^6}{12}}{8}$$

$$= \frac{10^6}{96}$$

$$= 10416.66$$

$q_3 \Rightarrow B_3$

$\frac{q_3}{2} \Rightarrow B_2$

$\frac{q_3}{4} \Rightarrow B_1$

$\frac{q_3}{8} \Rightarrow B_0$