

Clock counter

EDA playground

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Languages & Libraries

Tools & Simulators

Icarus Verilog 0.10.0 11/23/14

Compile Options

-Wall -g2012

Run Options

Run Options

☒ Open EPWave after run

☐ Show output file after run

☐ Download files after run

Examples

Community

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203

testbench.v

SV/Verilog Testbench

```
1 module tb();
2   reg clk;
3
4   wire[7:0] count1,count2;
5   clk_counter c1(clk,count1,count2);
6
7   initial
8     clk=0;
9   always begin
10     if(clk)
11       #4 clk=0;
12     else
13       #6 clk=1;
14   end
15   initial
16     #100 $finish;
17   $monitor("time=%0d clk=%b count1=%d count2=%d",
18     $time,clk,count1,count2);
19   initial
20     begin
21       $dumpfile("dump.vcd");
22       $dumpvars(0);
23     end
24 endmodule
```

design.v

clk_counter

```
1 module clk_counter(clk,count1,count2);
2   parameter clock_edge=1;
3   input clk;
4   output reg[7:0] count1,count2;
5   initial begin
6     count1=1'b0;
7     count2=1'b0;
8   end
9
10  if(clock_edge==1) begin
11    always@(posedge clk)
12      begin
13        count1<=count1+1;
14      end
15  end
16  else begin
17    always@(negedge clk)
18      count2<=count2+1;
19  end
20 end
```

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Log

Share

VCD info: dumpfile dump.vcd opened for output.

time=0 clk=0 count1= 0 count2= 0

time=6 clk=1 count1= 1 count2= 0

time=10 clk=0 count1= 1 count2= 0

time=16 clk=1 count1= 2 count2= 0

time=20 clk=0 count1= 2 count2= 0

time=26 clk=1 count1= 3 count2= 0

time=30 clk=0 count1= 3 count2= 0

time=36 clk=1 count1= 4 count2= 0

time=40 clk=0 count1= 4 count2= 0

time=46 clk=1 count1= 5 count2= 0

time=50 clk=0 count1= 5 count2= 0

time=56 clk=1 count1= 6 count2= 0

time=60 clk=0 count1= 6 count2= 0

time=66 clk=1 count1= 7 count2= 0

time=70 clk=0 count1= 7 count2= 0

time=76 clk=1 count1= 8 count2= 0

time=80 clk=0 count1= 8 count2= 0

time=86 clk=1 count1= 9 count2= 0

time=90 clk=0 count1= 9 count2= 0

time=96 clk=1 count1= 10 count2= 0

time=100 clk=0 count1= 10 count2= 0

Finding VCD file...

/dump.vcd

EPWave

From: 0s To: 100s

Get Signals Radix 100%

clk

count1[7:0]

count2[7:0]

clk

count1[7:0]

count2[7:0]

Note: To revert to EPWave opening in a new browser window, set that option on your user page.