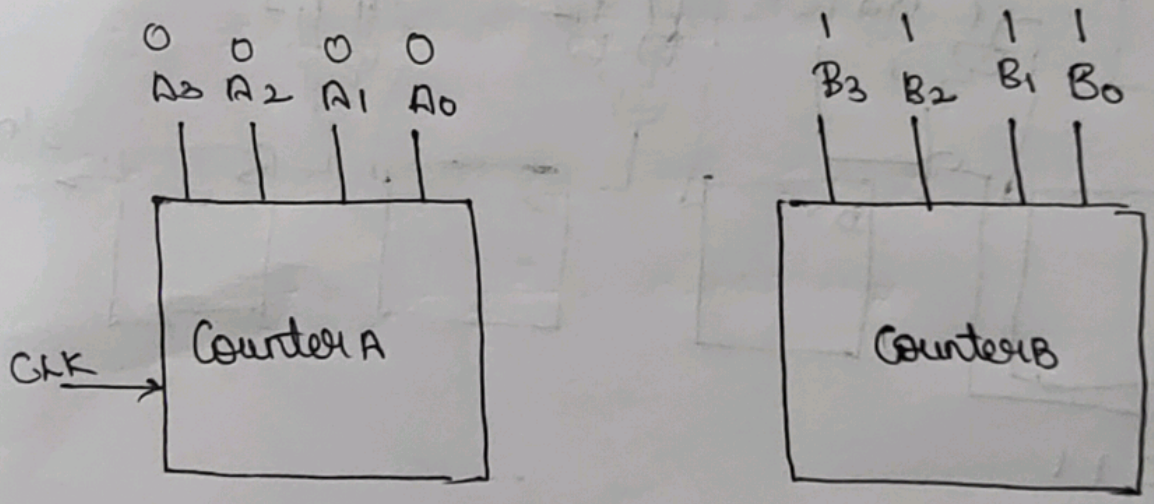
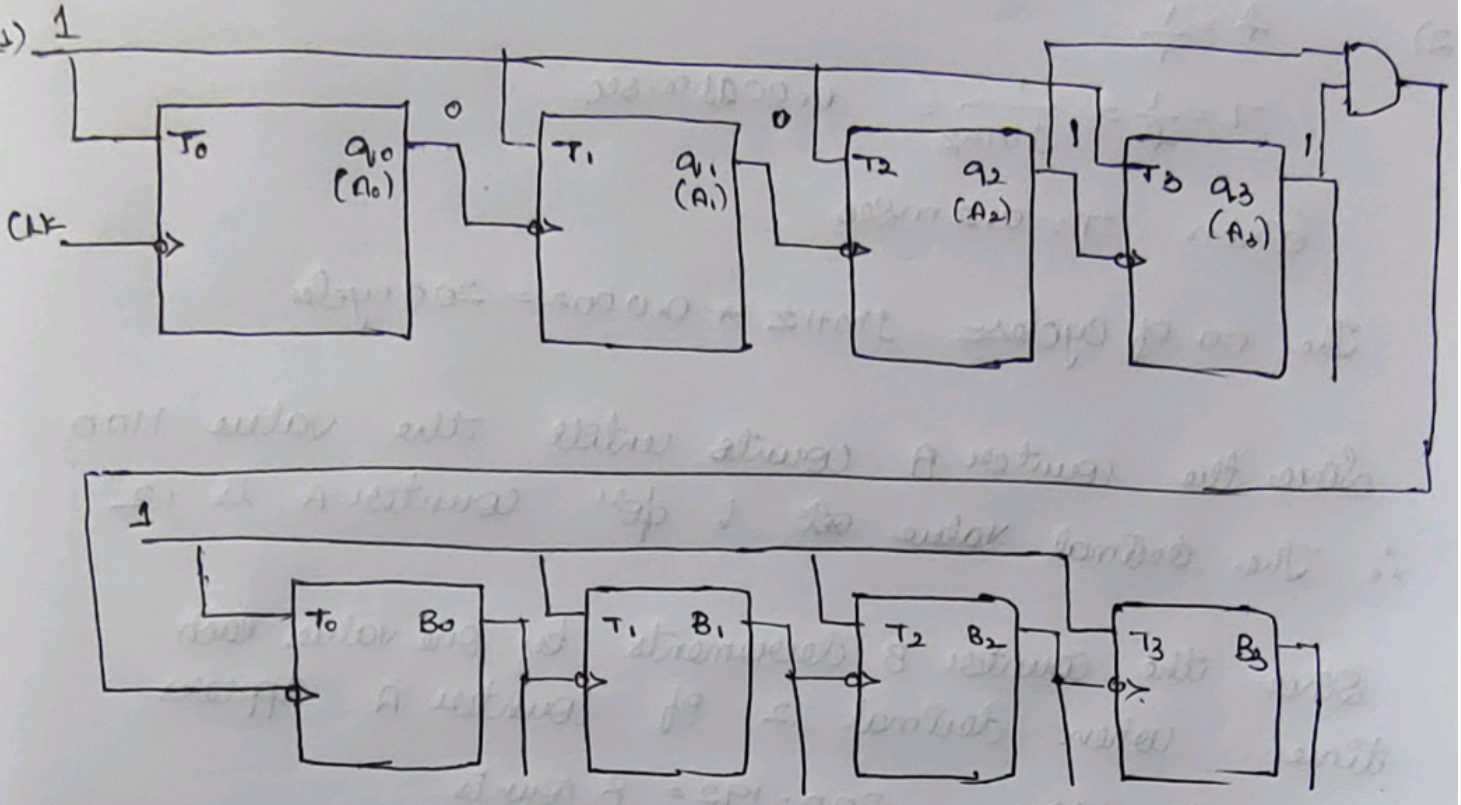
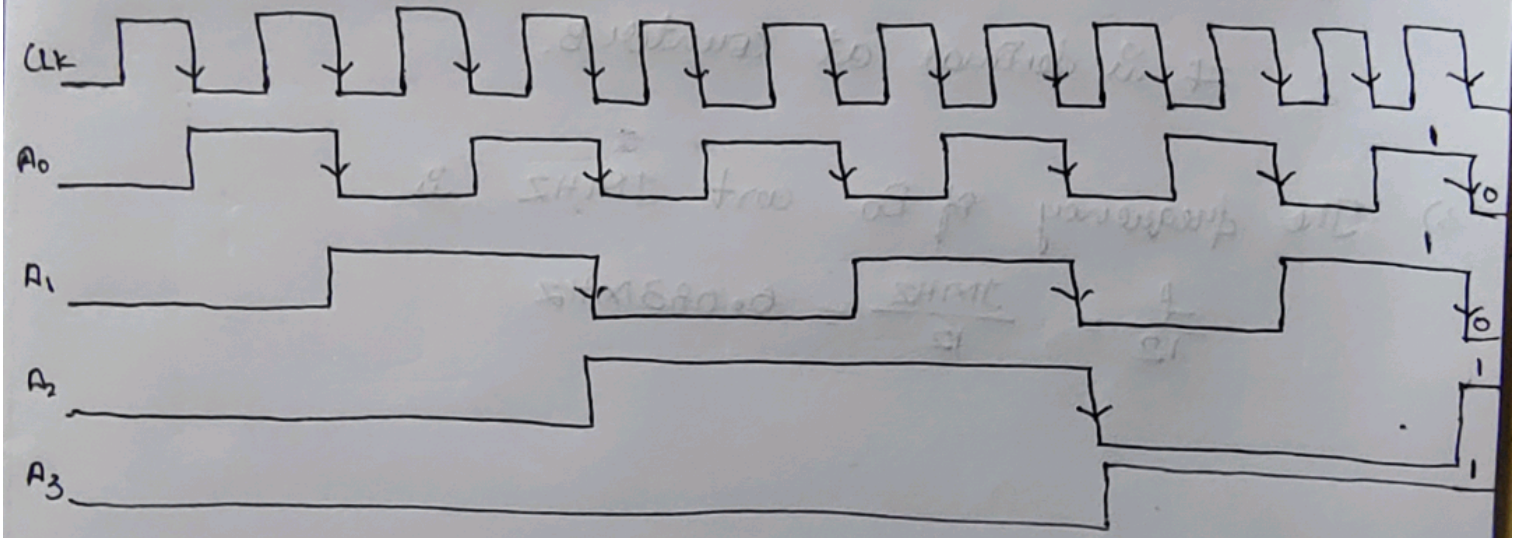
There are 2 counters, "Counter A" being asynchronous up counter and "Counter B" is an asynchronous down Counter and at T = 0, 0000 & 1111 are loaded respectively as shown. Clock source (CLK) available is 1MHZ.

1. Complete the design such that Counter B decrements by one value each time when decimal "12" appears at output of counter A (A_0 being LSB)?
2. what is the decimal value at outputs of both Counter A and counter B at T=0.2 milliseconds?
3. What is the frequency of B_0 with respect to CLK (1MHZ)?



(i)


1
T_0
q_0 (A_0)
T_1
q_1 (A_1)
T_2
q_2 (A_2)
T_3
q_3 (A_3)
CLK
0
0
1
1
1
T_0
B_0
T_1
B_1
T_2
B_2
T_3
B_3


CLK
A_0
A_1
A_2
A_3
1
0
1
0
1
1

2) $f = \frac{1}{T}$

$T = \frac{1}{f} = \frac{1}{1MHz} = 0.0001 msec$

Given $T = 0.2 msec$

The no of cycles = $1MHz * 0.0002 = 200$ cycles

Since the counter A counts until the value 1100
∴ The decimal value 6 for counter A is 12

Since the counter B decrements by one value each time when decimal 12 of counter A appears.

$12 \times 16 = 192$ $200 - 192 = 8$ counts

∴ 7 is decimal at counter B.

3) The frequency of B_0 out 1MHz is

$\frac{f}{024} = \frac{1MHz}{24} = 0.0416 MHz$