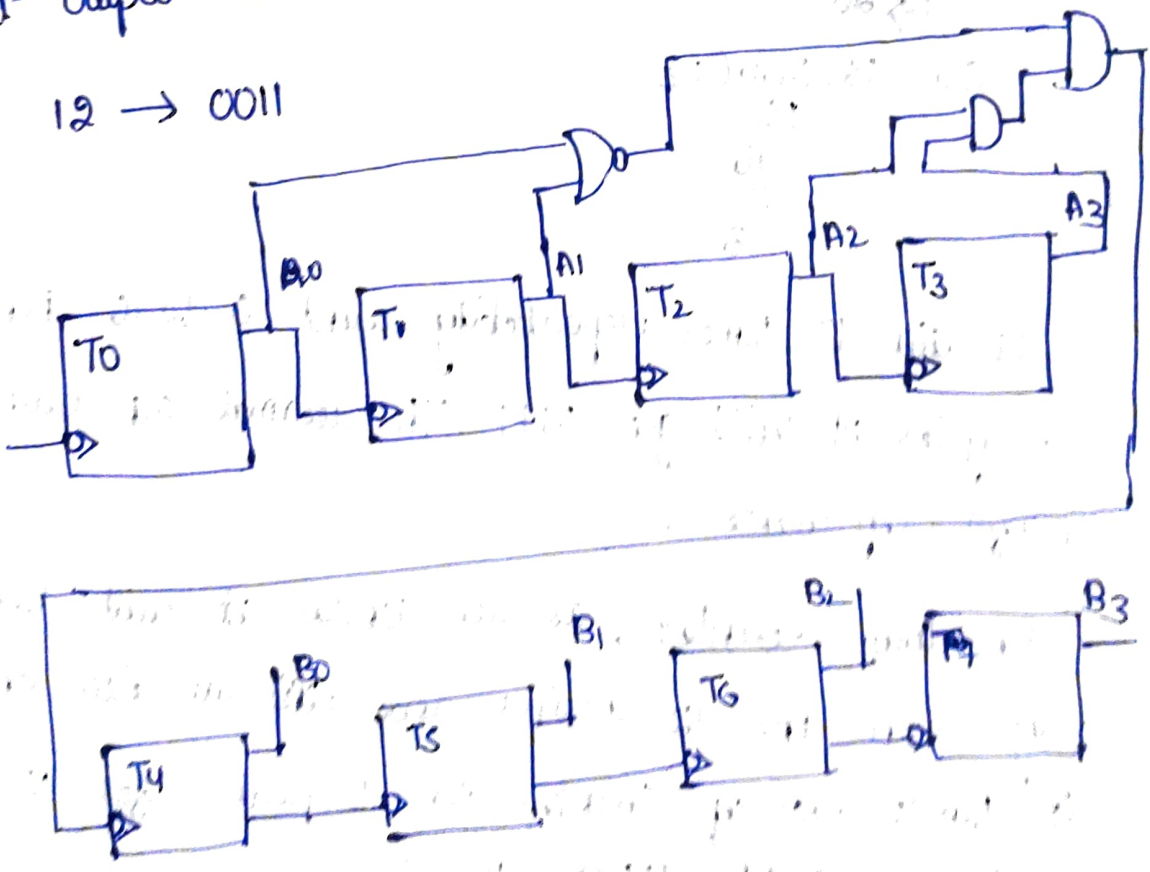
8/12/2023 ASSIGNMENT-7

I. There are two counters "counter A" being asynchronous up counter and counter B is an asynchronous down counter and at T=0, 0000 & 1111 were loaded respectively as shown. Clock source (CLK) available 1 MHz.

a. Complete the design such that counter B decreaments by one value each time when decimal "12" appears at output of counter A.

12 → 0011



b. What is the decimal value at o/p's of both Counter A and Counter B at T = 0.2 mS.

as the given question f = 1 mHz

$$\text{Then } T = \frac{1}{f} = \frac{1}{1m} = 1\times10^{-6}\,S$$

$$\text{NO. of clock cycle} = \frac{T}{\text{Time period of single cycle}} = \frac{0.2\,m}{1\times10^{-6}}$$

$$= 200 \text{ clock cycles}$$

For up counter, it will count ~~osp~~ from 0 to 15

That is 16 state.

~~16)200~~

So 16)200(12

16

40

32

8

It will 12 times repeatebly count 0 to 16. Then for 8 cycles it will get 0111. The decimal o/p will be 7 for up counter.

For down counter, as we know it will decreament only when the 12 arrives and this we also know 12 times ~~one~~ up counter is repeat for 12 times and so, ~~XXXXXXXX~~ 15 - 12 = 3

So, The down counter decimal o/p will be 3.

c. What is the frequency of Bo with respect to clk (1 MHz).

Bo clock frequency = $\frac{\text{CLK frequency}}{\text{Total count range of Bo}}$

$= \frac{1\ MHz}{2}$

$= 0.5\ MHz$