

EDA playground

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FREE WEBINAR - JANUARY 17 Signal Integrity PCB Vias and Remedies

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Languages & Libraries

Tools & Simulators

Icarus Verilog 0.10.0 11/23/14

Compile Options

Run Options

Open EPWave after run

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Examples

Community

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Follow @edaplayground

testbench.v

design.v

```

1 // Code your design here
2 module seq_detector(
3     input x,clk,reset,
4     output reg z
5 );
6
7 parameter S0 = 0 , S1 = 1 , S2 = 2 , S3 = 3 , S4 = 4;
8 reg [3:0] PS,NS ;
9
10 always@(posedge clk or posedge reset)
11 begin
12     if(reset)
13         PS <= S0;
14     else
15         PS <= NS ;
16     end
17
18 always@(PS or x)
19 begin
20     case(PS)
21         S0 : begin
22             z <= 0 ;
23             NS <= x ? S0 : S1 ;
24             $display(PS);
25         end
26         S1 : begin
27             z <= 0 ;
28             NS <= x ? S2 : S1 ;
29             $display(PS);
30         end
31         S2 : begin
32             z <= 0 ;
33             NS <= x ? S3 : S1 ;
34             $display(PS);
35         end
36         S3 : begin
37             z <= 0;
38             NS <= x ? S0 : S4 ;
39             $display(PS);
40         end
41         S4 : begin
42             z <= 1;
43             NS <= x ? S2 : S1 ;
44             $display(PS);
45         end
46         default: NS = S0;
47     endcase
48 end
49
50 always @(PS)
51 begin
52     case(PS)
53         S4: z = 1;
54         default: z = 0;
55     endcase
56 end
57
58 endmodule
59
60

```

Sequence detection0110

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```

1 module mooreoutput;
2
3     reg x;
4     reg clk;
5     reg reset;
6     wire z;
7
8     seq_detector sel (
9         .x(x),
10        .clk(clk),
11        .reset(reset),
12        .z(z)
13    );
14
15    always #5 clk = ~clk;
16
17    initial begin
18        $dumpfile("dump.vcd");
19        $dumpvars(0);
20    end
21
22    initial begin
23        clk = 1'b0;
24        reset = 1'b1;
25        #15 reset = 1'b0;
26
27        #11 x = 0; #10 x = 1; #11 x = 1; #10 x = 0;
28        #11 x = 1; #10 x = 1; #11 x = 0; #10 x = 1;
29        #11 x = 1; #10 x = 0; #11 x = 1; #10 x = 1;
30        #11 x = 0; #10 x = 1; #11 x = 1; #10 x = 0;
31        #10 $finish;
32    end
33    initial
34        $monitor("time=%0d x=%b clk=%b reset=%b z=%b", $time,x,clk,reset,z);
35 endmodule

```

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DOULOS

testbench.sv

design.sv

Log

Share

```

0
time=25 x=x clk=1 reset=0 z=0
0
time=26 x=0 clk=1 reset=0 z=0
time=30 x=0 clk=0 reset=0 z=0
1
time=35 x=0 clk=1 reset=0 z=0
1
time=36 x=1 clk=1 reset=0 z=0
time=40 x=1 clk=0 reset=0 z=0
2
time=45 x=1 clk=1 reset=0 z=0
time=50 x=1 clk=0 reset=0 z=0
3
time=55 x=1 clk=1 reset=0 z=0
3
time=57 x=0 clk=1 reset=0 z=0
time=60 x=0 clk=0 reset=0 z=0
4
time=65 x=0 clk=1 reset=0 z=1
4
time=68 x=1 clk=1 reset=0 z=1
time=70 x=1 clk=0 reset=0 z=1
2
time=75 x=1 clk=1 reset=0 z=0
time=80 x=1 clk=0 reset=0 z=0
3
time=85 x=1 clk=1 reset=0 z=0
3

```

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ompile Options

/all -g2012

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Playgrounds

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EPWave

From: 0s To: 193s

Get Signals Radix Q 100%

clk

reset

x

z

clk

NS[3:0]

PS[3:0]

reset

x

z

Note: To revert to EPWave opening in a new browser window, set that option on your user page.