

## **UNIT-1**

# **DIGITAL LOGIC FAMILIES AND INTERFACING**

**By**  
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# INTRODUCTION

- Logic gates are available in the form of Integrated circuit( IC's)
- As per the level of integration, the IC's can accommodate more number of logic gates and digital functions.
- These forms are referred as logic family



Number of gates fabricated in single IC

There are 4 generation

- Small Scale Integration (SSI) = 12 gates in 1 Chip
- Medium Scale Integration (MSI) = 12 to 100 gates
- Large Scale Integration(LSI)= 100 to 1000 gates
- Very Large Scale Integration(VLSI)= Up to 1,00,000 or more

- The types of digital circuit devices are classified in families that based on the specific circuit technology. Among them, the most important are TTL and CMOS
  - **TTL** (Transistor-Transistor Logic), made of bipolar transistors
    - It is called transistor-transistor logic because the logic function (e.g., AND) and amplification is performed by transistors
  - **CMOS** (Complementary Metal Oxide Semiconductor) made from MOSFET transistors
    - In the modern world, CMOS is the dominate technology used to construct digital circuit components, especially large-scale integrated circuits
- The logic families differ from each other primarily in output current capability, power dissipation, propagation delay time, and operating power supply voltage

# INTRODUCTION TO LOGIC FAMILIES

- The digital integrated circuits are designed using **bipolar devices** or **Metal Oxide Semiconductor (MOS)** or a combination of both.
- There are two kinds of semiconductor devices. The logic family which falls under the first kind **Bipolar logic family** and the other is **Unipolar logic family**.
- There are two kinds of operations in bipolar integrated circuits: **Saturated Bipolar Logic family** and **Non-saturated Bipolar Logic family**.
- Unipolar logic family consists of **Metal Oxide Semiconductor (MOS) logic families**.

# CLASSIFICATION OF LOGIC FAMILIES

- Logic families are mainly classified as Bipolar Logic Families and Unipolar Logic Families.

**Bipolar Logic Families:** It mainly uses bipolar devices like diodes, transistors in addition to passive elements like resistors and capacitors. These are sub classified as saturated bipolar logic family and unsaturated bipolar logic family.

**Saturated Bipolar Logic Family:** In this family the transistors used in ICs are driven into saturation. For example:

1. Transistor-Transistor Logic (TTL)
2. Resistor-Transistor Logic (RTL)
3. Direct Coupled Transistor Logic (DCTL)
4. Diode Transistor Logic (DTL)
5. High Threshold Logic(HTL)
6. Integrated Injection Logic (IIL or I<sub>2</sub>L)

**Unsaturated bipolar logic family:** In this family the transistors used in IC is not driven into saturation. For example:

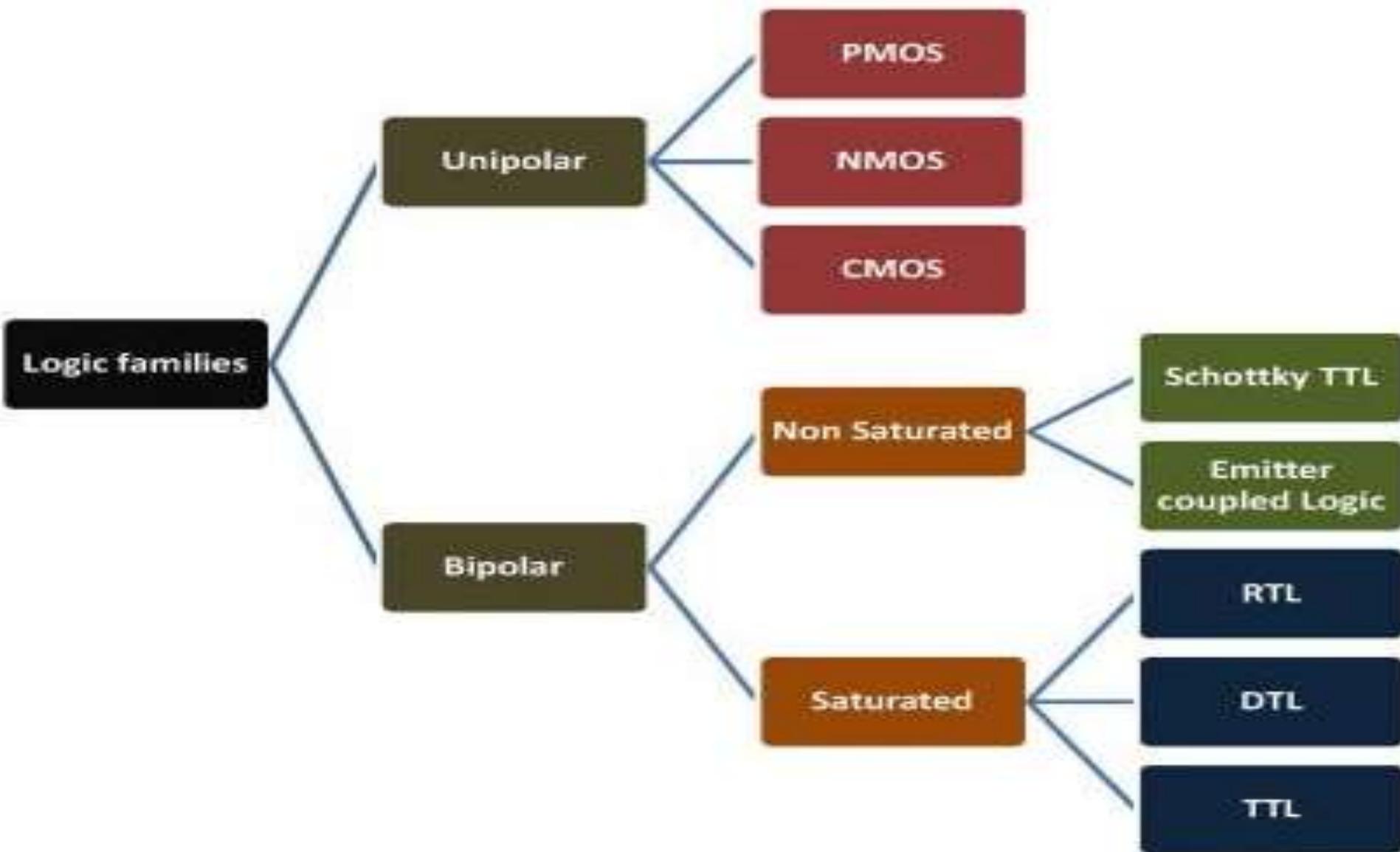
1. Schottky TTL
2. Emitter Coupled Logic(ECL)

**Unipolar Logic Families:** It mainly uses Unipolar devices like MOSFETs in addition to passive elements like resistors and capacitors. These logic families have the advantages of high speed and lower power consumption than Bipolar families. These are classified as:

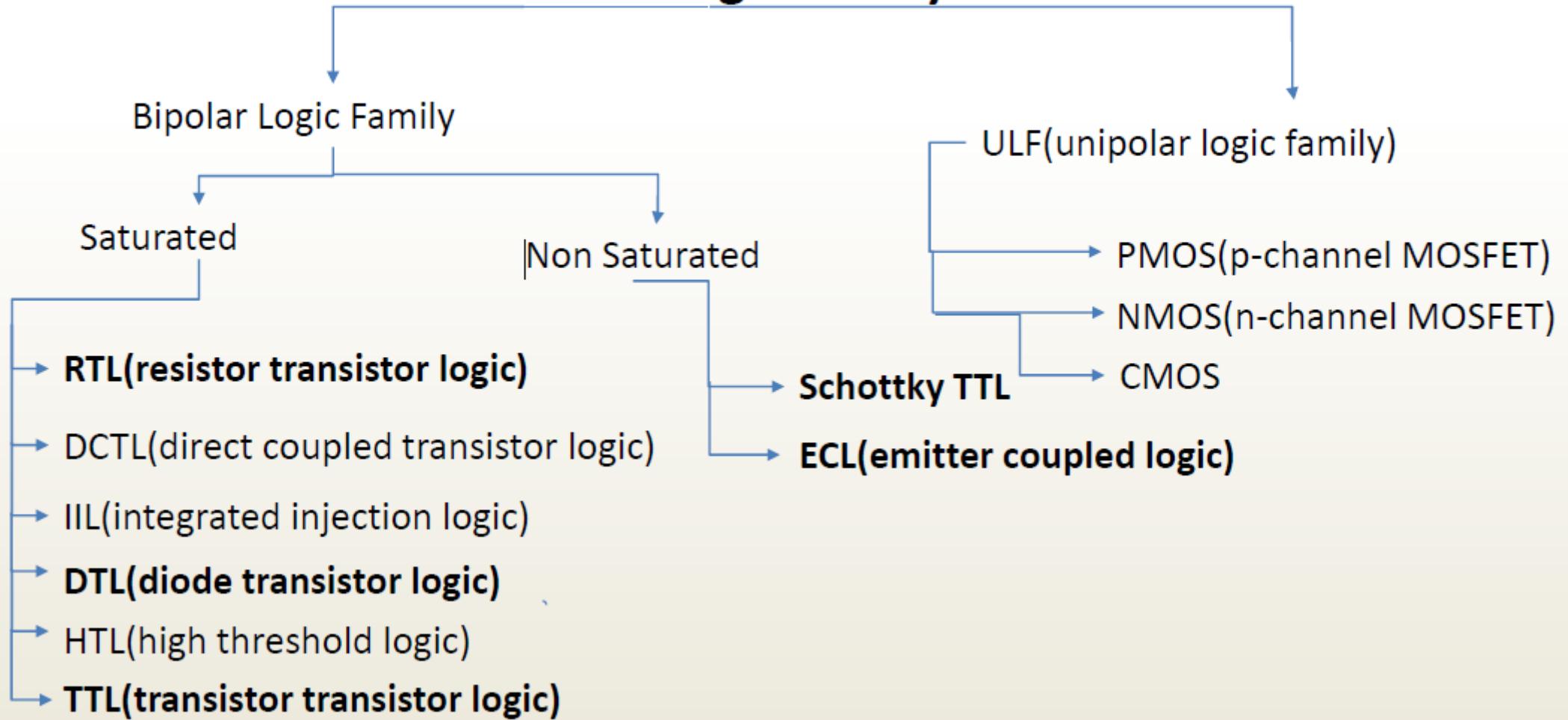
1. PMOS or P-Channel MOS Logic Family.
2. NMOS or N-Channel MOS Logic Family.
3. CMOS Logic Family.

## Classification of logic families

- The digital family is categorized by two types (i)Bipolar and (ii) Unipolar
- In Saturated Bipolar logic families, the transistor in the IC driven in to saturation. In Non Saturated Bipolar logic families, the transistor in the IC not driven in to saturation
- In PMOS & NMOS Unipolar logic family only P & N channel MOSFETs are used. CMOS Unipolar logic family both P& N- channel MOSFETs are used.
- All family same logic level & same Voltage.



# Logic Family



## Characteristics of an Ideal Logic Family

- The ideal logic family should have or be:
  - Low power
  - High speed
  - Easy to use
  - Many different logic functions
  - Clear voltage levels for 0 (LOW) and 1 (HIGH)

# Specifications of Digital IC's

- Different types of ICs are manufactured, based on the components used and their interconnections.
- These ICs are compared using certain performance specifications.

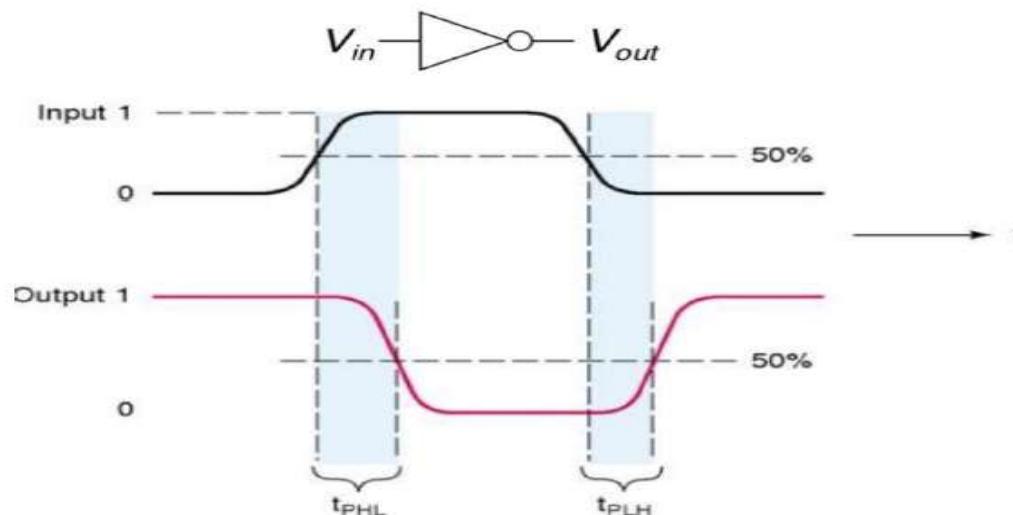
- 1. Power Dissipation**
- 2. Propagation Delay**
- 3. Fan-In**
- 4. Fan-Out**
- 5. Input Logic Level**
- 6. Output Logic Level**
- 7. Compatibility**
- 8. Noise Margin**
- 9. Speed – Power Product**

# 1. Power Dissipation

- This is **the mean power of logic circuit draws from the supply** during one complete cycle.
- This parameter is very important because if the power dissipation is large, then the life period of the IC is reduced.
- It should be noted that in one complete cycle, the IC is in logic '1' for half the time and in logic '0' during the remaining half.
- The power dissipation of a logic gate is equal to the de supply voltage ( $V_{CC}$ ) times the average supply current ( $I_C$ ).

## 2. Propagation Delay

- This parameter characterizes the **speed of a logic circuit**.
- The propagation delay of IC is the mean time required for a pulse to pass through the IC.
- It is thus defined as the time interval between a change in input and the resulting change in the output of an IC.
- It is represented by  $t_p$ .



Average Propagation Delay  
Time  $t_p = \frac{t_{PHL} + t_{PLH}}{2}$

A measure of how long it takes for a gate to change state. Ideally, should be as short as possible.

$t_{PHL}$  - the time it takes the output to go from a high to a low

$t_{PLH}$  - the time it takes the output to go from a low to a high

### 3. FAN-IN

Fan in of a logic circuit gives the **maximum number of inputs** that can be connected to the logic circuit without impairing other primary parameters.

### 4. FAN-OUT

Fan-out of a logic circuit **is the maximum number of outputs** the circuit may have and still operate properly. The fanout is the limiting factor which determines the number of loads that the given data can drive.

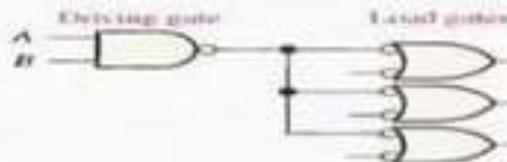
#### Fan in and Fan out

##### Fan-in:

Number of inputs a gate has. For example, a two input gate will have fan-in equal to 2

##### Fan-out:

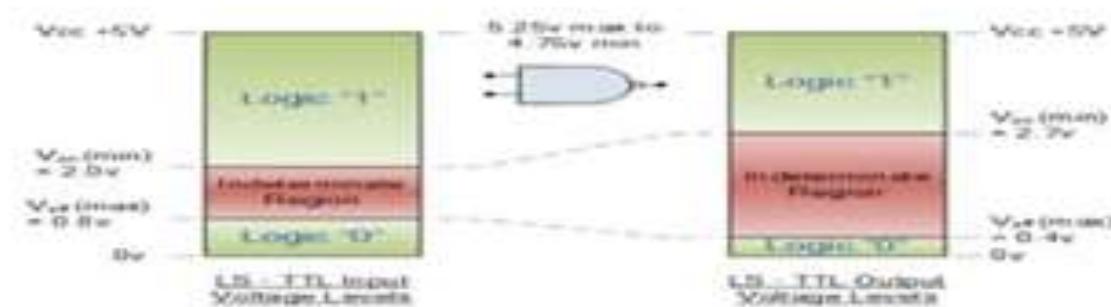
Maximum family to outside



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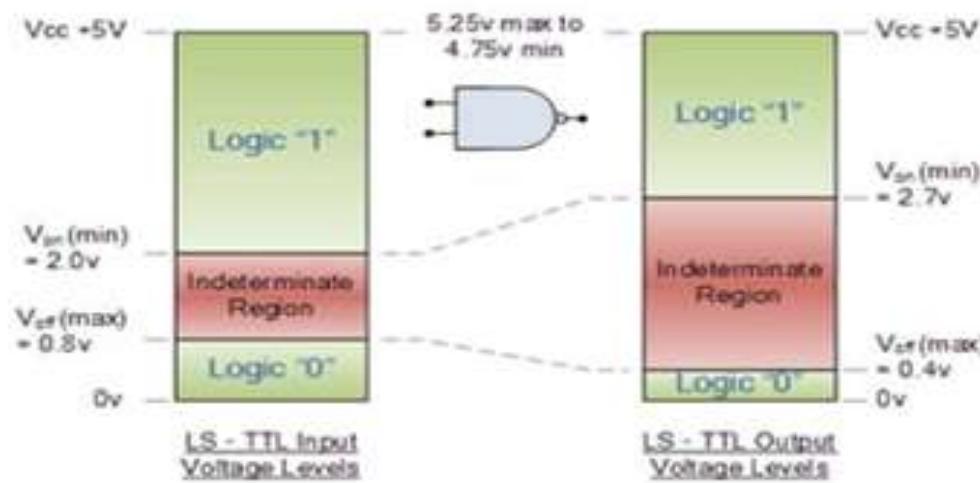
## 5. Input Logic Level ( $V_{IL}$ & $V_{IH}$ )

- If the input voltage level changes without changing the output, this is known as **Input Logic Level**.
- The input is either in logic 0 – low(0V) or logic 1 – High(+5 V)
- some tolerance is allowed to the input voltage.
- Eg: If the input voltage may change from 0V to 0.8V without changing the output level. This voltage of 0.87V is defined as the **Maximum low input voltage ( $V_{IL}$ )**.
- If the logic 1 may change from + 5V to + 2V without affecting, the output level, then the + 2V is known us the **Minimum high level input voltage ( $V_{IH}$ )**.



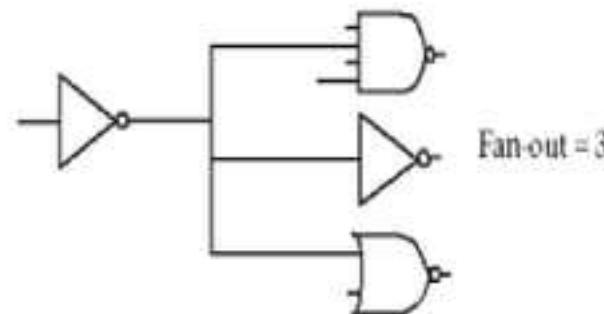
## 6. Output Logic Level

- The output voltage is at 0V for logic 0 and at 5V for logic 1.
- Eg: In supply voltage variations, voltage drop across resistors etc., so these voltages tend to vary. Thus any voltage say, from 0V to 0.4V is considered as low output.
- Similarly any voltage from 2.7V to 5V is considered as logic 1.
- Thus the worst-case output voltages are the **Maximum low level output voltage ( $V_{OL}$ )** and the **Minimum high level output voltages ( $V_{OH}$ )**.



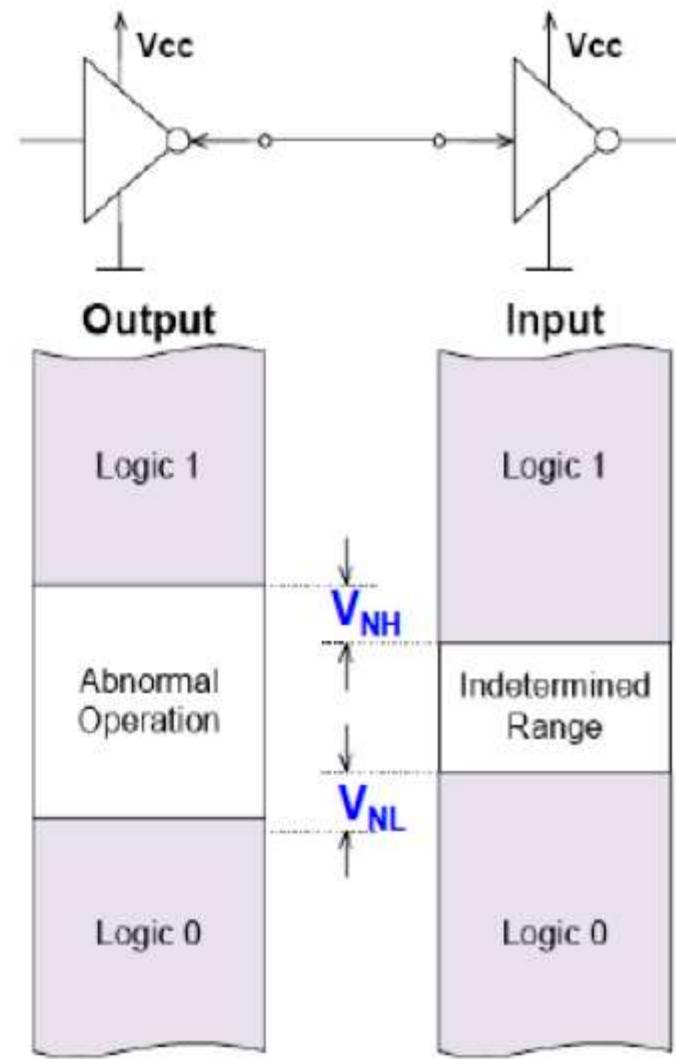
## 7. Compatibility (Ability to work with another)

- Compatibility is defined as the **ability of one device to drive the input of another device**.
- If the output of one device is connected to the input of another device, for both the devices the Input Logic Level and Output Logic Level must be same, then these two devices are compatible .



## 8. Noise Margin

- Noise is present in all real systems. This adds random fluctuations to voltages representing logic levels.
- Hence, the voltage ranges defining the logic levels are more tightly constrained at the output of a gate than at the input.
- Small amounts of noise will not affect the circuit. The maximum noise voltage that can be tolerated by a circuit is termed its **noise immunity (noise Margin)**.



## 9. Speed-Power Product

- It is specified by the manufacturer as a measure of the performance of a logic circuit based on the product of the propagation delay time and the power dissipation at a specified frequency.
- It is expressed in the units of joules (J).

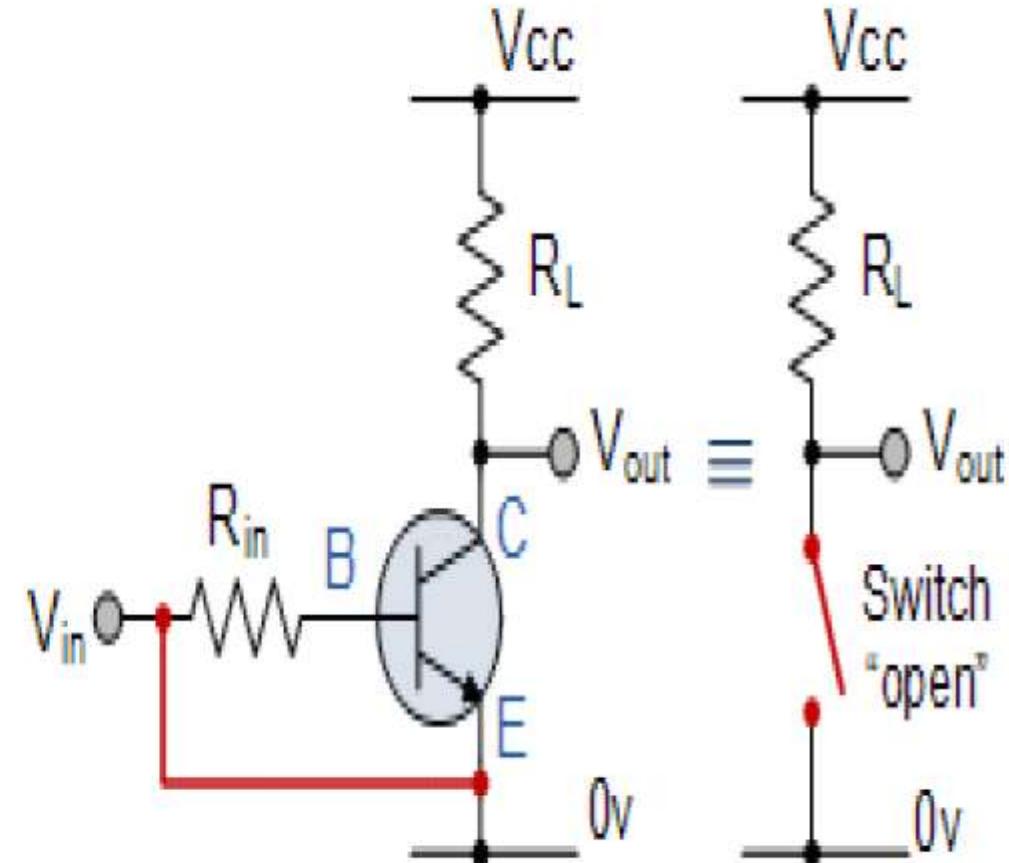
### Speed-Power Product

- Desirable properties:
  - Short propagation delays (high speed)
  - Low power dissipation
- Speed-power product measures the combined effect.



# Transistor as a switch

- A circuit that can turn on/off current in electrical circuit is referred to a switching circuit and transistor can be employed as an electronic switch.
- Cut off region - OFF State  
Both junctions are reverse biased,  
 $I_C = 0$  and  $V(BE) < 0.7$  v
- Saturation region - ON State  
 $I_C = \text{maximum}$  and  $V(BE) > 0.7$  v



# CMOS TECHNOLOGY

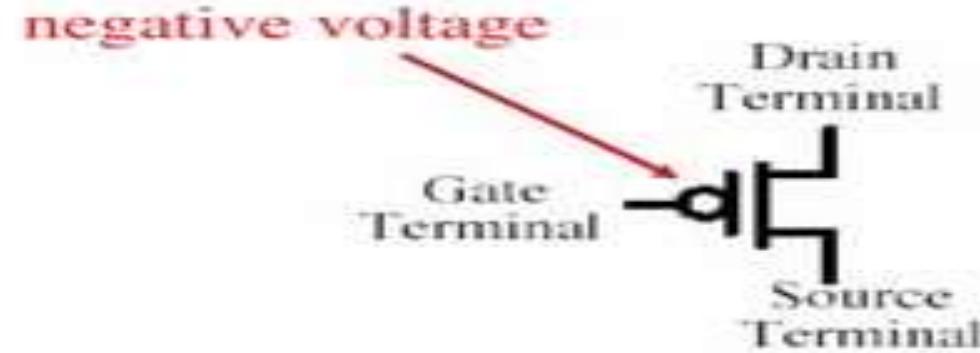
- MOS stands for Metal Oxide Semiconductor
  - Uses FETs
- MOS can be classified into three sub-families:
  - PMOS (P-channel)
  - NMOS (N-channel)
  - CMOS (Complementary MOS, most common)
- The concept of CMOS was introduced in 1963 but become common until the 1980's
- CMOS still dominates digital IC design today
- CMOS technology provides two types of transistors: an n-type transistor(nMOS) and a p-type transistor (pMOS).

# MOSFET Circuit Symbol

- The following simplified symbols are used to represent MOSFET transistors in most CMOS circuit diagrams:



N-Channel  
MOSFET Symbol

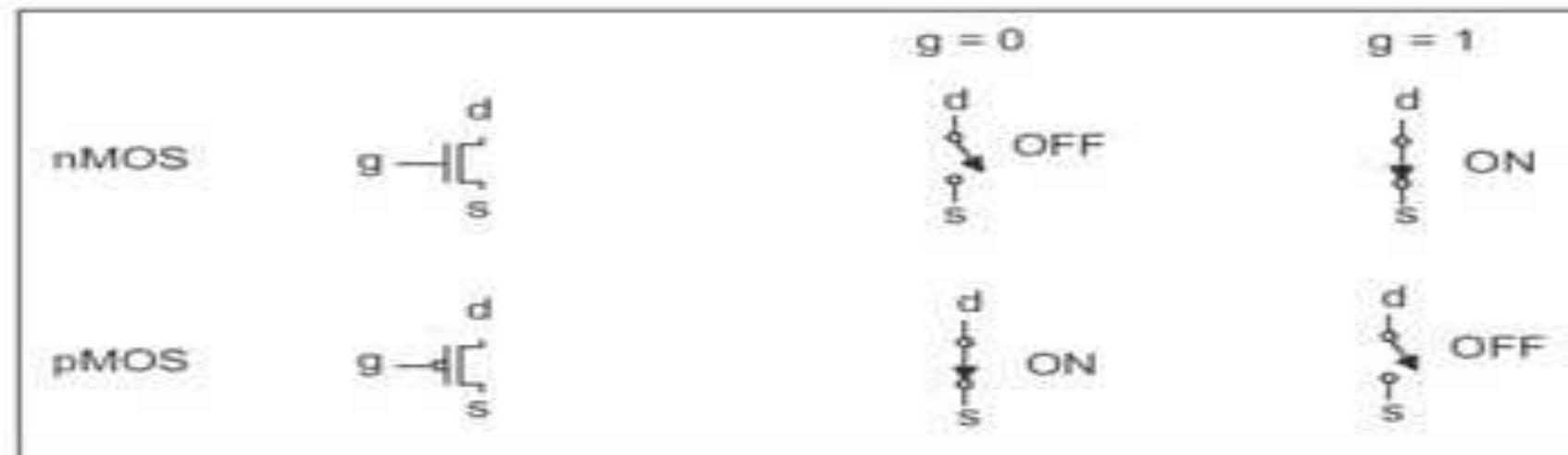


P-Channel  
MOSFET Symbol

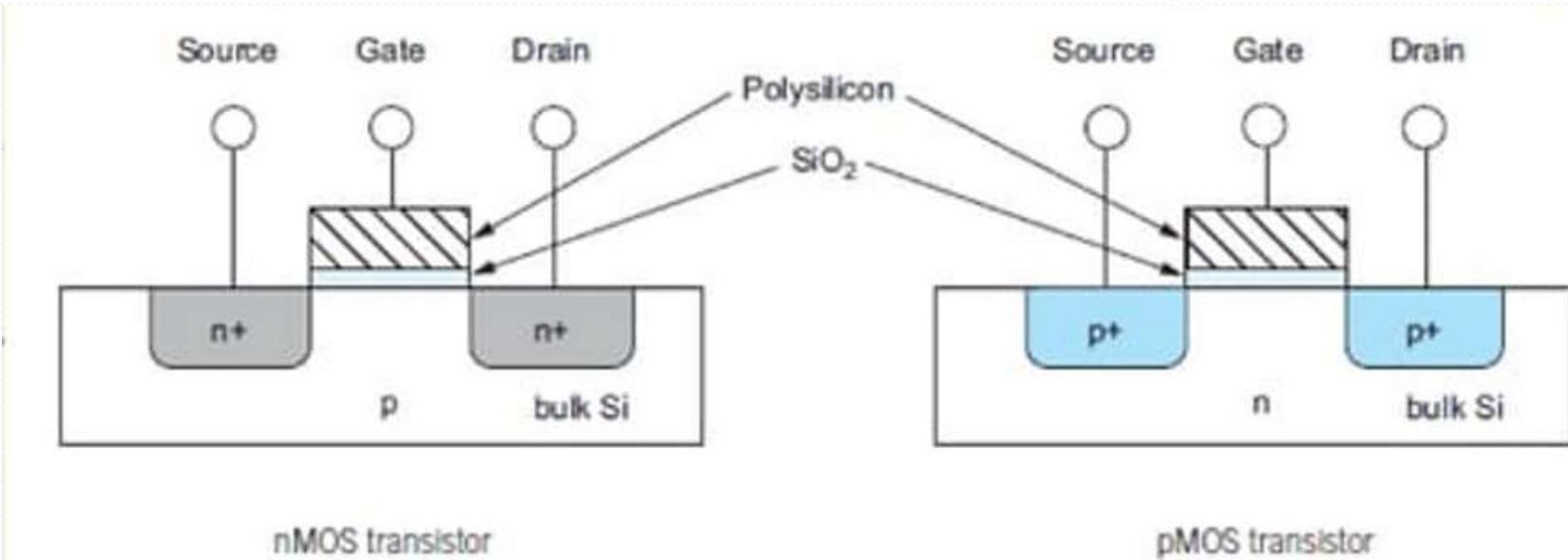
## MOS principle:

The gate is a control input. It effects the flow of electrical current between source and drain

- The gate of a MOS transistor controls the flow of the current between the drain and the source
- The MOS transistor can be viewed as a simple ON/OFF switch

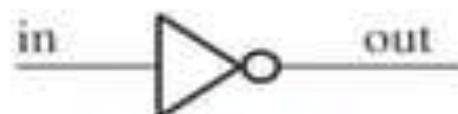


- Each transistor consists of a stack of conducting gate, an insulating layer of silicon dioxide( $\text{SiO}_2$ ) and the silicon wafer, also called the substrate .
- An nMOS transistor is built with a p-type body and has regions of n-type semiconductor adjacent to the gate called the source and drain.
- A pMOS consists of p-type source and drain regions with an n-type body.
- In a CMOS technology, with both flavors of transistors, the substrate is either n-type or p-type.



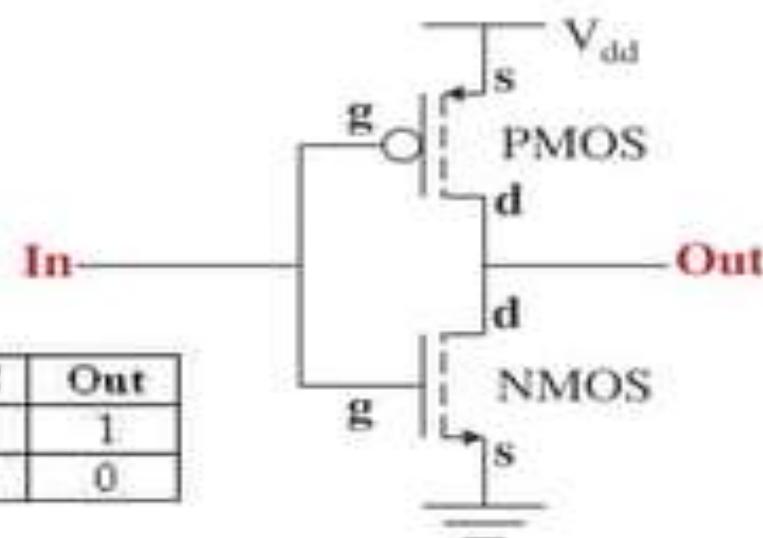
# CMOS INVERTER

- CMOS gates are built around the technology of the basic CMOS inverter
  - Transistors come in complementary pairs
- Two Transistors are enhancement mode MOSFETs
  - N-Channel with its source grounded
  - P-Channel with its source connected to +V
- Input: gates connected together
- Output: drains connected



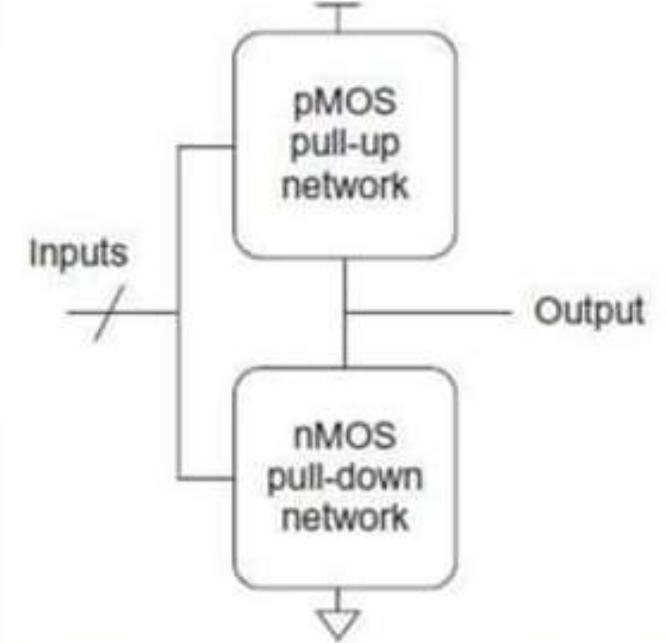
Symbol

In	PMOS	NMOS	Out
0	ON	OFF	1
1	OFF	ON	0



# CMOS LOGIC STRUCTURE

- In general, a static CMOS gate has
  - an nMOS *pull-down network* to connect the output to 0 (GND) and
  - pMOS *pull-up network* to connect the output to 1 (VDD)
- In general, when we join a pull-up network to a pull-down network to form a logic gate, they both will attempt to exert a logic level at the output.
- *The networks are arranged such that one is ON and the other OFF for any input pattern.*



# CMOS NAND

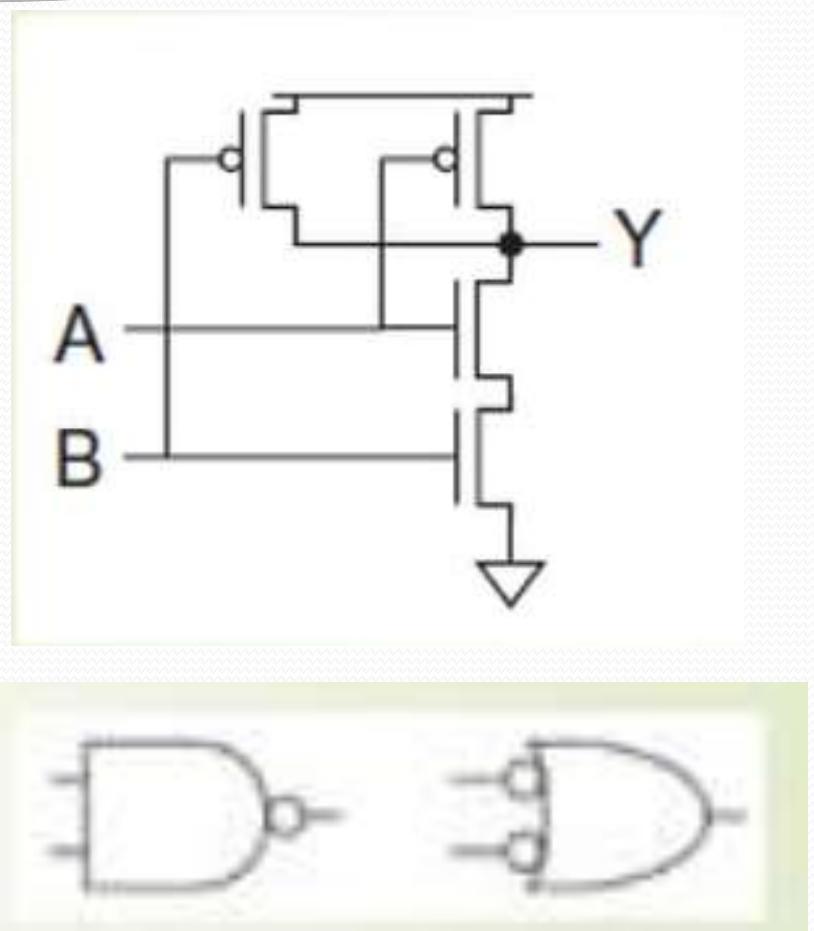
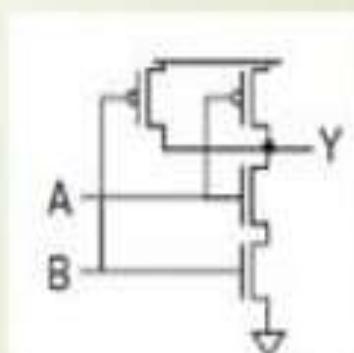
It consists of two series nMOS transistors between Y and GND and two parallel pMOS transistors between Y and VDD.

If either input A or B is 0:

- At least one of the nMOS transistors will be OFF, breaking the path from Y to GND.
- But at least one of the pMOS transistors will be ON, creating a path from Y to VDD.
- Hence, the output Y will be 1.

If both inputs are 1,

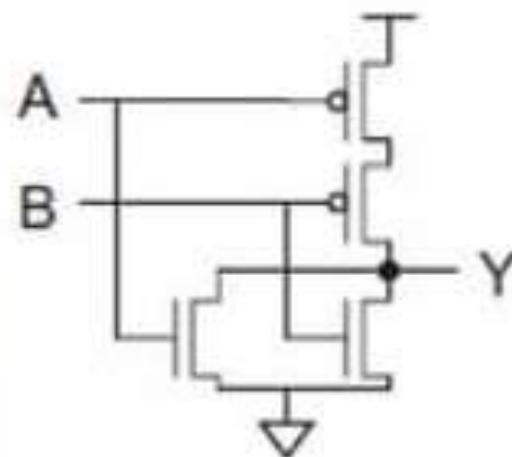
- both of the nMOS transistors will be ON and
- both of the pMOS transistors will be OFF.
- Hence, the output will be 0.



A	B	Pull-Down Network	Pull-Up Network	Y
0	0	OFF	ON	1
0	1	OFF	ON	1
1	0	OFF	ON	1
1	1	ON	OFF	0

# CMOS NOR Gate

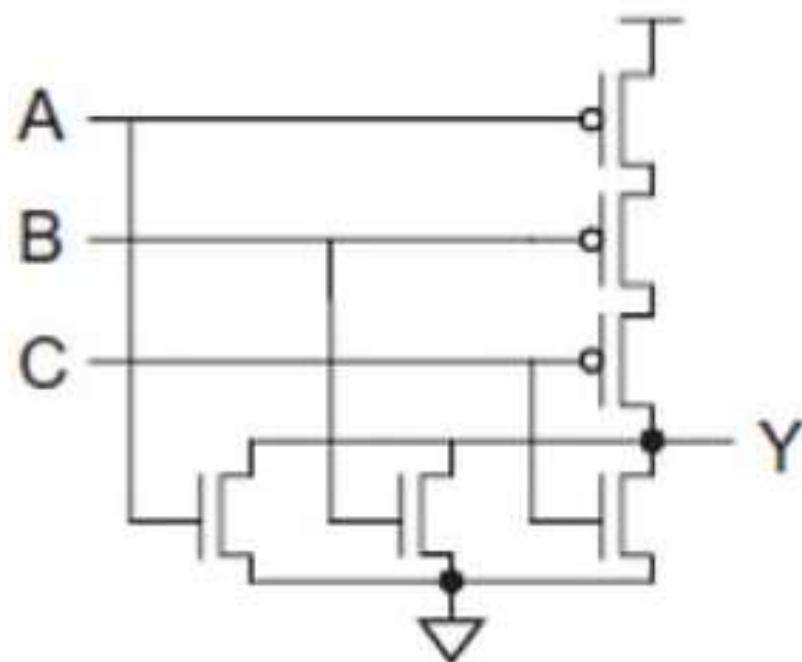
- ▶ The nMOS transistors are in parallel to pull the output low when either input is high.
- ▶ The pMOS transistors are in series to pull the output high when both inputs are low



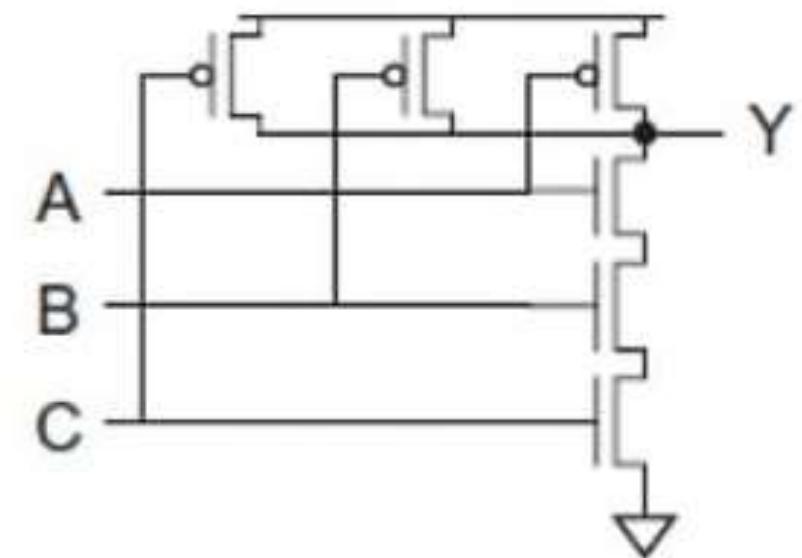
NOR gate truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

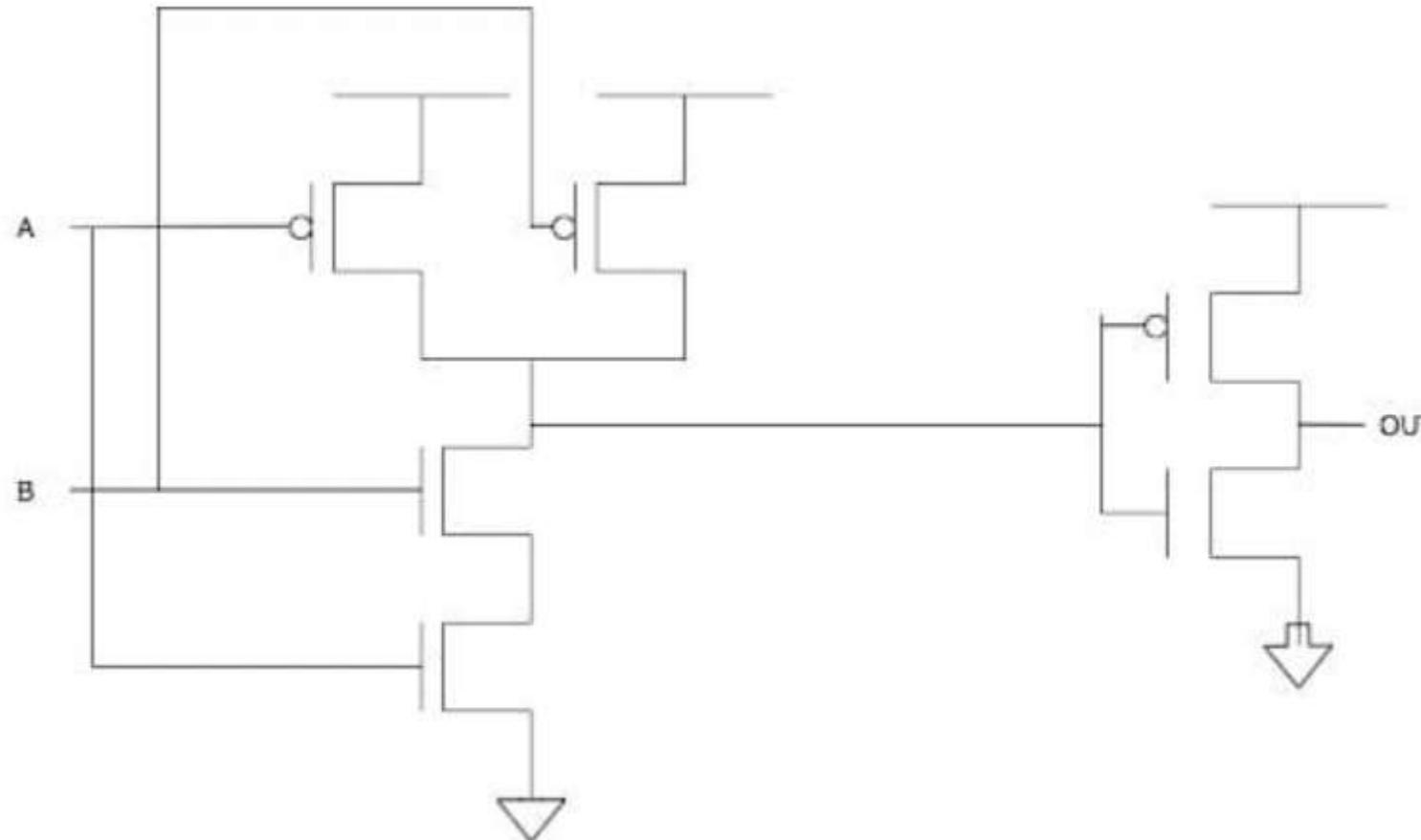
## 3 Input NOR Gate:



## 3 Input NAND Gate:

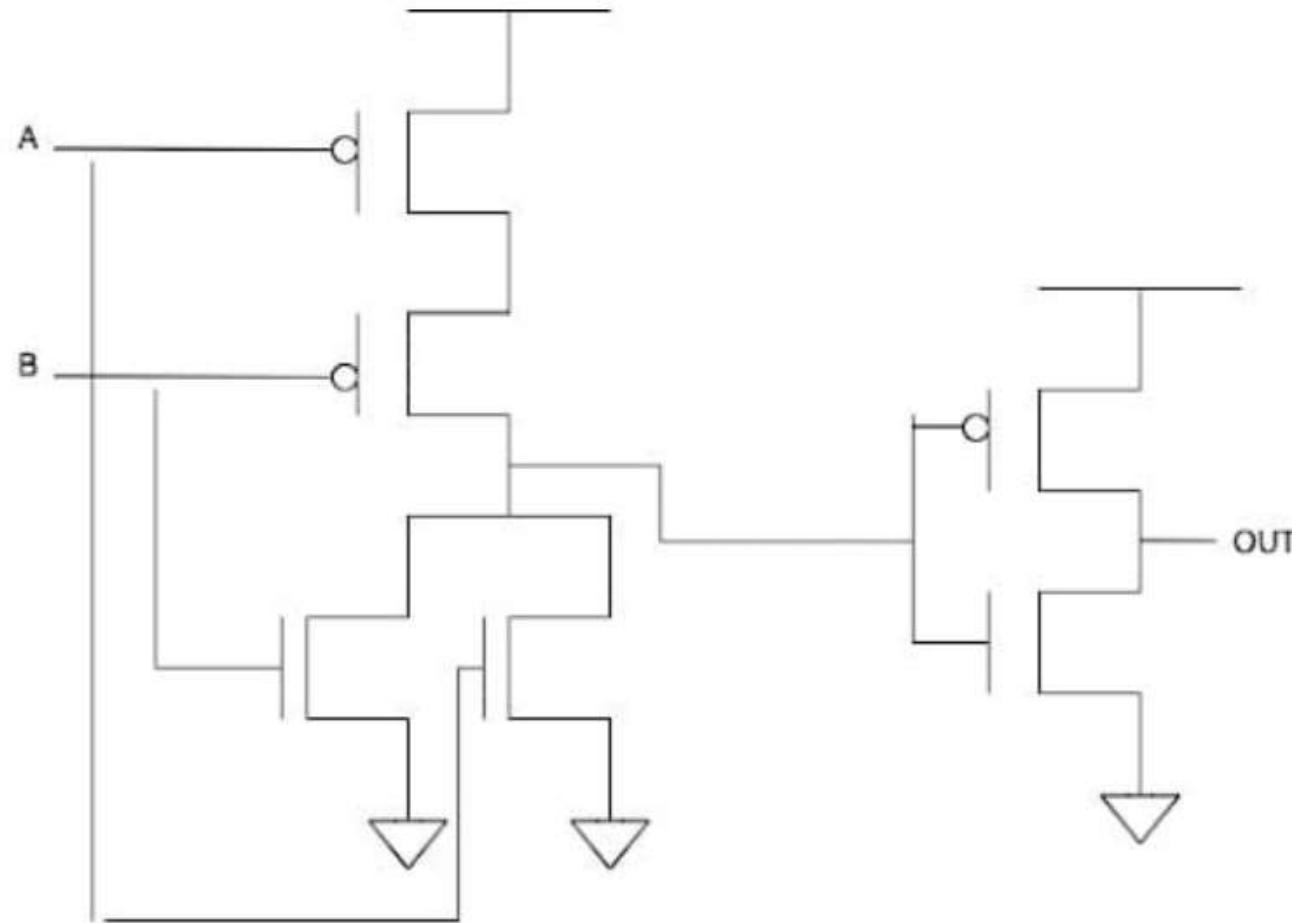


# CMOS AND GATE



A	B	AND	NAND
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

# CMOS OR GATE



A	B	NOR	OR
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

# CMOS Logic Families

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- CMOS Logic Families
  - 40xx/45xx      Metal-gate CMOS
  - 74C              TTL-compatible CMOS
  - 74HC             High speed CMOS
  - 74ACT           Advanced CMOS -TTL compatible
- **Remark:** DO NOT leave CMOS inputs floating!
  - Unused CMOS inputs must be tied to a fixed voltage level (or to another input)

# Pros and Cons of MOS Digital ICs

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- The Good:
  - Simple
  - Inexpensive to fabricate
  - Higher integration
  - Consumes little power
- The bad:
  - Static-electricity damage
  - Slower than TTL

# **Electrical behavior of the CMOS:**

The electrical behavior of CMOS circuits includes the

- 1. Steady state electrical behavior**
- 2. Dynamic electrical behavior**

**1. Steady state electrical behavior:** It is the behavior at the circuit when the inputs & outputs are not changing.

## **Logic levels & Noise margin:**

The CMOS device manufacturers specify the four voltage parameters. They are

➤  **$V_{IH(min)}$ : High level input voltage**

It is the minimum voltage level required for logic 1 at an input. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

➤  **$V_{IL(max)}$ : Low level input voltage**

It is the maximum voltage level required for a Logic 0 at an input. Any voltage above this level will not be accepted as a Low by the logic circuit.

➤  **$V_{OH(min)}$ : High level output voltage**

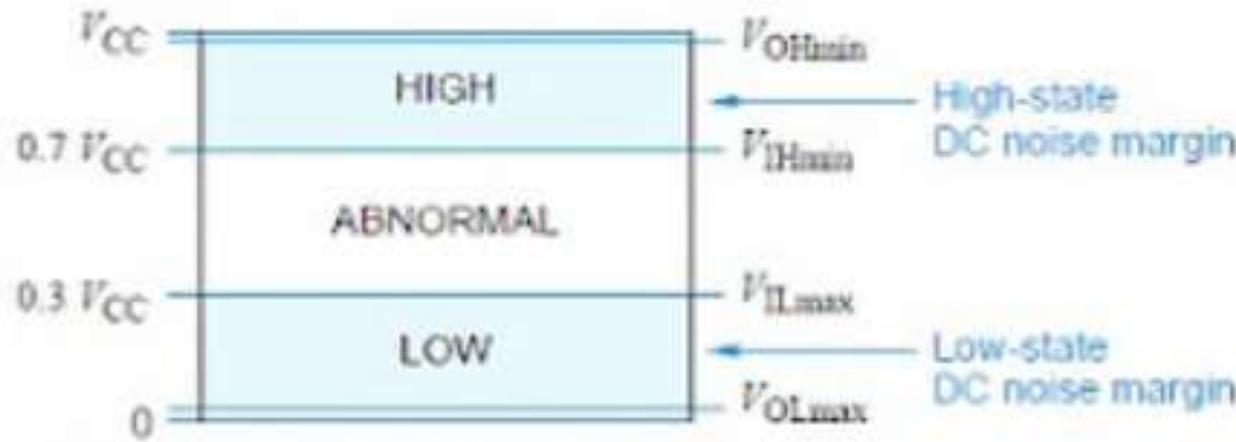
It is the minimum voltage level required for logic 1 at an output under defined load conditions.

➤  **$V_{OL(max)}$ : Low level output voltage**

It is the maximum voltage level required for a Logic 0 at an output under defined load conditions.

In practice, due to the unwanted signal called noise, sometimes the voltage at the input drops below  $V_{IH(min)}$  or rise above  $V_{IL(max)}$ , which produces unpredictable operation.

To avoid this problem due to noise, voltage level  $V_{IH(min)}$  is kept a few fraction of volts below  $V_{OH(min)}$  and  $V_{IL(min)}$  is kept above  $V_{OL(max)}$ , at the design time.



## ➤ Voltage levels & Noise margins:

$V_{OH(min)}$ :  $V_{CC} - 0.1V$  ;  $V_{IH(min)}$ : 70% of  $V_{CC}$

$V_{IL(max)}$  : 30% of  $V_{CC}$  ;  $V_{OL(max)}$  : Ground + 0.1V

- Fan-in: The maximum no. of digital inputs that a single logic gate can accept.
- Fan-out: The maximum no. of digital outputs that the circuit can operate properly.

## **2. CMOS Dynamic electrical behavior:**

- The speed & power consumption of CMOS devices are mostly depends on AC or dynamic characteristics of the device and its load.
- The AC characteristics refers to the output changes between states.

The speed of the CMOS device depends on 2 characteristics:

- 1. Transition time**
- 2. Propagation delay**

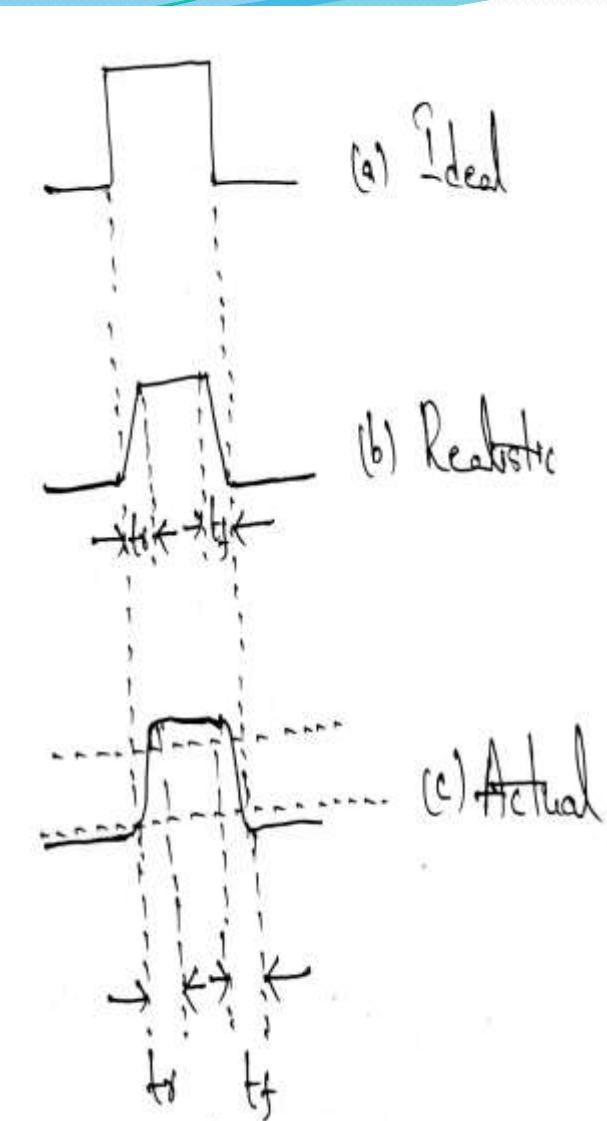
**1. Transition time:** The amount of time that the output at a logic circuit takes to change from one state to another is called the transition time.

In practice outputs cannot change instantaneously, because they need time to change.

Rise time( $t_r$ ): It is the time taken by the output to change from low to high.

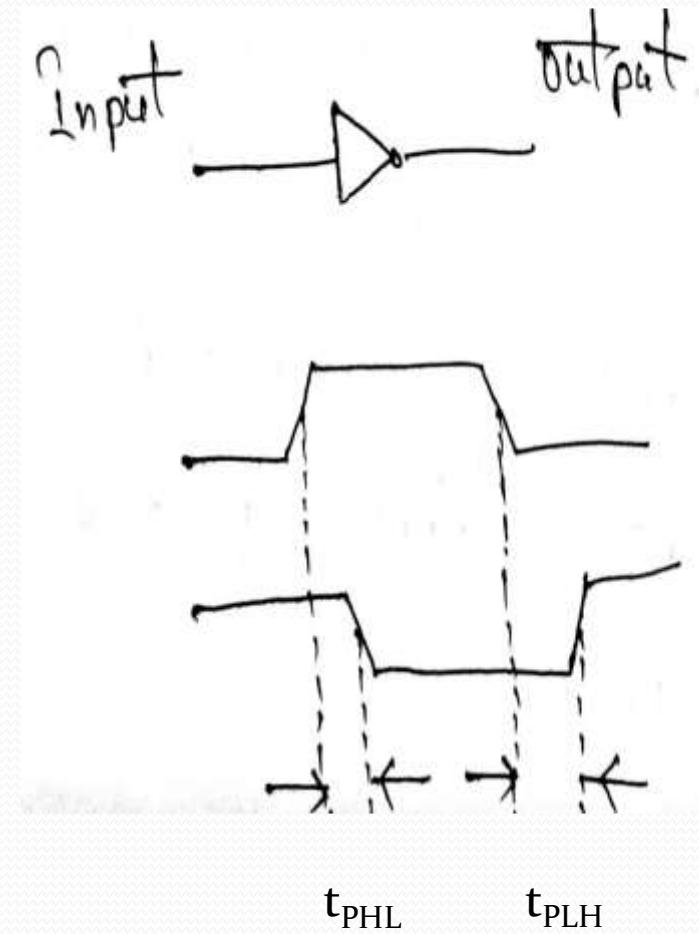
Fall time( $t_f$ ): It is the time taken by the output to change from high to low.

The rise time & fall time of a CMOS output depends mainly on two factors, the ON transistor resistance and the load capacitance. Since increase in load capacitance increases transition time.



## 2. Propagation delay:

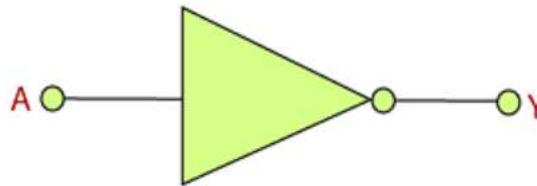
- The propagation delay is the amount of time that it takes for a change in the input signal to produce in the output signal.
- The shorter propagation delay, the higher the speed of the circuit & vice-versa
- The propagation delay is determined using two basic time intervals.
  1.  $t_{PLH}$ : It is the delay time measured when output is changing from logic 0 to logic 1.
  2.  $t_{PHL}$ : It is the delay time measured when output is changing from logic 1 to logic 0.



# **Resistor Transistor Logic (RTL)**

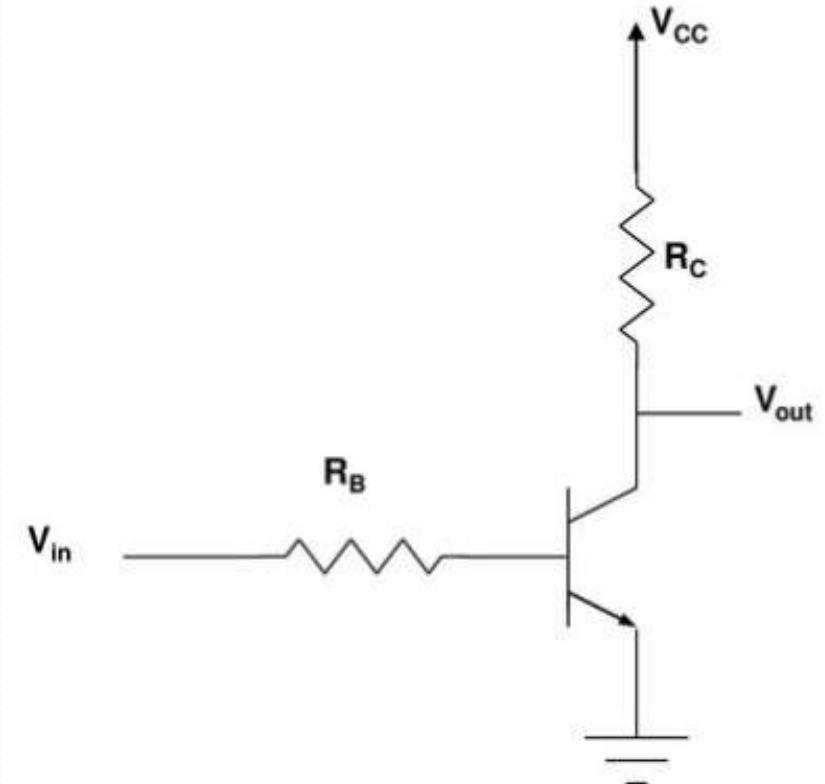
- **Resistor–transistor logic (RTL)** (sometimes also **transistor–resistor logic (TRL)**) is a class of digital circuits built using resistors as the input network and bipolar junction transistors (BJTs) as switching devices.
- RTL is the earliest class of transistorized digital logic circuit; it was succeeded by diode–transistor logic (DTL) and transistor–transistor logic(TTL).
- RTL circuits were first constructed with discrete components but in 1961 it became the first digital logic family to be produced as a monolithic integrated circuit.
- Here Transistors used in Saturation and Cut-off region. So speed of this logic family is low.

# RTL INVERTER



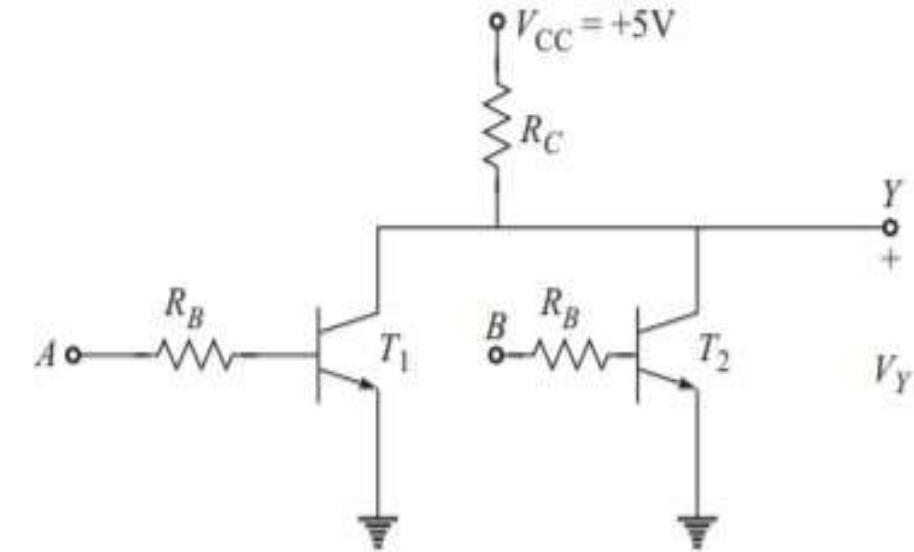
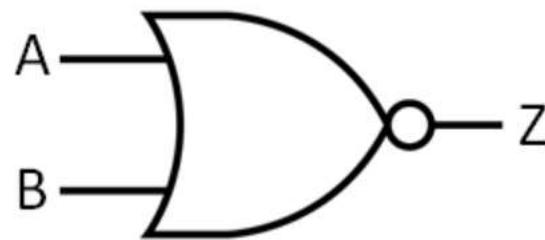
NOT Gate

J/P	O/P	Transistor region
Low	High	Cut off [ 0.0 ]
High	Low	Sat. [ $V_{CE} = 0.2V$ ]



# RTL NOR GATE

An RTL NOR gate can be made by replicating the Base resistor and the transistor in parallel for each input



## Disadvantages:

- Low noise margin
- Low speed
- Low fan out
- High power dissipation

$V_A$	$V_B$	$V_Y$
0	0	1
0	1	0
1	0	0
1	1	0

## **Advantages:**

- The primary advantage of RTL technology was that it used a minimum number of transistors.
- In circuits using discrete components, before integrated circuits, transistors were the most expensive component to produce.
- Early IC logic production (such as Fairchild's in 1961) used the same approach briefly, but quickly transitioned to higher-performance circuits such as diode-transistor logic and then transistor-transistor logic (starting in 1963 at Sylvania Electric Products), since diodes and transistors were no more expensive than resistors in the IC.

## **Limitations:**

- The disadvantage of RTL is its high power dissipation when the transistor is switched on, by current flowing in the collector and base resistors.
- This requires that more current be supplied to and heat be removed from RTL circuits.
- In contrast, TTL circuits with "totem-pole" output stage minimize both of these requirements
- Another limitation of RTL is its limited fan-in: 3 inputs being the limit for many circuit designs, before it completely loses usable noise immunity. It has a low noise margin.

# Diode Transistor Logic (DTL)

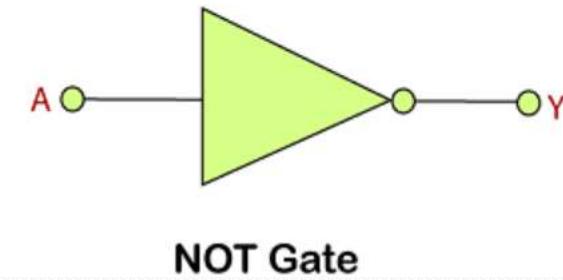
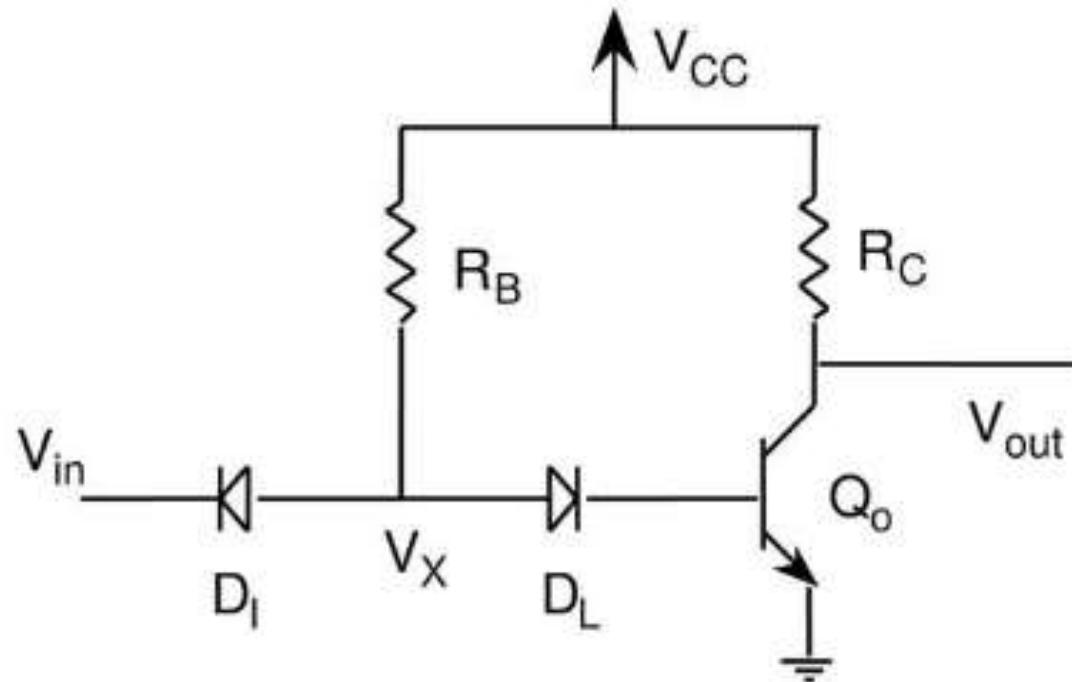
- **Diode-transistor logic (DTL)** is a class of digital circuits. It is called so because the logic gating functions AND and OR are performed by diode logic, while logical inversion (NOT) and amplification (providing signal restoration) is performed by a transistor (in contrast with RTL and TTL).

## Disadvantages:

- Low speed
- Power dissipation as heat

- ★ It has fan-out of 8.
- ★ It has high noise immunity.
- ★ Power dissipation is 12mw.
- ★ Propagation constant is average 30ns.
- ★ Noise margin is about 0.7v.

## DTL INVERTER:

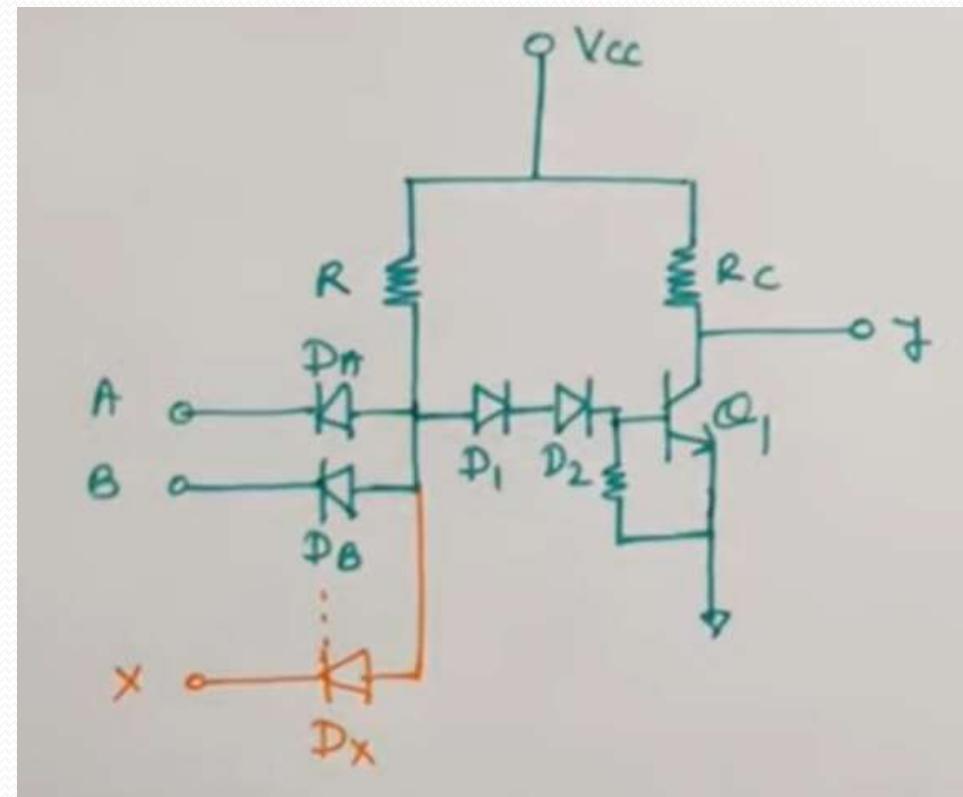
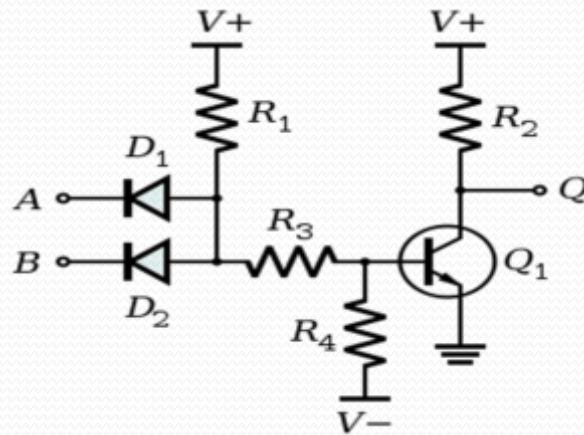


NOT Gate

Input	Output
0	1
1	0

## DTL NAND GATE

- Diode-Transistor Logic (DTL): The basic circuit in the DTL logic is the NAND gate.
  - Each input associated with one diode.
  - The diode and resistor form an AND gate.
  - The transistor amplifies the output



Input A	Input B	Output Y
0	0	1
0	1	1
1	0	1
1	1	0

### Case 1:

$A=0, B=0 \Rightarrow D_A \& D_B - F.B; D_1 \& D_2 - R.B,$   
 $Q_1$ -OFF. Then  $Y=1$

### Case 2:

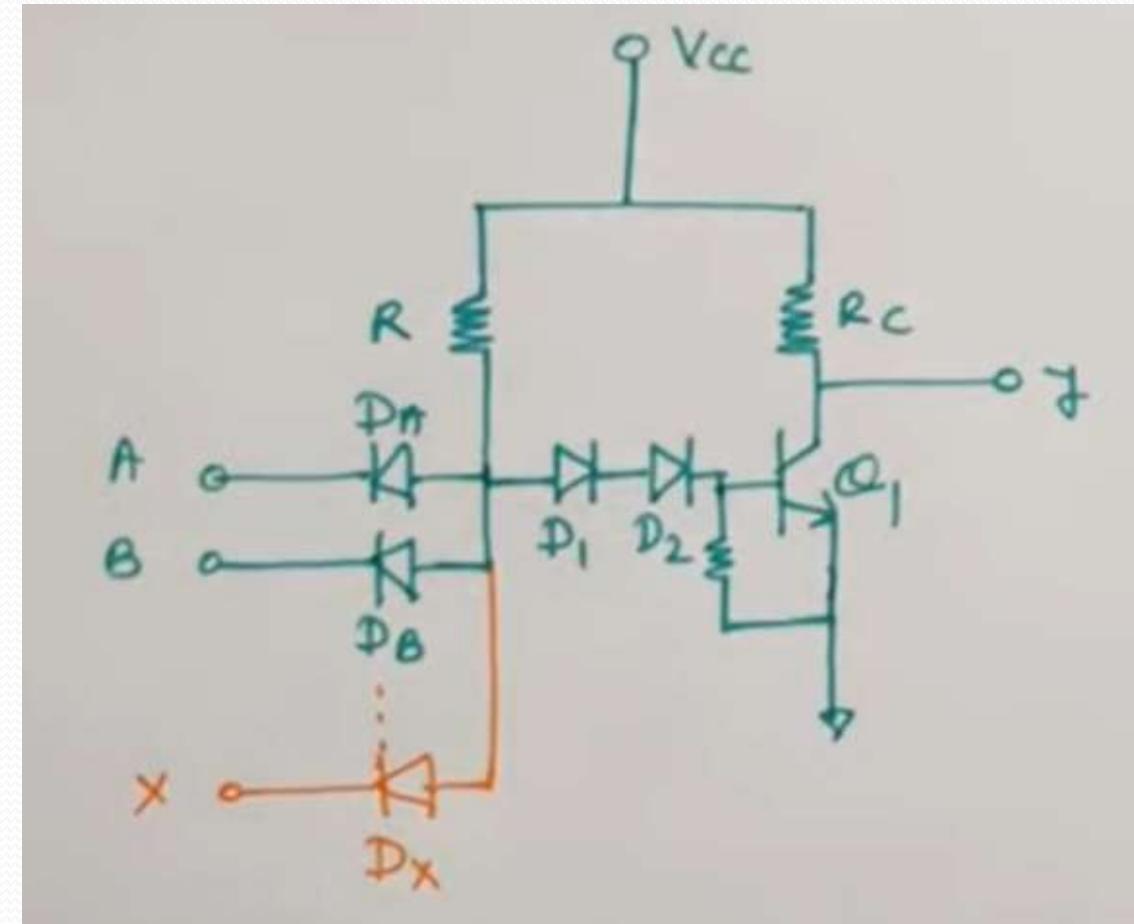
$A=0, B=1 \Rightarrow D_A - F.B \& D_B - R.B; D_1 \& D_2 - R.B,$   
 $Q_1$ -OFF. Then  $Y=1$

### Case 3:

$A=1, B=0 \Rightarrow D_A - R.B \& D_B - F.B; D_1 \& D_2 - R.B,$   
 $Q_1$ -OFF. Then  $Y=1$

### Case 4:

$A=1, B=1 \Rightarrow D_A \& D_B - R.B; D_1 \& D_2 - F.B,$   
 $Q_1$ -ON. Then  $Y=0$



# **TRANSISTOR TRANSISTOR LOGIC (TTL)**

- **Transistor-transistor logic (TTL)** is a logic family built from bipolar junction transistors. Its name signifies that transistors perform both the logic function (the first "transistor") and the amplifying function (the second "transistor"), as opposed to earlier resistor-transistor logic (RTL) and diode-transistor logic (DTL).
- TTL integrated circuits(ICs) were widely used in applications such as computers, industrial controls, test equipment and instrumentation, consumer electronics, and synthesizers.
- TTL manufacturers offered a wide range of logic gates, flip-flops, counters, and other circuits.

- TTL circuit design offered higher speed or lower power dissipation to allow design optimization.
- As transistor becomes ON and OFF much rapidly than a diode, switching time will be faster.
- TTL or Transistor-transistor logic replaced resistor-transistor logic, and used much less power.
- The TTL family is very fast and reliable, and newer faster, less power-consuming, etc.
- Transistor-Transistor Logic (TTL): uses multiple emitter transistor at the input.

### **TTL Classifications:**

- Standard TTL
- TTL Totem pole output
- TTL open collector output
- TTL Tristate

- ★ TTI has greater speed than DTL.
- ★ Less noise immunity.
- ★ Power dissipation is 10nw.
- ★ It has fan-in of 6 and fan-out of 10.
- ★ Propagation time delay is 5-15nsec.

## TTL NAND GATE

### Case 1:

- If any of the input is low, then T1 is in active region.
- Diode (BE) forward biased and diode (BC) reverse biased.
- T2 – OFF; T3 – OFF; **Output - HIGH**

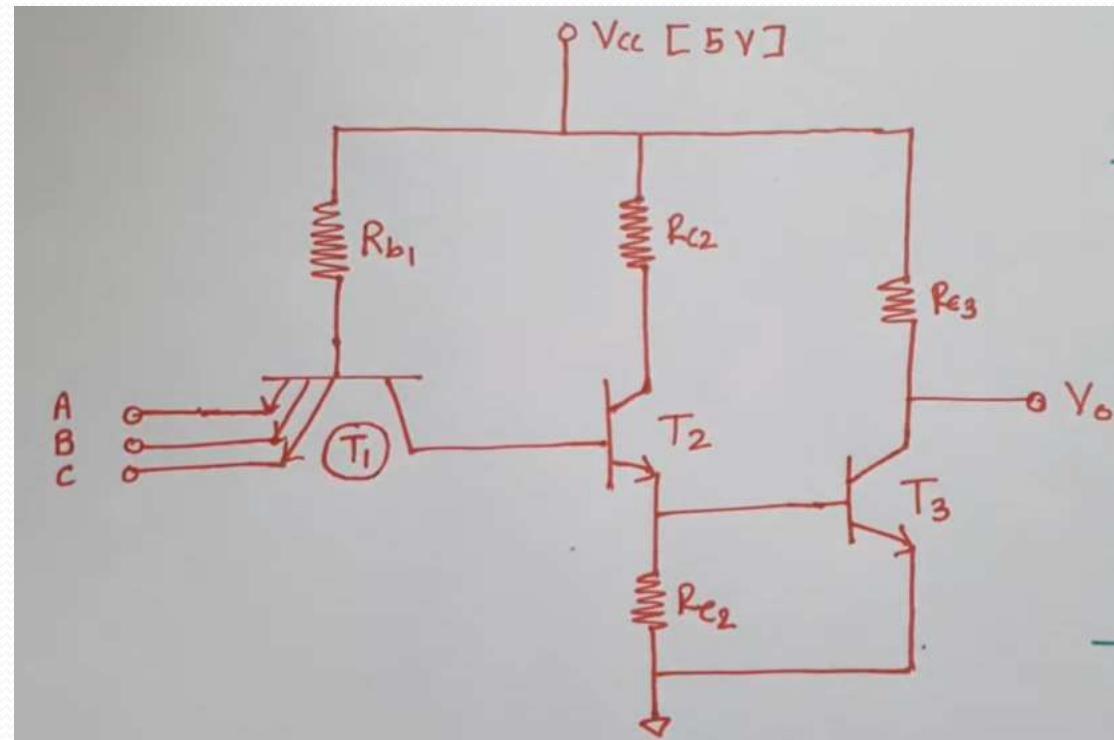
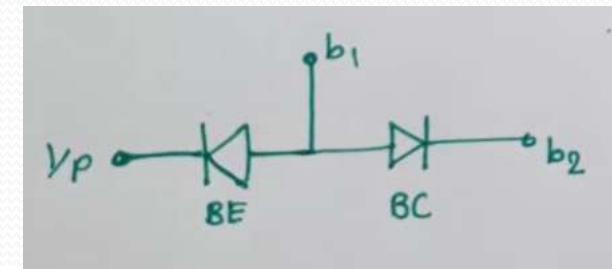
### Case 2:

- If all the input is HIGH
- Diode (BE) reverse biased and diode (BC) forward biased.
- T2 – ON; T3 – ON; **Output - LOW**

Drawback:

When T3-ON; R is HIGH

When T3-OFF; R is LOW

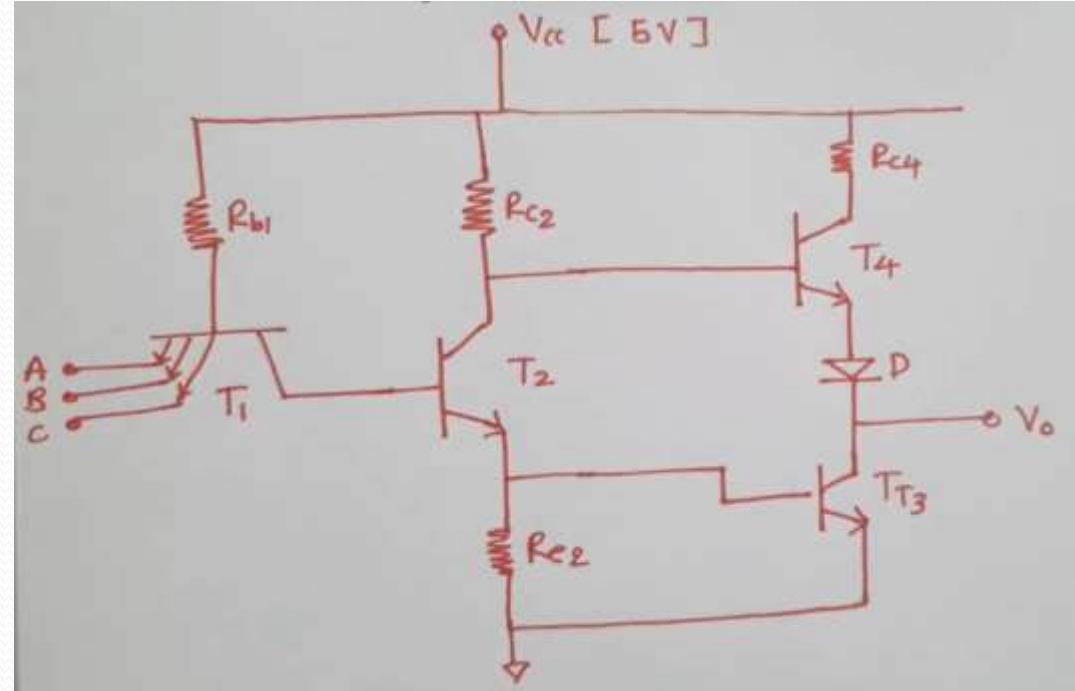
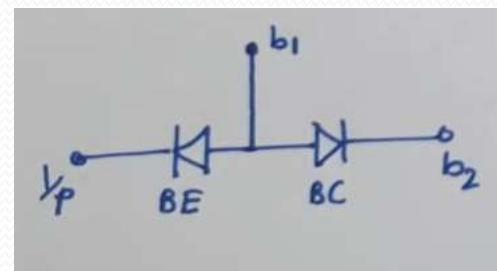


Input			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

## TTL NAND GATE WITH TOTEMPOLE OUTPUT

### Case 1:

- If any of the input is low, then T1 is in active region.
- Diode (BE) forward biased and diode (BC) reverse biased.
- T2 – OFF; T3 – OFF
- T4 - ON
- **Output - HIGH**



### Case 2:

- If all the input is HIGH
- Diode (BE) reverse biased and diode (BC) forward biased.
- T2 – ON; T3 – ON
- T4 - OFF
- **Output - LOW**

❖ Fanout & Noise margin improved by using totempole circuit at output.

Input			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

# TTL NOR GATE USING TOTEMPOLE

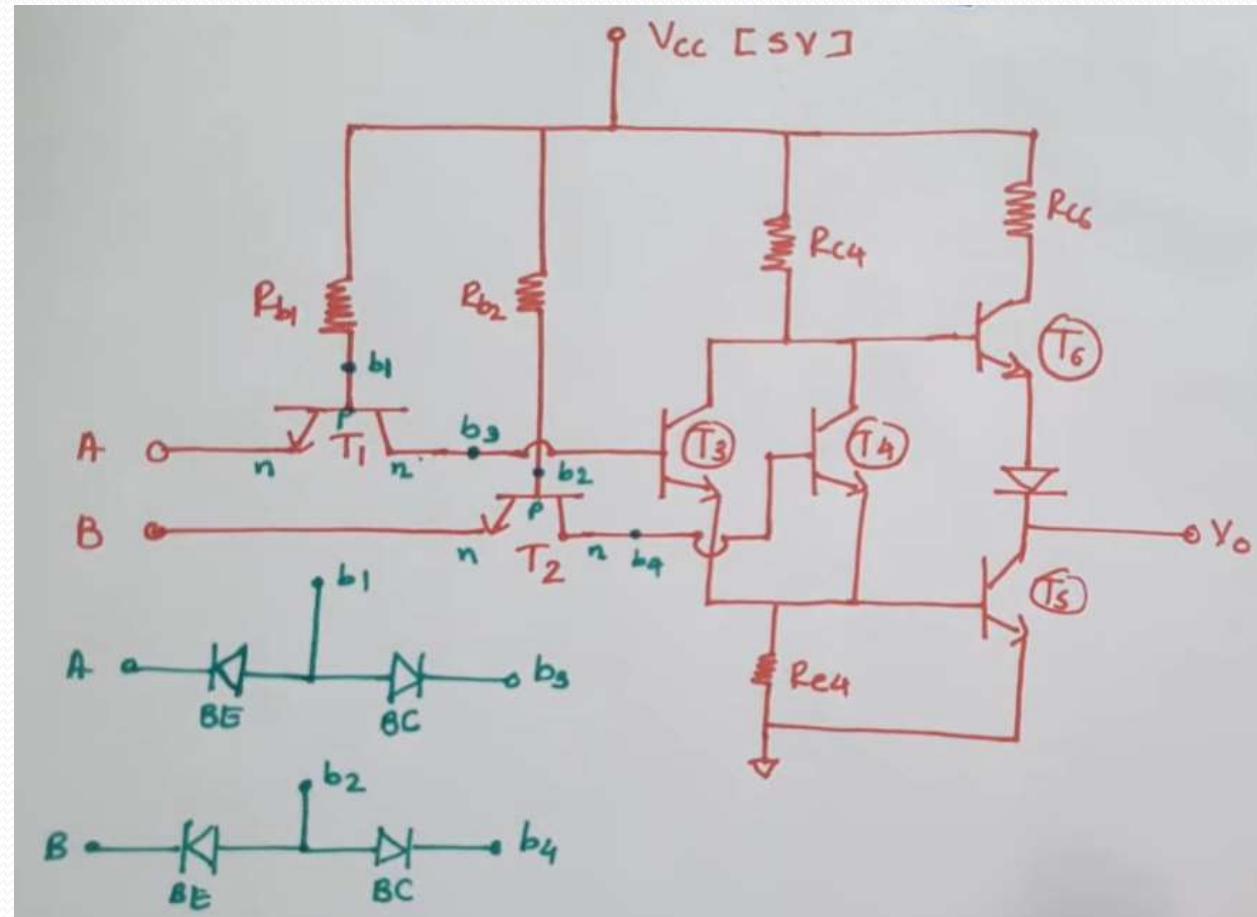
## Case 1:

- If both the inputs low, then T1 & T2 - BE forward biased and diode & BC reverse biased.
- T3 – OFF; T4 – OFF
- T5 – OFF; T6 - ON
- **Output - HIGH**

## Case 2:

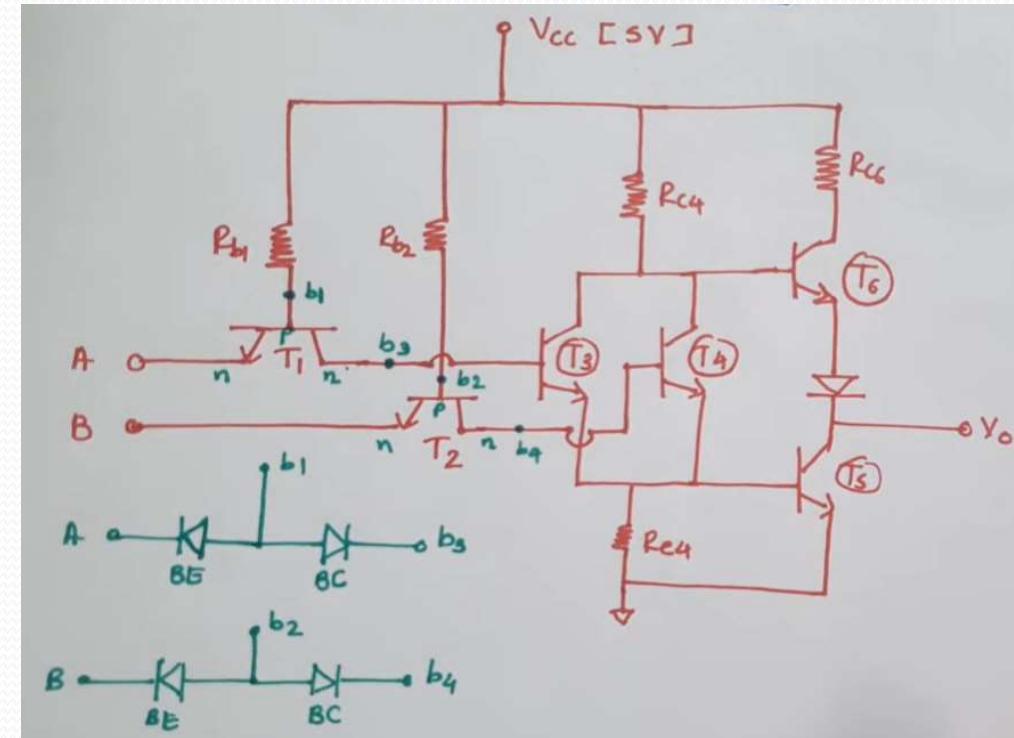
- If A==1, B=1, then
- T1 & T2 - BE reverse biased and diode & BC forward biased.
- T3 – ON; T4 – ON
- T5 – ON; T6 - OFF
- **Output - LOW**

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	0



### **Case 3:**

- If  $A=0, B=1$ , then
- T1 -(BE) forward biased and diode (BC) reverse biased.
- T2 - (BE) reverse biased and diode (BC) forward biased
- T3 – OFF; T4 – ON; T5 – ON; T6 - OFF
- **Output - LOW**



### **Case 4: If $A=1, B=0$ , then**

- T1 -(BE) reverse biased and diode (BC) forward biased.
- T2 - (BE) forward biased and diode (BC) reverse biased
- T3 – ON; T4 – OFF; T5 – ON; T6 - OFF
- **Output - LOW**

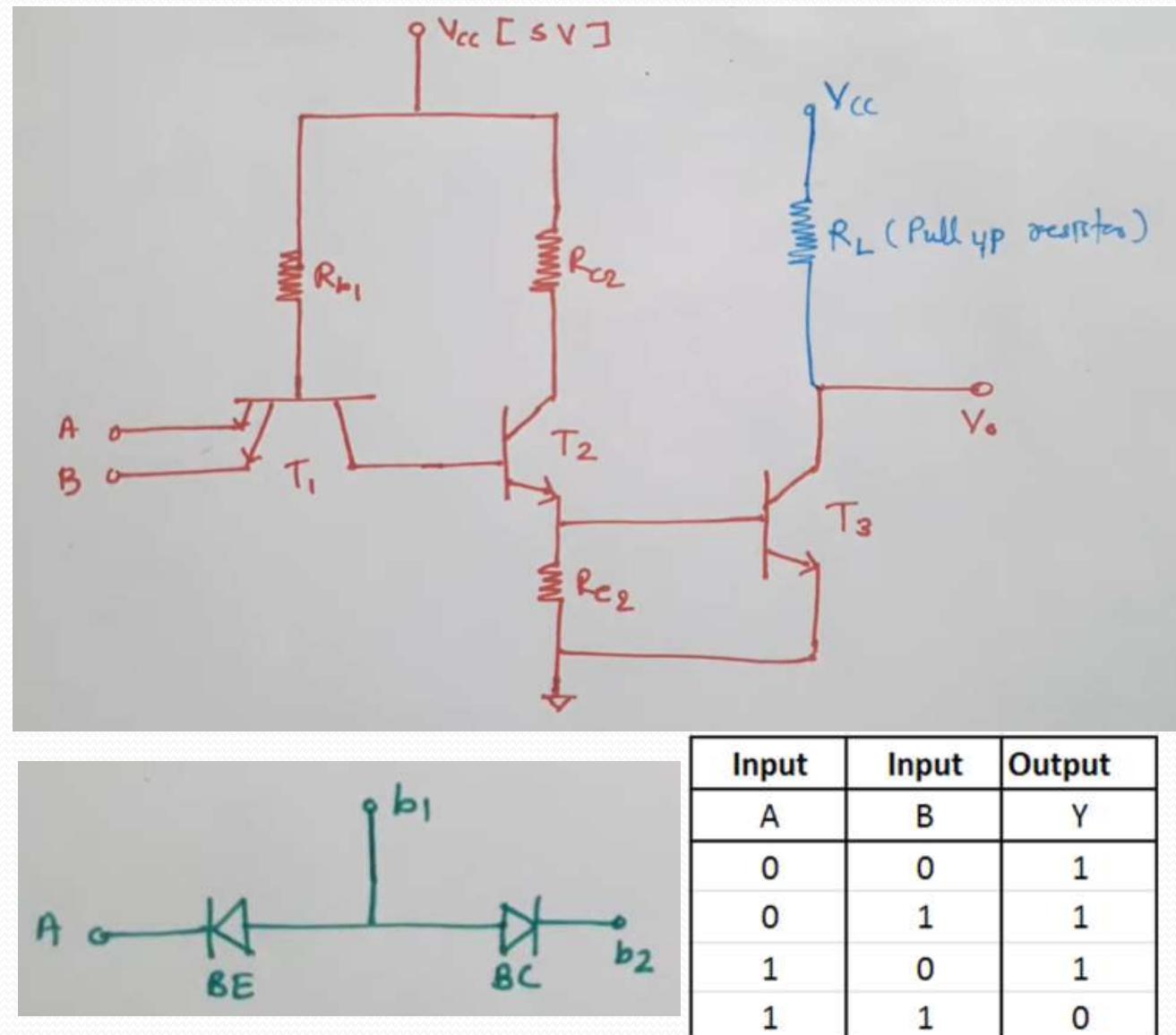
# TTL OPEN COLLECTOR NAND GATE

## Case 1:

- If any of the inputs LOW,
- Then T1 - BE forward biased & BC reverse biased.
- T2 – OFF; T3 – OFF
- **Output - HIGH**

## Case 2:

- If both the inputs HIGH,
- Then T1 - BE reverse biased & BC forward biased.
- T2 – ON; T3 – ON
- **Output – LOW**



## TTL TRISTATE LOGIC

In Tristate at the output there are 3 states.

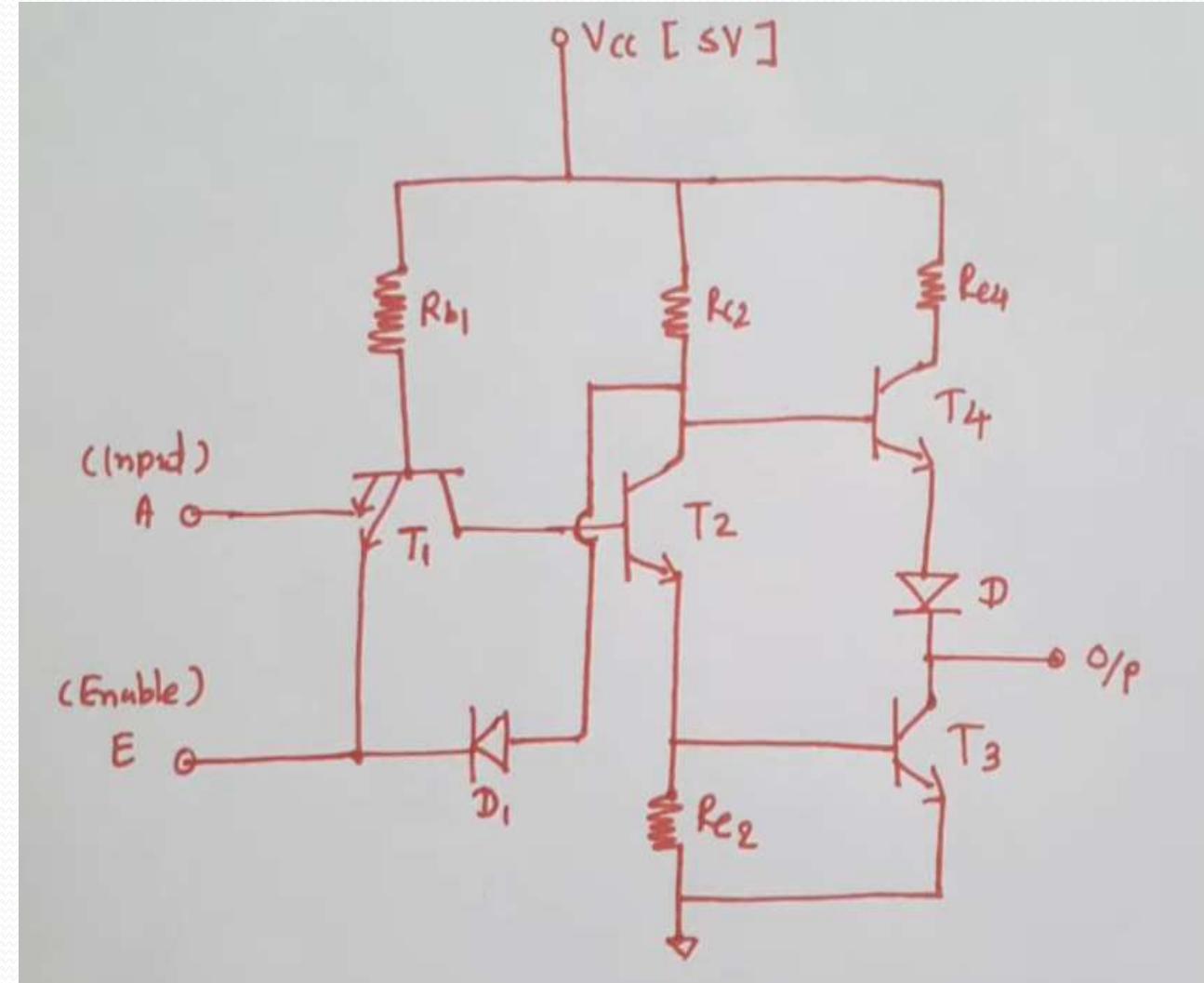
1. Logic high
2. Logic low
3. High impedance state

### Case 1:

- **Enable=0**, A is either 0 or 1
- D1-FB
- T2 – OFF; T3 – OFF; ; T4 – OFF
- **Output – At High impedance level**

### Case 2:

- **Enable=1**, D1-RB; A =0
- Then T1 - BE forward biased & BC reverse biased.
- T2 – OFF; T3 – OFF; ; T4 – ON
- **Output – High**

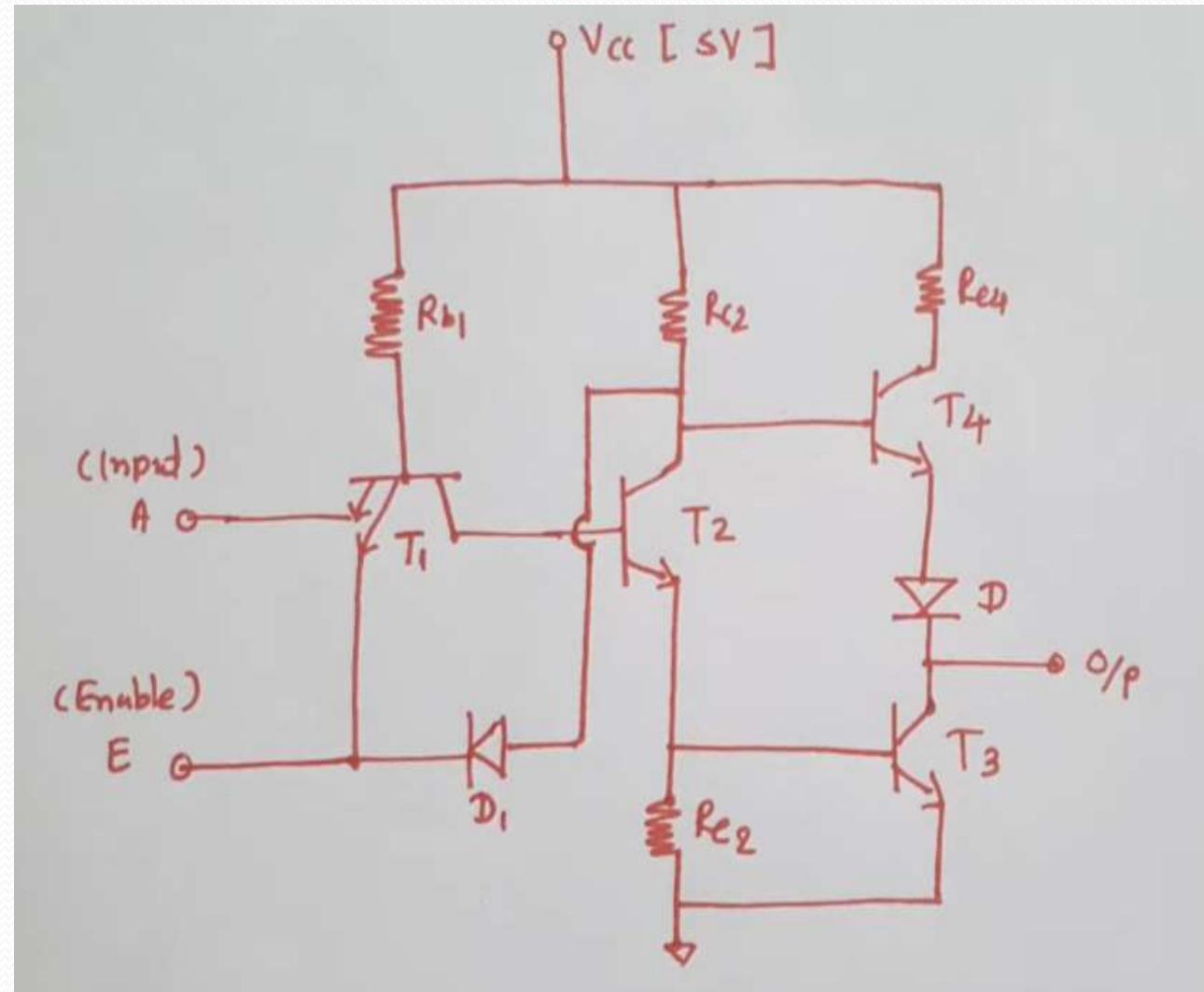


### Case 3:

- **Enable=1**, D1-RB; A =1
- Then T1 - BE reverse biased & BC forward biased.
- T2 – ON; T3 – ON; ; T4 – OFF
- **Output – Low**

### NOTE: 3 States

- **Enable=0 => High impedance**
- **Enable=1**
  - (i) **A=0 => Output – High**
  - (ii) **A=1 => Output – Low**

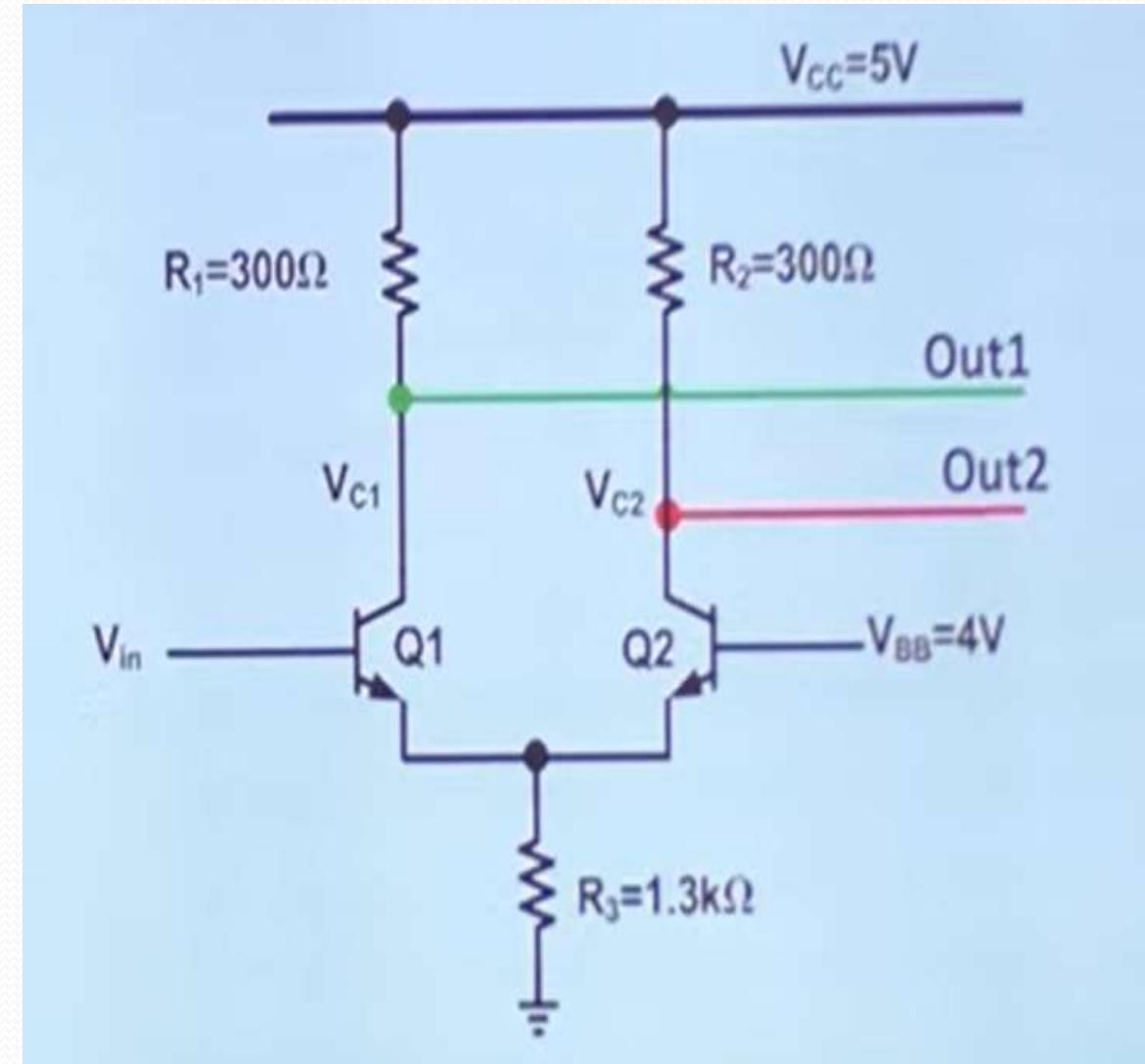


## **EMITTER COUPLED LOGIC**

- ECL was invented in August 1956 at IBM
- Originally called current-steering logic. The logic was also called a current mode circuit
- Positive ECL ( $V_{CC}=+5V$ ,  $V_{EE}=0V$ ) and Negative ECL ( $V_{EE}=-5.2V$ ,  $V_{CC}=0V$ )
- ECL achieves its high speed operation
- In the late 1960s, when the standard TTL family offered 20ns gate delay and the CMOS 4000 family had delays of 100ns or more, ECL offered an incredible delay of only 1ns
- ECL is a High speed logic family based on bipolar transistor
- It basically operates on current mode of operation
- Transistors are driven either in cut-off or in active region.
- It is the fastest of all the logic families. Propagation delay is less than 1ns per gate.
- It is differential logic.

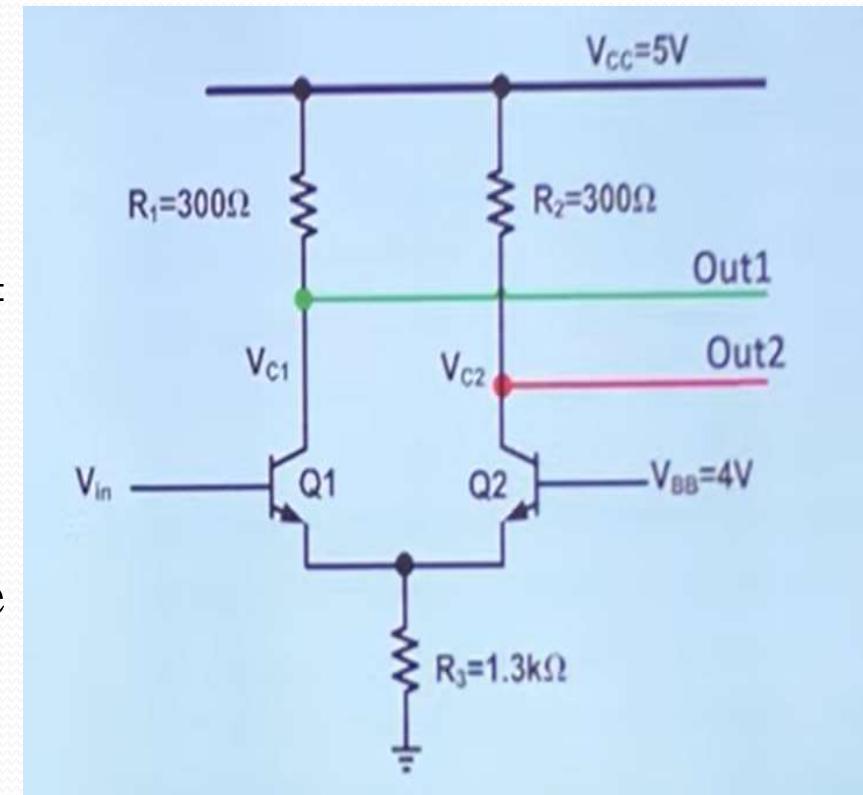
## ECL INVERTER / BUFFER GATE

- The input LOW level is 3.6V
- The input HIGH level is 4.4V
- This circuit produces output LOW and HIGH levels that are 4.2 and 5V.
- The outputs of this inverter are called differential outputs because they are always complementary.
- The output is 1 if  $(V_{out1}-V_{out2}) > 0$  and it is 0 if  $(V_{out1}-V_{out2}) < 0$

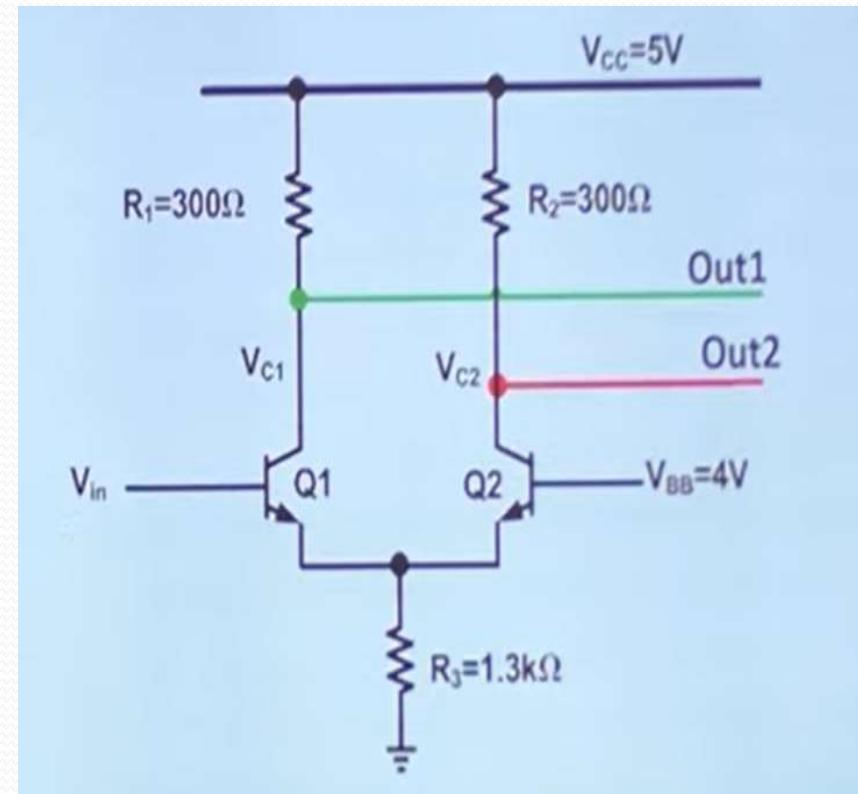


## OPERATION OF ECL INVERTER / BUFFER GATE

- CASE-1: Input is logic HIGH=4.4V applied to Q1
- V<sub>BB</sub>=4V – reference voltage
- Q1 – ON for 4.4V
- At emitter junction voltage is  $4.4 - V_{BE} = 4.4 - 0.6 = 3.8V$
- At Q2, input is 4v and emitter voltage is 3.8V.
- So  $V_{BE}=4-3.8=0.2V$ . So Q2-OFF
- In the first branch some amount of current flows. In the second branch current is zero.
- **VC2= V<sub>cc</sub>-IR2=5-0=5V - Logic HIGH**
- **VC1=V<sub>cc</sub>-(IE \* R1)= 5 – 2.9mA\*300=4.2V - Logic LOW**  
 $IE=VE / R3= 3.8/1.3K\Omega=2.9mA$
- Vin= 4.4V (LOGIC HIGH)
- **Outputs: VC1=4.2V (LOGIC LOW) – Inverter output ;**  
**VC2=5V (LOGIC HIGH) – Buffer output**



- CASE-2: Input is logic LOW=3.6V applied to Q1
- V<sub>BB</sub>=4V – reference voltage applied to Q2
- **Q2 – ON** for 4V
- At emitter junction voltage is  $4 - V_{BE} = 4 - 0.6 = 3.4V$
- At Q1, input is 3.6v and emitter voltage is 3.4V.
- So  $V_{BE}=3.6-3.4=0.2V$ . So **Q1-OFF**
- In the second branch some amount of current flows. In the first branch current is zero.
  
- **$V_{C1} = V_{CC} - IR_1 = 5 - 0 = 5V$  - Logic HIGH**
- **$V_{C2} = V_{CC} - (I_E * R_2) = 5 - 2.9mA * 300 = 4.2V$  - Logic LOW**  
 $I_E = V_E / R_3 = 3.8 / 1.3k\Omega = 2.9mA$
- $V_{in} = 3.6V$  (LOGIC LOW)
- **Outputs:  $V_{C1}=5V$  (LOGIC HIGH) – Inverter output ;**  
 **$V_{C2}=5V$  (LOGIC HIGH) – Buffer output**



# ECL NOR / OR GATE

**CASE-1:**  $a=b=0=3.6V$

Q1a, Q1b – OFF; Q2- ON

$V_{out1}=V_{C1}=V_{CC}=5V$  (Logic HIGH)

$V_{out2}=V_{C2}=4.2V$  (Logic LOW)

**CASE-2:**  $a=0=3.6V, b=1=4.4V$

Q1a=OFF; Q1b – ON; Q2- OFF

$V_{out1}=V_{C1}=V_{CC}-I_E R_1=4.2V$  (Logic LOW)

$V_{out2}=V_{C2}=5V$  (Logic HIGH)

**CASE-3:**  $a=1=4.4V, b=0=3.6V$

Q1a=ON; Q1b – OFF; Q2- OFF

$V_{out1}=V_{C1}=V_{CC}-I_E R_1=4.2V$  (Logic LOW)

$V_{out2}=V_{C2}=5V$  (Logic HIGH)

**CASE-4:**  $a=b=1=4.4V$

Q1a = Q1b = ON; Q2- OFF

$V_{out1}=V_{C1}=V_{CC}-I_E R_1=4.2V$  (Logic LOW)

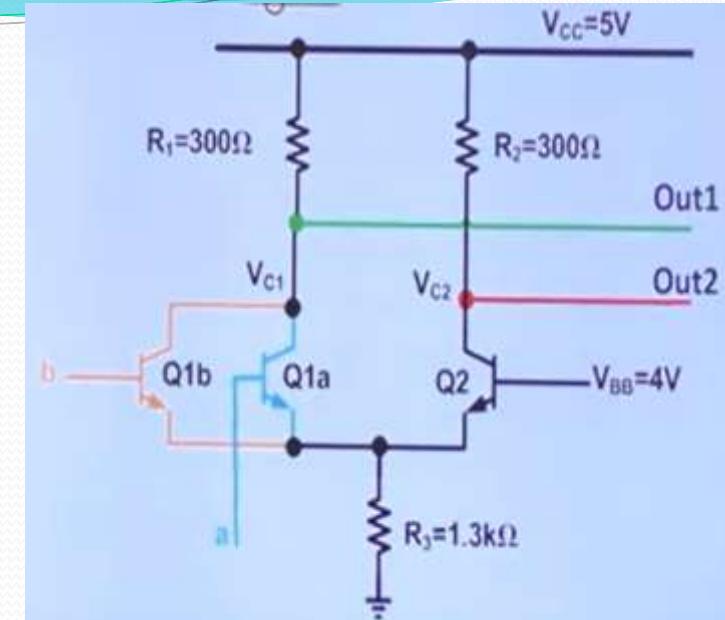
$V_{out2}=V_{C2}=5V$  (Logic HIGH)

a	b	Vout1	Vout2
3.6	3.6	5	4.2
0	0	1	0
NOR		OR	

a	b	Vout1	Vout2
3.6	4.4	4.2	5
0	1	0	1
NOR		OR	

a	b	Vout1	Vout2
4.4	3.6	4.2	5
1	0	0	1
NOR		OR	

a	b	Vout1	Vout2
4.4	4.4	4.2	5
1	1	0	1
NOR		OR	



I/P	Q1A	Q1B	Q2	Out1	Out2
0 0	OFF	OFF	ON	1	0
0 1	OFF	ON	OFF	0	1
1 0	ON	OFF	OFF	0	1
1 1	ON	ON	OFF	0	1

# ECL Logic Families

- ECL 10K/10H Families
  - Came from Motorola
  - Voltage Compensated
  
- ECL 100K Families
  - Came from Fairchild
  - Voltage & Temperature Compensated

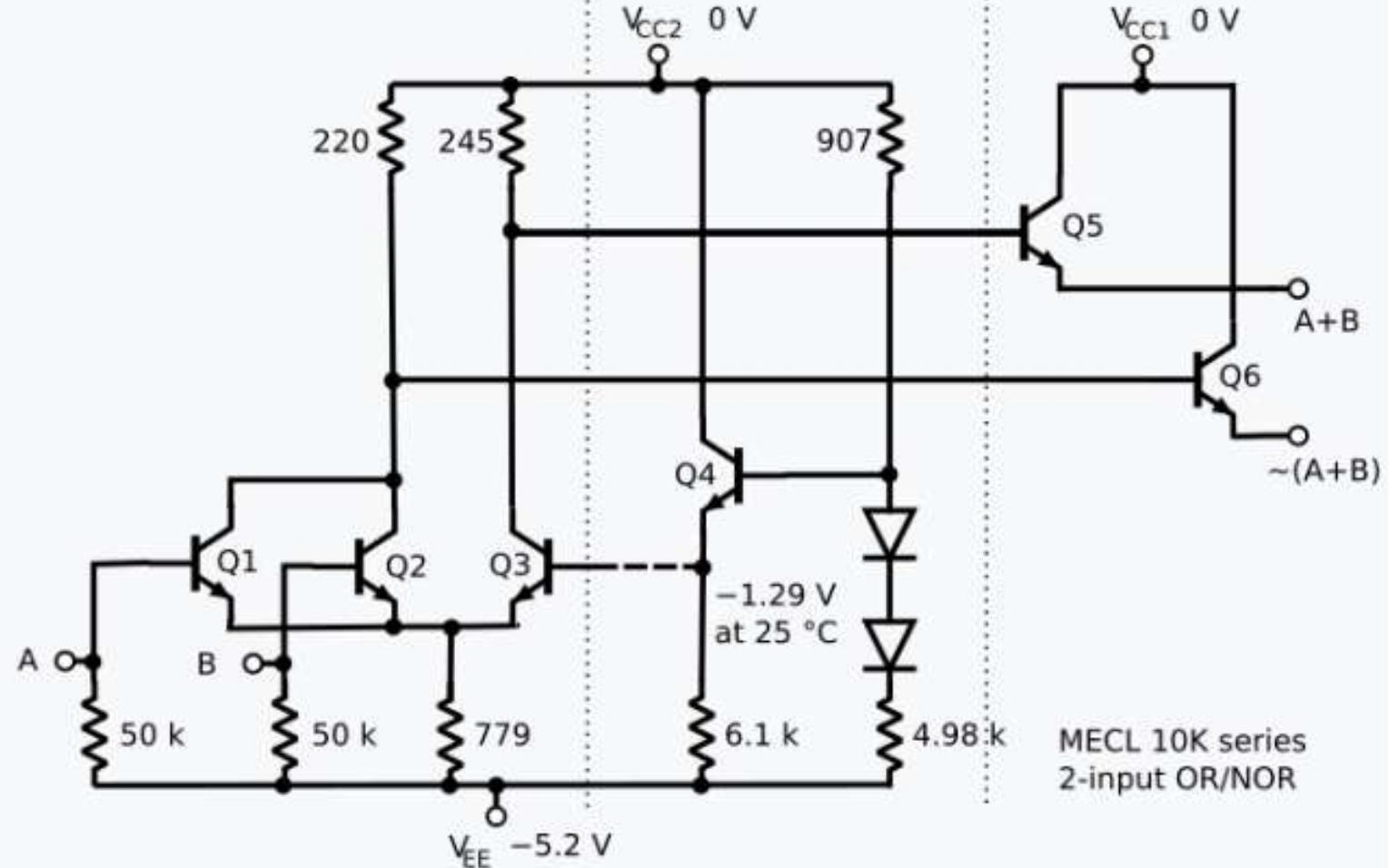
3 stages

- Differential stage
- Biasing stage
- Emitter follower stage

Differential-amplifier input and logic section

Internal temperature- and voltage-compensated bias network section (one supplies several differential amplifiers)

Emitter-follower output section



## **Advantages & Disadvantages of ECL**

### **Advantages:**

- Fastest logic family
- Low gate delays
- High fan-out capability
- Low power consumption
- Compatibility with other logic families

### **Disadvantages:**

- Negative supply
- High static power dissipation
- Limited choice of manufacturers and devices
- Low noise margin

# Comparison between Logic Families

S.No.	Parameter	CMOS	TTL	ECL
1	Device used	NMOS & PMOS	BJT	BJT
2	Basic gate	NAND/NOR	NAND	NOR/OR
3	Propagation Delay	70ns	10ns	500ps
4	Switching speed	Less than TTL	Faster than CMOS	Fastest
5	Power Dissipation per gate	0.1mW	10mW	25mW
6	Power Dissipation	Increases with frequency	Increases with frequency	Constant with frequency
7	Fan out	50	10	25
8	Power Supply Voltage	3-15V	Fixed 5V	-4.5 to 5.2V
9	Noise Immunity	Excellent	Very good	Good
10	Applications	Portable instrument where battery supply is used	Laboratory instruments	High speed instruments