Guru Nanak Institutions Technical Campus
School of Engineering and Technology

Ibrahimpatnam, R R District, Telangana – 501506

B. TECH. III YEAR II SEM. ALL SUBJECTS HANDBOOK

Academic Year: 2023-2024

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHOOL OF ENGINEERING AND TECHNLOGY

ANTENNAS AND PROPAGATION (21PE0EC2A)

HANDBOOK

K.RAMYASREE

ASSISTANT PROFESSOR

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHOOL OF ENGINEERING AND TECHNLOGY

Vision & Mission

Vision of the Institution: GURU NANAK INSTITUTIONS TECHNICAL CAMPUS

To be an internationally renowned institution in Engineering, Management, Pharmacy and related fields to produce scientists, engineers, entrepreneurs, leaders, academicians and thinkers of tomorrow with exemplary professional conduct and adherence to ethical values to serve for changing needs of industry and society.

Mission of the Institution: GNITC

M1: Imbibe soft skills, technical skills, creatively and passion in students.

M2: Develop the faculty to reach the International standards.

M3: Maintain outcome based student centric teaching learning with high academic standards and quality that promotes the analytical thinking and independent judgment.

M4: Promote research, innovation, product development by collaborating with reputed industries & reputed universities in India and abroad. Offer collaborative industry programs in emerging areas and instill the spirit of enterprising.

M5: To instill the ethical values in the faculty and students to serve the society.

Department of Electronics and Communications Engineering

Vision of the Department:

To be a premier Department of Electronics and Communication Engineering in the region by providing high quality Education, Research and Employability.

Mission of the Department:

M1: Nurture young individuals into knowledgeable, skillful, and ethical professionals in their pursuit of Electronics and Communication Engineering.

M2: Transform the students through soft skills, excellent teaching learning process and sustain high performance by innovations.

M3: Extensive MoUs with National & Foreign universities to enrich the knowledge of the students & faculty and active participation in Research..

M4: Develop industry-interaction for innovations and product design & development to provide to make the students as innovators, set up the start up units and get good placements

Guru Nanak Institutions Technical Campus (Autonomous)
School of Engineering & Technology

III Year B.Tech. ECE II-Sem

L	T	P	C
3	0	0	3

(21PE0EC2A) Antenna and Propagation

Unit – I	**Antenna Basics Fundamental Concepts:** Physical concept of radiation, Radiation pattern, near-and far-field regions, reciprocity, directivity and gain, effective aperture, polarization, input impedance, efficiency, Friis transmission equation, radiation integrals and auxiliary potential functions. **Wire and Loop Antennas:** Radiation from Wires and Loops- Infinitesimal dipole, finite-length dipole, linear elements near conductors, dipoles for mobile communication, small circular loop.
Unit –II	**Aperture and Reflector Antennas:** Huygens' principle, radiation from rectangular and circular apertures, design considerations, Babinet's principle, Radiation from sectoral and pyramidal horns, design concepts, prime-focus parabolic reflector and cassegrain antennas. **Broadband Antennas:** Log-periodic and Yagi-Uda antennas, frequency independent antennas, broadcast antennas.
Unit – III	**Micro strip Antennas:** Basic characteristics of micro strip antennas, feeding methods, methods of analysis, design of rectangular and circular patch antennas
Unit – IV	**Antenna Arrays Antenna Arrays:** Analysis of uniformly spaced arrays with uniform and non-uniform excitation amplitudes, extension to planar arrays, and synthesis of antenna arrays using Schelkunoff polynomial method, Woodward-Lawson method.
Unit -V	**Basic Concepts of Smart Antennas:** Concept and benefits of smart antennas, fixed weight beam forming basics, Adaptive beam forming. Different modes of Radio Wave propagation used in current practice.

TEXT BOOKS:

1. J.D. Kraus, Antennas, McGraw Hill, 1988.
2. C.A. Balanis, Antenna Theory - Analysis and Design, John Wiley, 1982.

REFERENCE BOOKS:

1. R.E. Collin, Antennas and Radio Wave Propagation, McGraw Hill, 1985.
2. R.C. Johnson and H. Jasik, Antenna Engineering Handbook, McGraw Hill, 1984.
3. I.J. Bahl and P. Bhartia, Micro Strip Antennas, Artech House, 1980. 4. R.E. Crompton, Adaptive Antennas, John Wiley

CONSOLIDATED UNIT WISE LESSON PLAN:-

Subject: Antennas & Propagation			
Name of the Faculty: K Ramyasree			
Text Books			
Book 1	J.D. Kraus, Antennas, McGraw Hill, 1988.		
Book 2	C.A. Balanis, Antenna Theory - Analysis and Design, John Wiley, 1982.		
Reference Books			
Book 3	R.E. Collin, Antennas and Radio Wave Propagation, McGraw Hill, 1985.		
Book 4	R.C. Johnson and H. Jasik, Antenna Engineering Handbook, McGraw Hill, 1984.		
Book 5	I.J. Bahl and P. Bhartia, Micro Strip Antennas, Artech House, 1980. 4. R.E. Crompton, Adaptive Antennas, John Wiley		
Unit	**Topic**	**Books**	**No of Classes**
I	**Antenna Basics Fundamental Concepts**	1,2,3,4,5	**16**
II	**Aperture and Reflector Antennas**	3,4	**13**
III	**Micro strip Antennas**	4,5	**8**
IV	**Antenna Arrays Antenna Arrays**	1,3	**8**
V	**Basic Concepts of Smart Antennas**	5	**10**
	Contact classes for syllabus coverage		55
	Tutorial Classes		10
	Descriptive Tests		02
	Classes for beyond syllabus		03
	Remedial Classes/NPTEL		05
	Total Number of Classes		75

COURSE PRE-REQUISITES:

C.CODE	COURSE NAME	DESCRIPTION	SEM
22PC0EC21	**ELECTROMAGNETIC WAVES AND TRANSMISSION LINES**	**Coordinate system, Maxwell equations**	**II/I**

COURSE OBJECTIVE

Understand the basic terminology, concept of radiation, design antennas and understand the propagation of waves

COURSE OUTCOMES

1	Define the basics of antenna
2	Characterize the antennas based on frequency.
3	Analyze the Microstrip patch antenna and reflector antenna.
4	Design Broadside array and End fire array antenna.
5	Differentiate fixed beam forming and adaptive beam forming and different wave propagation mechanism

TUTORIAL CLASSES

S. No.	Topic delivered	
	UNIT -I	
1	Show that radiation resistance of λ/2 dipole antenna is 73ohms?	
2	Calculate the Effective Aperture of an Antenna	
	UNIT -II	
3	Explain in details about various frequency independent antennas and their radiation patterns	
4	Explain in detail about Broadcast Antennas	
	UNIT -III	
5	Give the geometry of Microstrip patch antenna and draw the normalized radiation pattern obtained	
6	E xplain in detail about various feeding methods used in Micro strip patch antennas	
	UNIT -IV	
7	Synthesize the antenna array using schelkunoff polynomial method	
8	Give the equations for antenna array using Woodward lawson method	
	UNIT -V	
9	Explain in detail about the advantage of adaptive beam forming compared with fixed beam forming	
10	A high frequency radio link to be established between 2 points at a distance of 2500km on earth surface. Considering the ionosphere height to be 200km and its critical frequency 5MHz, calculate MUF for given path	

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Lecture Plan with Blooms Taxonomy

Name of the Subject: Antennas & Propagation
Subject Code: 21PE0EC2A
Name of Faculty: K.Ramyasree
Class & section: III-3

BTL- Blooms Taxonomy Level

Level 0 - Remembering
Level 1 - Understanding
Level 2 - Applying
Level 3 - Analyzing
Level 4 - Evaluating
Level 5 - Creating

Cumm. Periods	Time (Min)	Topics	BTL	Teaching – Learning Method
UNIT I : ANTENNA BASICS FUNDAMENTAL CONCEPTS				
1	50	Pre-Requisites About EMTL	1	Chalk & Talk
2	50	Introduction To Waves And Electromagnetic Spectrum	1	PPT
3	50	Introduction To Antennas	1	Chalk & Talk
4	50	Physical Concept Of Radiation	2	Chalk & Talk
5	50	Radiation Pattern	2	Chalk & Talk
6	50	Near-And Far-Field Regions	2	Chalk & Talk
7	50	Reciprocity, Directivity And Gain	3	Chalk & Talk
8	50	Effective Aperture	2	Chalk & Talk
9	50	Polarization, Input Impedance	3	Chalk & Talk
10	50	Efficiency, Friis Transmission Equation	3	PPT
11	50	Radiation Integrals And Auxiliary Potential Functions	3	Chalk & Talk
12	50	Radiation From Wires And Loops- Infinitesimal Dipole	3	Chalk & Talk
13	50	Finite-Length Dipole	2	Chalk & Talk
14	50	Linear Elements Near Conductors	2	Chalk & Talk

15	50	Dipoles For Mobile Communication	2	Chalk & Talk
16	50	Small Circular Loop	3	Chalk & Talk
17	50	**Tutorial Classes 1**		Chalk & Talk
18	50	**Tutorial Classes 2**		Chalk & Talk
19	50	**Remedial Classes/NPTEL 1**		Chalk & Talk
UNIT II : APERTURE AND REFLECTOR ANTENNAS				
20	50	Huygens' Principle	2	PPT
21	50	Radiation From Rectangular And Circular Apertures	3	Chalk & Talk
22	50	Design Considerations	3	Chalk & Talk
23	50	Babinet's Principle	2	PPT
24	50	Radiation From Sectoral And Pyramidal Horns	3	Chalk & Talk
25	50	Design Concepts	4	Chalk & Talk
26	50	Prime-Focus Parabolic Reflector	3	PPT
27	50	Cassegrain Antennas	3	Chalk & Talk
28	50	Log-Periodic Antenna	3	Chalk & Talk
29	50	Yagi-Uda Antennas	4	PPT
30	50	Frequency Independent Antennas	3	Chalk & Talk
31	50	Broadcast Antennas	4	Chalk & Talk
32	50	Advantages, Disadvantages, Applications	2	Chalk & Talk
33	50	**Classes for beyond syllabus 1**		Chalk & Talk
34	50	**Tutorial Classes 3**		Chalk & Talk
35	50	**Tutorial Classes 4**		Chalk & Talk
36	50	**Remedial Classes/NPTEL 2**		Chalk & Talk
37	50	**SDT 1**		Chalk & Talk
UNIT III : MICROSTRIP ANTENNAS				
38	50	Basic Characteristics Of Micro Strip Antennas	1	Chalk & Talk
39	50	Feeding Methods	2	PPT

40	50	Methods Of Analysis	3	Chalk & Talk
41	50	Rectangular Patch Antennas	4	PPT
42	50	Circular Patch Antennas	3	Chalk & Talk
43	50	Designing Parameters	4	Chalk & Talk
44	50	Parameters of Micro strip Antennas	2	Chalk & Talk
45	50	Advantages, Disadvantages, Applications	2	Chalk & Talk
46	50	**Classes for beyond syllabus 2**		Chalk & Talk
47	50	**Tutorial Classes 5**		Chalk & Talk
48	50	**Tutorial Classes 6**		Chalk & Talk
49	50	**Remedial Classes/NPTEL 3**		Chalk & Talk
UNIT IV : ANTENNA ARRAYS				
50	50	Antenna Arrays	2	Chalk & Talk
51	50	Types of antenna Arrays	2	Chalk & Talk
52	50	Analysis Of Uniformly Spaced Arrays With Uniform Excitation Amplitudes	4	Chalk & Talk
53	50	Analysis Of Uniformly Spaced Arrays With Non-Uniform Excitation Amplitudes	4	Chalk & Talk
54	50	Extension To Planar Arrays	4	Chalk & Talk
55	50	Synthesis Of Antenna Arrays	4	Chalk & Talk
56	50	Schelkunoff Polynomial Method	3	Chalk & Talk
57	50	Woodward-Lawson Method	3	Chalk & Talk
58	50	**Classes for beyond syllabus 3**		Chalk & Talk
59	50	**Tutorial Classes 7**		Chalk & Talk
60	50	**Tutorial Classes 8**		Chalk & Talk
61	50	**Remedial Classes/NPTEL 4**		Chalk & Talk
UNIT V : SMART ANTENNAS AND WAVE PROPAGATION				
62	50	Introduction To Smart Antennas	1	Chalk & Talk
63	50	Concept Of Smart Antennas	2	Chalk & Talk
64	50	Benefits Of Smart Antennas	1	Chalk & Talk

65	50	Beam Forming Basics	3	PPT
66	50	Fixed Weight Beam Forming	3	Chalk & Talk
67	50	Adaptive Beam Forming	3	Chalk & Talk
68	50	Modes Of Radio Wave Propagation	2	Chalk & Talk
69	50	Ground Wave Propagation	2	Chalk & Talk
70	50	Space Wave Propagation	2	PPT
71	50	Sky Wave Propagation	2	PPT
72	50	**Tutorial Classes 9**		Chalk & Talk
73	50	**Tutorial Classes 10**		Chalk & Talk
74	50	**Remedial Classes/NPTEL 5**		Chalk & Talk
75	50	**SDT 2**		Chalk & Talk

TEXT/REFERENCE BOOKS:

T/R	BOOK TITLE/AUTHORS/PUBLICATION
T	J.D. Kraus, Antennas, McGraw Hill, 1988.
T	C.A. Balanis, Antenna Theory - Analysis and Design, John Wiley, 1982.
R	R.E. Collin, Antennas and Radio Wave Propagation, McGraw Hill, 1985.
R	R.C. Johnson and H. Jasik, Antenna Engineering Handbook, McGraw Hill, 1984.
R	I.J. Bahl and P. Bhartia, Micro Strip Antennas, Artech House, 1980. 4. R.E. Crompton, Adaptive Antennas, John Wiley

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Date:

Question Bank with Blooms Taxonomy Level (BTL)

Academic Year: **2023-24**

Subject Name with code: **ANTENNAS AND PROPAGATION (21PE0EC2A)**

Class: **III YEAR /II SEMESTER**

Name of the Faculty Member: **K.RAMYASREE**

Blooms Taxonomy Levels (BTL)

1. Remembering
2. Understanding
3. Applying
4. Analyzing
5. Evaluating
6. Creating

Sl.No.	Questions (Select Questions from University question Bank and mention year in bracket or you may give own standard question with (new) in bracket)	BTL level (Please mention L1 or L2 or etc...)	Course Outcome (Please mention CO1 or CO2 etc…)
	Unit - I		
	Part – A (2 Marks)		
1	Define isotropic source? **(NOV/DEC 2016 - R13)**	1	CO1
2	What is meant by Beam area? **(NOV/DEC 2016 – R13)**	2	CO1
3	Distinguish between far field and near field? **(NOV 2015 – R09)**	2	CO1
4	Define Radiation Intensity of an Antenna **(New)**	2	CO1
5	Define Directivity and Gain of an Antenna and give the relation between them **(New)**	2	CO1
6	Give the Friis transmission equation**(New)**	1	CO1
7	Define a Hertzian dipole? **(New)**	1	CO1
	Part – B (5 Marks)		
1	Show that radiation resistance of λ/2 dipole antenna is 73ohms? **(JUNE/JULY 2014 – R09,NOV/DEC 2017 –R15)**	3	CO1
2	Explain the concept of retarded vector potential? **(NOV 2015 - R09)**	2	CO1

3	Derive the expression for field components of a small loop antenna? **(NOV/DEC 2016 –R13)**	3	CO1
4	Calculate the Effective Aperture of an Antenna **(New)**	3	CO1
5	Draw and explain the concept of Antenna Radiation pattern **(New)**	2	CO1
6	Explain the concept of Polarization and its types**(New)**	3	CO1
	Unit – II		
	Part – A (2 Marks)		
1	Explain the characteristics of yagi-uda antenna? **(NOV 2015 - R09)**	1	CO2
2	What is Reflector antenna? What are its types **(NOV 2016 - R09)**	2	CO2
3	What is Hygens principle? (New)	2	CO2
4	What is Aperture Blocking? **(New)**	2	CO2
5	What is Babinets Principle?	2	CO2
6	What is Aperture antenna?	2	CO2
	Part – B (5 Marks)		
1	What is Yagi-uda antenna? Explain the construction and operation of it with general characteristics? **(NOV/DEC 2016-R13)**	2	CO2
2	Explain design considerations of pyramidal horn? **(JUNE /JULY 2014 –R09, NOV 2015 –R13)**	3	CO2
3	Explain the special features of parabolic reflector antenna and discuss on different types of feeds used with neat diagram? **(NOV. / DEC 2011- R09)**	3	CO2
4	Explain the operation of Cassegrain reflector antenna with its limitation **(New)**	2	CO2
5	Draw and explain the functioning of Log-periodic Antenna**(New)**	2	CO2
6	Explain in details about various frequency independent antennas and their radiation patterns **(New)**	3	CO2
7	Explain in detail about Broadcast Antennas**(New)**	2	CO2
	Unit – III		
	Part – A (2 Marks)		
1	List out the applications of patch antennas? **(NOV 2015 – R13)**	1	CO3
2	Discuss the features of microstrip antennas? **(NOV 2015 –R13)**	2	CO3
3	List out the limitation of Microstrip antennas **(New)**	2	CO3
4	List out the advantages of Microstrip antennas**(New)**	2	CO3

5	What is patch antenna? what are its types	2	CO3
6	List out various feeding methods used for patch antennas	2	CO3
	Part – B (5 Marks)		
1	With necessary illustrations explain the characteristics of Rectangular patch micro strip antenna and mention its possible applications? **(NOV / DEC 2011 – R09)**	3	CO3
2	What are micro strip patch antennas? List the advantages and limitations of it? **(NOV/DEC 2017 – R15)**	3	CO3
3	Give the geometry of Microstrip patch antenna and draw the normalized radiation pattern obtained **(New)**	3	CO3
4	Explain in detail about various feeding methods used in Micro strip patch antennas **(New)**	3	CO3
5	A rectangular microstrip antenna (RMSA) is designed at 1800 MHz on a substrate having $\varepsilon r = 2.33$, h = 1.6 mm and tan $\delta = 0.0012$. Calculate width,effective dielectric constsnt,length,input impedance,gain		
	Unit – IV		
	Part – A (2 Marks)		
1	What is a uniform linear array? **(NOV 2015 – R13)**	1	CO4
2	Differentiate broadside array and end fire array? **(May 2008 - RR, APR 2011- R09, NOV/DEC 2017- R15)**	1	CO4
3	Define array factor? **(DEC 2007-RR,NOV 2017- R15)**	1	CO4
4	What is binomial array? **(New)**	1	CO4
5	List out the advantages of Binomial array **(New)**	1	CO4
6	What are planar arrays? **(New)**	1	CO4
	Part – B (5Marks)		
1	Determine fields due to **(MAY / JUNE 2013 – R09)** A) Array of two point sources of same amplitude and in phase at distance R? B) Array of two point sources of same amplitude and opposite phase at distance R?	4	CO4
2	Compare BSA and EFA? **(NOV/DEC 2016 – R13, NOV/DEC 2017 – R15)**	3	CO4

3	What is binomial array antenna? What is the working principle? Mention its advantages & disadvantages? **(MAR 2017 – R13)**	3	CO4
4	Derive an expression for radiation pattern of broad side uniform linear array of 4 elements with $\lambda/2$ spacing, obtain its radiation pattern? **(NOV 2015 – R13)**	3	CO4
5	What are planar arrays? Explain in detail **(New)**	2	CO4
6	Synthesize the antenna array using schelkunoff polynomial method**(New)**	4	CO4
7	Give the equations for antenna array using Woodward lawson method**(New)**	3	CO4
	Unit – V		
	Part – A (2 Marks)		
1	Define wave tilt of ground wave? **(NOV 2015 – R13)**	1	CO5
2	What is Duct propagation? **(MAY 2015 – R16)**	1	CO5
3	What is sporadic E layer? **(MAY 2015 – R16)**	1	CO5
4	What are smart antennas? (New)	1	CO5
5	List out the advantages of smart antennas**(New)**	1	CO5
6	What are the applications of Smart antennas**(New)**	1	CO5
7	What is beam forming? what are its types**(New)**	1	CO5
	Part – B (5 Marks)		
1	Explain the mechanism of ionosphere propagation? **(APRIL / MAY 2011 – R09)**	3	CO5
2	**Explain the terms: (APRIL / MAY 2011- R09, NOV/ DEC 2011- R09, NOV/DEC 2017- R15)** i). Critical Frequency. ii). Maximum usable frequency. iii). Skip Distance	2	CO5
3	Explain the important features of ground wave propagation? **(NOV / DEC 2011 – R09)**	2	CO5
4	What is Skip distance? Obtain the relation between skip distance and MUF? **(JUNE /JULY2014 –R09, NOV 2015- R13)**	3	CO5
5	Explain different beam forming techniques **(New)**	4	CO5
6	Explain in detail about the advantage of adaptive beam forming	2	CO5

	compared with fixed beam forming **(New)**		
7	A high frequency radio link to be established between 2 points at a distance of 2500km on earth surface. Considering the ionosphere height to be 200km and its critical frequency 5MHz, calculate MUF for given path **(New)**	3	CO5

SOLUTIONS

PART A

UNIT-I

1. **Define isotropic source?**

   An isotropic radiator is a theoretical point source of electromagnetic or sound waves which radiates the same intensity of radiation in all directions. It has no preferred direction of radiation. It radiates uniformly in all directions over a sphere centered on the source.

2. **What is meant by Beam Area?**

BEAM AREA (OR BEAM SOLID ANGLE) Ω_A

In polar two-dimensional coordinates an incremental area dA on the surface of a sphere i the product of the length $r\,d\theta$ in the θ direction (latitude) and $r\sin\theta\,d\phi$ in the ϕ directio (longitude), as shown in Fig. 2–5.

Thus,

$$dA = (r\,d\theta)(r\sin\theta\,d\phi) = r^2\,d\Omega \qquad (1$$

where

$d\Omega$ = *solid angle* expressed in steradians (sr) or square degrees ($^\square$)
$d\Omega$ = solid angle subtended by the area dA

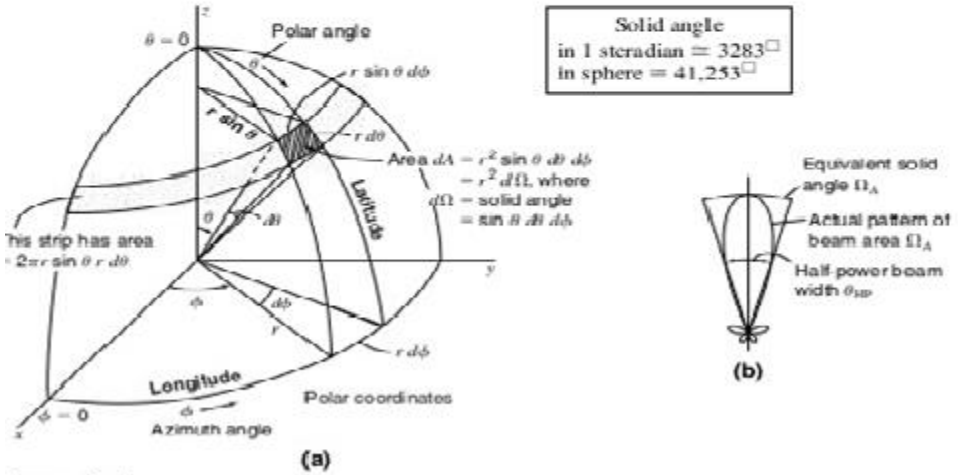
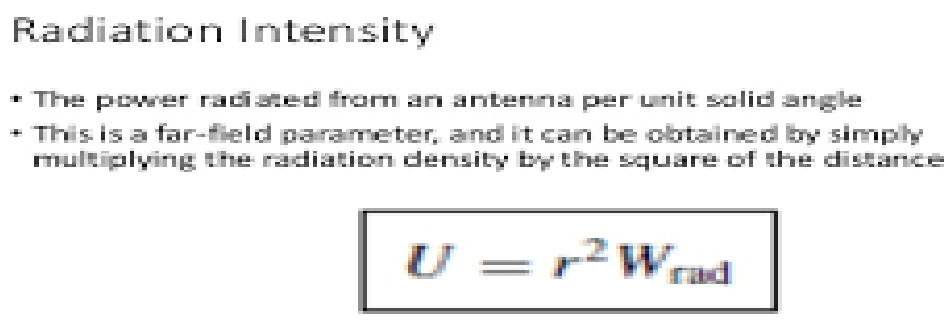


Figure 2–5
Polar coordinates showing incremental solid angle $dA = r^2\,d\Omega$ on the surface of a sphere of radius r where $d\Omega$ = solid angle subtended by the area dA. (*b*) Antenna power pattern and its equivalent solid angle or beam area Ω_A.

3. **Distinguish between far field and near field? (NOV-2015- R13)**

Non-radiative 'near-field' behaviors of electromagnetic fields dominate close to the antenna or scattering object, while electromagnetic radiation 'far-field' behaviors dominate at greater distances. Far-field E and B field strength decreases inversely with distance from the source, resulting in an inverse-square law for the radiated power intensity of electromagnetic radiation. By contrast, near-field E and B strength decrease more rapidly with distance inverse-distance squared or cubed), resulting in relative lack of near-field effects within a few wavelengths of the radiator.

4. **Define Radiation Intensity of an Antenna (New)**



5. **Define Directivity and Gain of an Antenna and give the relation between them (New)**

Directivity D is a quantitative measure of an antenna's ability to concentrate energy in a certain direction. Specifically, D is the ratio of the maximum radiation intensity Umax to the average radiation intensity Uavg

Directivity = $U_{max/UAvg}$ (dimensionless)

Is the ratio of the radiation intensity in a given direction to the radiation intensity that would be obtained if the power were radiated isotropically

G=KD

6. **Give the Friis transmission equation(New)**

The Friis Transmission Equation is used to calculate the power received from one antenna (with gain G1), when transmitted from another antenna (with gain G2), separated by a distance R, and operating at frequency f or wavelength lambda.

$$P_r = \frac{P_t G_t G_r \lambda^2}{(4\pi R)^2}$$

Where,

P_r = Power at the receiving antenna

P_t = Output power of transmitting antenna

G_t = Gain of the transmitting antenna

G_r= Gain of the receiving antenna

λ = Wavelength

R = Distance between the antennas

7. Define a Hertzian dipole? (New)

A very simple radiating element we can study is the ideal dipole, also known as Hertzian dipole and infinitesimal dipole. It is very short (length $\ll \lambda$), and as such has current uniformly distributed along its length.

UNIT V

1. Define wave tilt of ground wave? (NOV 2015 – R13)

At a point in a perfect dielectric medium close to the surface separating this medium from a medium of finite conductivity, the angle between the major axis of the polarization ellipse of a surface **wave** and the normal to the separating surface is called as wave tilting

2. What is Duct propagation? (MAY 2015 – R16)

A radio wave propagation technique that allows the transmission of UHF and VHF electromagnetic waves through the region near the tropospheric layer of atmosphere is known as duct propagation. Duct propagation allows the propagation of the signals beyond the horizon.

1. **What is sporadic E layer? (MAY 2015 – R16)**

   The term sporadic E (Es) layer refers to extremely anomalous values of ionization confined within layers of very limited thickness (a few km) occurring between 90 and 130 km, whose critical frequency is often higher than the normal E layer.

2. **What are smart antennas? (New)**

   Smart Antennas, also known as multiple antennas, adaptive array antennas, and so on is used to increase the efficiency in digital wireless communication systems. It works by taking the advantage of the diversity effect at the transceiver of the wireless system that is the source and the destination.

3. **What are the applications of Smart antennas(New)**

Applications	Description
RADAR	Phased array RADAR; air traffic control; synthetic aperture RADAR
SONAR	Source location and classification
Communications	Smart antenna systems; Directional transmission and reception; sector broadcast in satellite communications
Imaging	Ultrasonic; optical; tomographic
Geophysical Exploration	Earth crust mapping; oil exploration
Astrophysical Exploration	High resolution imaging of universe
Biomedical	Neuronal spike discrimination; fetal heart monitoring; tissue hyperthermia; hearing aids

4. **What is beam forming? what are its types(New)**

   Beamforming or spatial filtering is a signal processing technique used in sensor arrays for Adaptive beamforming is used to detect and estimate the signal of interest at Beamforming techniques can be broadly divided into two categories:.

   Switched/Fixed beam forming

   Adaptive beam forming

UNIT-II

1. Explain the characteristics of yagi-uda antenna? (NOV 2015 - R09)

Yagi-Uda antenna or aerial is a particularly popular form of antenna where directivity and gain are required. Although the Yagi has become particularly popular for television reception; it is also used in many other applications, both domestic and commercial or professional. The gain and directivity of the Yagi antenna enable improved reception by enabling better levels of signal to noise ratio to be achieved, and by reducing interference levels by only picking up signals from a given direction. For transmitting much better use of the available power is made because it is possible to focus the transmitted power on areas where it is needed. Similarly levels of general interference can be reduced to other users because the signal is not transmitted to areas where it is not needed.

2. What is Reflector antenna? What are its types (NOV 2016 - R09)

When integrated into an **antenna** assembly, the **reflector** serves to modify the radiation pattern of the **antenna**, increasing gain in a given direction. Common integrated **reflector** types are. Parabolic **reflector**, which focuses a beam signal into one point or directs a radiating signal into a beam.

3. What is Huygens principle? (New)

Huygens' principle**,** in optics, a statement that all points of a wave front of light in a vacuum or transparent medium may be regarded as new sources of wavelets that expand in every direction at a rate depending on their velocities.

4. **What is Aperture Blocking? (New)**

   Aperture blockage is normally due to shadowing by feed, sub reflector and/or support members. Deviations in reflector surfaces cause non-uniform aperture distributions, resulting in reduced gains.

5. **What is Babinets Principle? (New)**

   In physics, Babinet's principle states that the diffraction pattern from an opaque body is identical to that from a hole of the same size and shape except for the overall forward beam intensity.

6. **What is Aperture antenna? (New)**

   The aperture is defined as the area, oriented perpendicular to the direction of an incoming electromagnetic wave, which would intercept the same amount of power from that wave as is produced by the antenna receiving it.

UNIT-III

1. List out the applications of patch antennas? (NOV 2015 – R13)

Mobile communication used in mobile phones.

Medical applications in the treatment of malignant tumors

Textile antennas Wearable antennas will find use in healthcare, recreation

Defense antennas are used in airplanes and in other military applications.

Microwave integrated circuits used as an active element

2. Discuss the features of microstrip antennas? (NOV 2015 –R13)

Fabricated using micro strip techniques on a printed circuit board (PCB)

Mostly used at microwave frequencies

Antenna is connected to the the Tx/Rx through micro strip transmission lines

Micro strip antenna consists of a patch of metal foil of various shapes

Patch is made up of highly conductive material such as copper

3. List out the Limitations of Microstrip Antennas (New)

Low impedance bandwidth.

Low gain.

Extra radiation occurs from its feeds and junctions

Excitation of surface waves.

Size of micro strip antenna comes in both advantages and disadvantages but there are some applications where the size of microstrip antenna is too large to be used.

5. List out the advantages of Microstrip antennas (New)

Low profile (can even be “conformal”).

Easy to fabricate (use etching and phototlithography).

Easy to feed (coaxial cable, microstrip line, etc.) .

Easy to use in an array or incorporate with other microstrip circuit elements.

Patterns are somewhat hemispherical, with a moderate directivity (about 6-8 dB is typical).

6. What is patch antenna? what are its types

A patch antenna is a type of radio antenna with a low profile, which can be mounted on a flat surface. It consists of a planar rectangular, circular, triangular, or any geometrical sheet or "patch" of metal, mounted over a larger sheet of metal called a ground plane.

There are three types in microstrip antenna:

Microstrip patch antenna, Microstrip slot/travelling antenna and Printed dipole antenna.

7. List out various feeding methods used for patch antennas

A feedline is used to excite to radiate by direct or indirect contact. There are many different methods of feeding and four most popular methods are microstrip line feed, coaxial probe, aperture coupling and proximity coupling.

UNIT IV

1. What is a uniform linear array? (NOV 2015 – R13)

An antenna composed of a relatively large number of usually identical elements arranged in a single line or in a plane with uniform spacing and usually with a uniform feed system

2. Differentiate broadside array and end fire array?
(May 2008 - RR, APR 2011- R09, NOV/DEC 2017- R15)

An array is said to be End-fire array if the main beam is along the axis of the array. An array is said to be Broadside array if the main beam is perpendicular to the axis of the array.

3. Define array factor? (DEC 2007-RR,NOV 2017- R15)

The array factor is the complex-valued far-field radiation pattern obtained for an array of isotropic radiators located at coordinates, as determined by: where are the complex-valued excitation coefficients, and is the direction unit vector.

4. What is binomial array? (New)

A binomial array is a non-uniform antenna array for which the elements are equally spaced with unequal amplitude excitation using a specified current excitation known as binomial excitation.

5. List out the advantages of Binomial array (New)

The signal strength increases.

High directivity is obtained.

Minor lobes are reduced much.

High Signal-to-noise ratio is achieved.

High gain is obtained.

Power wastage is reduced.

Better performance is obtained.

6. What are planar arrays? (New)

A planar array provides a large aperture and may be used for directional beam control by varying the relative phase of each element.

OBJECTIVE TYPE

UNIT-I

Fill in the blanks

1. Radiation resistance dissipates an amount of power that is equal to **radiated power**
2. An isotropic radiator has the directivity of **unity**
3. The noise temperature of an antenna is equal to its **radiation resistance**
4. With the help of **tuning** method, an electrical length of the parasitic element can be adjusted
5. According to Helmholtz theorem, if the **curl** and **divergence** of the field are know at a point then any vector can be defined uniquely

Multiple choices

1. The efficiency of an antenna in terms of radiated power and ohmic losses is,

a) $\frac{wr}{wr+wl}$ $b)$ $\frac{wl}{wr+wl}$

c) $\frac{2wr}{wr+wl}$ $d)$ $\frac{2wl}{wr+wl}$

2. The variation of radiated power with an elevation angle is called

(a) Electric field pattern (b) magnetic field pattern

(c) **Power pattern** (d) none

3. The relation between antenna's size and frequency is,

(a) Directly proportional (b) **Inversely proportional**

(c) Independent of frequency (d) inversely proportional to the square of the frequency

4. If L_{eff} is an effective length and 'L' is the actual length of antenna, then the relation between effective length and actual length is,

(a) **$L_{eff}<L$** (b) $L_{eff}>L$

(c) $L_{eff}=L$ (d) $L_{eff}=3L$

5. When the directivity of an antenna increases then its beam width,

(a) Increases (b) **Decreases**

(c) Increases by 2 times (d) No effect

UNIT-II

Fill in the blanks

1. In **parasitic** elements, currents are induced due to the field in other elements.

2. The **yagi-uda** antenna with three elements including one reflector, one driven element and one director is commonly called beam antenna

3. The **E-plane sectorial horn** is obtained when tapering in done is the direction of electric field vector

4. The tapering in a gradual exponential manner **minimizes** the reflections of guided waves

5. The optimum pitch angle for the axial mode of helical antenna is at **14degrees**

Multiple choices

1. Parasitic element is capacitive in nature when,

(a) **Its length is less than resonant length** (b) Its length is greater than resonant length

(c) Its length is twice the resonant length (d) none

2. Directors in Yagi-uda antenna are----------

(a) 1 (b) 2

(c) 3 (d) **one or more**

3. Helical antenna provides----------polarization.

(a) **Circular** (b) Rectangular

(c)Elliptical (d) None of these

4. The pitch angle of helical antenna is given by,

(a) **$\alpha = \tan^{-1}\frac{S}{\prod D}$** (b) $\alpha = \tan^{-1}\frac{\prod D}{S}$

(c) $\alpha = \tan^{-1}\frac{S}{\prod}$ (d) none

5. If the flare angle symbol is small, then the area of the wave front is approximately----------aperture.

(a) Less than (b) Greater than

(c) **Equal to** (d) None

UNIT-III

Fill in the blanks

1. **Rectangular patch antenna** is one of the micro strip antennas which has a rectangular patch in it

2. **Flat sheet reflector** is the simplest form of reflector antenna

3. The angle at which two plane reflector are joined is called **included angle**

4. The paraboloid which produces sharp major lobes and smaller minor lobes is called as **microwave dish**

5. The hyperboloid reflector, whose foci coincides with the focus of the paraboloid reflector is called **cassegrain secondary reflector**

Multiple choices

1. Limitation of micro strip antennas
   - **(a) Low bandwidth and low power handling capacity**
   - (b) Low efficiency and low size
   - (c) Low weight and low gain
   - (d) none

2. The RF power is directly fed to radiating patch; such a feed method is known as
   - (a) Connecting
   - (b) **contacting**
   - (c) Non- contacting
   - (d) Non- contacting

3. Sides of the corner reflector are made----the feed to vertex spacing, to get smaller included angles
   - (a) Smaller than twice
   - (b) Larger than twice
   - (c) Smaller than thrice
   - (d) **Larger than thrice**

4. An open end of parabolic reflector is called
   - (a) **Aperture**
   - (b) hollow
   - (c) Both (a) and (b)
   - (d) none

5. Half power beam width of large circular aperture is given by
   - (a) $115\frac{\lambda}{L}$
   - (b) 115 λ
   - (c) $\mathbf{58\frac{\lambda}{D}}$
   - (d) none

UNIT-IV

Fill in the blanks

1. An array of element for which the radiation is maximum in the direction of normal to the array axis is called **broad side array**

2. Directivity of a broadside array of 5λ length is **10**

3. The binomial array has **zero** side lobe level

4. The product of the pattern of the individual antenna with its array pattern is called **principal of pattern multiplication**

5. In binomial array, the excitation of **central** elements is very strong

Multiple choices

1. An excitation value of the broad-side array is,

(a) **0** (b) 1

(c) 2 (d) 3

2. For broad-side array, null-to-null beam width is,

(a) $\sqrt{\frac{Nd}{2\lambda}}$ (b) $2\sqrt{\frac{2\lambda}{Nd}}$

(c) $\sqrt{\frac{2\lambda}{Nd}}$ (d) $\boldsymbol{\frac{2\lambda}{Nd}}$

3. Null-to-null beam width is,

(a) Less than 3dB band width (b) **Greater than 3dB band width**

(c) Equal to 3dB band width (d) not related to 3dB band width

4. Directivity of an end-fire array is,

(a) $\boldsymbol{\frac{L}{\lambda}}$ (b) $2\frac{L}{\lambda}$

(c) $\boldsymbol{4\frac{L}{\lambda}}$ (d) $5\ \frac{L}{\lambda}$

5. A three element binomial array has excitation level as,

(a) 1, 4, 1 (b) 2, 3, 2

(c) 1, 3, 1 (d) **1, 2, 1**

UNIT-V

Fill in the blanks

1. **Sky wave** propagation plays a vital role in long distance radio communication.

2. The relative permittivity of the ionosphere at radio frequencies is **less than unity**

3. The major disadvantage of omnidirectional antenna broadcast that smart antennas try to overcome in a cellular network is **co-channel interference**

4. Switched beam antenna systems break a coverage area into microsectors in order to improve **range and capacity**

5. Smart antenna system is typically implemented as an integrated approach with less hardware redundancy called as **adaptive array antenna**

Multiple choices

1. Short wave radio broadcasting for long distance communication uses

(a) Ground wave (b) **Ionosphere wave** (c) Direct wave (d) none

2. During day which layer doesn't exists

(a) D-layer (b) F_2-layer (c) **F-layer** (d) E-layer

3. Refractive index of ionized layer is

(a) $\sqrt{1+\frac{81f2}{N}}$ (b) $\sqrt{\mathbf{1-\frac{81f2}{N}}}$ (c) $\sqrt{1-\frac{81N}{f2}}$ (d) $\sqrt{1-\frac{f2}{81N}}$

4. Adaptive array systems cover a cell area with

(a) a finite number of predefined patterns or combining strategies

(b) an infinite number of patterns that are adjusted in real time

(c) dividing the 360°-cell into three 120°-microsectors

(d) dividing the 360°-cell into three 60°-microsectors

5.The smarts of a smart antenna system are chiefly derived from

(a) the multiple elements of the antenna array

(b) frequency reuse

(c) the digital signal-processing capability

(d) frequency discrimination

COMPUTER NETWORKS (21PC0CS14)

III B Tech I Semester

Academic Year: 2023-24

G.Srujana Bharathi

Assistant Professor

Dept. of CSE

Guru Nanak Institutions Technical Campus (Autonomous)

School of Engineering and Technology

Ibrahimpatnam, R R District – 501 506 (T.S)

Vision & Mission

Vision of the Institution: GURU NANAK INSTITUTIONS TECHNICAL CAMPUS

To be an internationally renowned institution in Engineering, Management, Pharmacy and related fields to produce scientists, engineers, entrepreneurs, leaders, academicians and thinkers of tomorrow with exemplary professional conduct and adherence to ethical values to serve for changing needs of industry and society.

Mission of the Institution: GNITC

M1: Imbibe soft skills, technical skills, creatively and passion in students.

M2: Develop the faculty to reach the International standards.

M3: Maintain outcome based student centric teaching learning with high academic standards and quality that promotes the analytical thinking and independent judgment.

M4: Promote research, innovation, product development by collaborating with reputed industries & reputed universities in India and abroad. Offer collaborative industry programs in emerging areas and instill the spirit of enterprising.

M5: To instill the ethical values in the faculty and students to serve the society.

Department of Electronics and Communications Engineering

Vision of the Department:

To be a premier Department of Electronics and Communication Engineering in the region by providing high quality Education, Research and Employability.

Mission of the Department:

M1: Nurture young individuals into knowledgeable, skillful, and ethical professionals in their pursuit of Electronics and Communication Engineering.

M2: Transform the students through soft skills, excellent teaching learning process and sustain high performance by innovations.

M3: Extensive MoUs with National & Foreign universities to enrich the knowledge of the students & faculty and active participation in Research..

M4: Develop industry-interaction for innovations and product design & development to provide to make the students as innovators, set up the start up units and get good placements

GURU NANAK INSTITUTIONS TECHNICAL CAMPUS (AUTONOMOUS)

	L	T	P	C
III Year B.Tech.ECE Sem-II	**3**	**1**	**0**	**4**

COMPUTER NETWORKS (18PC0CS14)

PRE-REQUISITES:

1. A course on "Programming for Problem Solving"
2. A course on "Design and Analysis of Algorithms"

COURSE OBJECTIVE:

This course is intended to equip the students with an overview of the fundamental concepts of computer networks and the protocols of the various layers

SYLLABUS:

UNIT – I

Network hardware, Network software, OSI, TCP/IP Reference models, Example Networks: Internet, ARPANET. Physical Layer: Guided Transmission media: twisted pairs, coaxial cable, Power lines, fiber optics. Wireless transmission: Electromagnetic spectrum, Radio transmission, Microwave transmission, Infrared transmission, and Light transmission.

UNIT – II

Data link layer: Design issues, framing, Error detection and correction: Hamming codes, Parity, Checksum, and Cyclic Redundancy Check. Elementary data link protocols: simplex protocol, A simplex stop and wait protocol for an error-free channel, A simplex stop and wait protocol for noisy channel. Sliding Window protocols: A one-bit sliding window protocol, A protocol using Go-Back-N, A protocol using Selective Repeat.

Medium Access sub layer: The channel allocation problem, Multiple access protocols: ALOHA, Carrier sense multiple access protocols, collision free protocols.

UNIT – III

Network Layer: Design issues, Routing algorithms: the optimality principle, shortest path algorithm, Flooding, distance vector routing, Hierarchical routing, Broadcast Routing, Multicast Routing. Congestion Control Algorithms, Quality of Service, Internetworking, the Network layer in the internet: IPv4 Protocol, IP Address, IPv6.

UNIT – IV

Transport Layer: Transport Service, Elements of Transport protocols: Addressing, Connection Establishment, Connection Release. Connection management. The Internet Transport Protocols: Introduction to UDP, Remote Procedure calls, Introduction to TCP, The TCP Service Model, The TCP Protocol, and The TCP Segment Header, The TCP Connection Establishment, TCP Connection Release

UNIT – V

Application Layer –Domain name system: The DNS Name Space, Domain Resource Records, Name Servers, Electronic Mail: Architecture Services, SMTP, the World Wide Web: Architectural Overview, HTTP, Streaming audio and video: digital audio, digtal video, streaming stored media, streaming live media, real time conferencing.

TEXT BOOK:

1.Computer Networks -- Andrew S Tanenbaum, David. j. Wetherall,5th Edition. Pearson Education/PHI

REFERENCE BOOKS:

1. An Engineering Approach to Computer Networks-S. Keshav, 2nd Edition, Pearson Education
2. Data Communications and Networking – Behrouz A. Forouzan. 3rd Edition TMH.

COURSE INFORMATION SHEET

SUBJECT: Computer Networks

PROGRAMME: **ELECTRONICS & COMMUNICATION ENGINEERING**	DEGREE: **B.TECH**
COURSE: **COMPUTER NETWORKS**	SEMESTER: **II** CREDITS: **4**
COURSE CODE: **21PC0CS14** REGULATION: **R18**	COURSE TYPE: **CORE/LAB**
COURSE AREA/DOMAIN: **COMPUTER NETWORKS**	CONTACT HOURS: **4+1 (Tutorial) Hours/Week**
CORRESPONDING LAB COURSE CODE: 21PC0CS17	LAB COURSE NAME: **COMPUTER NETWORKS LAB**

UNIT	DETAILS	HOURS
I	**UNIT -I:** Network hardware, Network software, OSI, TCP/IP Reference models, Example Networks: Internet, ARPANET. Physical Layer: Guided Transmission media: twisted pairs, coaxial cable, Power lines, fiber optics. Wireless transmission: Electromagnetic spectrum, Radio transmission, Microwave transmission, Infrared transmission, and Light transmission	12
II	**UNIT –II:** Data link layer: Design issues, framing, Error detection and correction: Hamming codes, Parity, Checksum, and Cyclic Redundancy Check. Elementary data link protocols: simplex protocol, A simplex stop and wait protocol for an error-free channel, A simplex stop and wait protocol for noisy channel. Sliding Window protocols: A one-bit sliding window protocol, A protocol using Go-Back-N, A protocol using Selective Repeat. Medium Access sub layer: The channel allocation problem, Multiple access protocols: ALOHA, Carrier sense multiple access protocols, collision free protocols.	10
III	**UNIT -III:** Network Layer: Design issues, Routing algorithms: the optimality principle, shortest path algorithm, Flooding, distance vector routing, Hierarchical routing, Broadcast Routing, Multicast Routing. Congestion Control Algorithms, Quality of Service, Internet working, the Network layer in the internet: IPv4 Protocol, IP Address, IPv6.	10
IV	**UNIT -IV:** Transport Layer: Transport Service, Elements of Transport protocols: Addressing, Connection Establishment, Connection Release. Connection management. The Internet Transport Protocols: Introduction to UDP, Remote Procedure calls, Introduction to TCP, The TCP Service Model, The TCP Protocol, and The TCP Segment Header, The TCP Connection Establishment, TCP Connection Release.	11
V	**UNIT -V:** Application Layer –Domain name system: The DNS Name Space, Domain Resource Records, Name Servers, Electronic Mail: Architecture Services, SMTP, the World Wide Web: Architectural Overview, HTTP, Streaming	10

	audio and video: digital audio, digital video, streaming stored media, streaming live media, real time conferencing.	
	TOTAL HOURS	**55**
	Tutorial Classes	**06**
	Descriptive Tests	**02**
	Classes for beyond syllabus	**03**
	Remedial Classes/NPTEL	**04**
	Total Number of Classes	**70**

Teaching Schedule/Model Lesson Plan

Subject	**(21PC0CS14) Computer Networks**
Faculty	**G.Srujana Bharathi, Assistant Professor**

Text Books (to be acquired by the Students)

Book 1	Computer Networks -- Andrew S Tanenbaum, David. j. Wetherall 5th Edition. Pearson Education/PHI

Reference Books

Book 2	An Engineering Approach to Computer Networks-S. Keshav, 2nd Edition, Pearson Education
Book 3	Data Communications and Networking – Behrouz A. Forouzan. 3rd Edition TMH.

Unit	**Topic**	**Chapters**			**No of Classes**
		Book 1	**Book 2**	**Book3**	
I	Over view of the Internet, OSI, TCP/IP reference models.	Ch 1, 2 & 3	-	-	12
II	Data link Layer	Ch 4	-	-	10
III	Network Layer	Ch 5	-	-	10
IV	Transport Layer	Ch 6	-	-	11
V	Application Layer	Ch 6, 7	-	-	10
	Contact classes for syllabus coverage				**55**
	Classes for beyond syllabus :03 **Descriptive tests:** 02 **Remedial Classes/NPTL Classes:** 04				**09**
	Tutorial classes				**06**
	Total classes				**70**

TEXT/REFERENCE BOOKS:

T/R	BOOK TITLE/AUTHORS/PUBLICATION
T	Computer Networks - Andrew S Tanenbaum, David. j. Wetherall, 5th Edition, Pearson Education/PHI
R	An Engineering Approach to Computer Networks - S.Keshav, 2nd Edition, Pearson Education
R	Data Communications and Networking – Behrouz A. Forouzan, Third Edition TMH

WEB SOURCE REFERENCES:

1	The TCP/IP Guide, by Charles M. Kozierok, Free online Resource, http://www.tcpipguide.com/free/index.htm
2	Shelly, Gary, et al. "Discovering Computers" 2003 Edition
3	Cisco Systems, Inc., (2003, March 14). CCNA: network media types. Retrieved from ciscopress.com
4	Wendell Odom, Rus Healy, Denise Donohue. (2010) CCIE Routing and Switching. Indianapolis, IN: Cisco Press
5	Kurose James F and Keith W. Ross : Computer Networking: A Top-Down Approach Featuring the Internet, Pearson Education 2005.
6	Andrew S. Tanenbaum, *Computer Networks*, Fourth Edition, Pearson Education 2006 (ISBN 0-13-349945-6).

COURSE PRE-REQUISITES:

C.CODE	COURSE NAME	DESCRIPTION	SEM
18PC0CS01	Programming for problem solving	For understanding the socket programming	I/I
18PC0CS02	Data Structures	For understanding routing algorithms, they need to know the data structures	II/I

COURSE OBJECTIVES:

This course is intended to equip the students with an overview of the fundamental concepts of computer networks and the protocols of the various layers

COURSE OUTCOMES:

At the end of this course students will demonstrate the ability to:

S.NO	DESCRIPTION
1	Describe the basic computer network technology
2	Express the functions of each layer in the OSI and TCP/IP reference model
3	Apply the skills of subnet and routing mechanisms
4	Examine the protocols of computer networks
5.	Apply the concepts of computer networks in network design and implementation

TOPICS BEYOND SYLLABUS/ADVANCED TOPICS/DESIGN:

1	High Speed Networks with wireless LANs
2	How to do network programming using java by Remote Method Invocation (RMI).
3	LAN Switching (1) Virtual LANs (2) VLAN Truncking Protocol (VTP) (3) Spanning Tree Protocol (STP) (4) Inter VLAN Routing

MICRO LESSON PLAN

Guru Nanak Institutions Technical Campus (Autonomous)
Subjective Question Bank

Academic Year : 2023-24

Subject Name with code : Computer Networks (21PC0CS14)

Class : III ECE Sec-4

Name of the Faculty Member : G.Srujana Bharathi

Blooms Taxonomy Levels (BTL)

1. Remembering
2. Understanding
3. Applying
4. Analyzing
5. Evaluating
6. Creating

Sl. No.	Questions (Select Questions from University question Bank and mention year in bracket or you may give own standard question with (new) in bracket)	BTL level (Please mention L1 or L2 or etc.)	Course Outcome (Please mention CO1 or CO2 etc.)
	Unit - I		
	Part – A (2 Marks)		
1.	List Out types Of networks?	L1	CO1
2.	Brief the Guided Transmission Media	L1	CO1
3.	What is internet? Differentiate it from intranet.	L1	CO1
4.	List out OSI/ISO reference Model& Tcp/Ip reference model layers	L1	CO1
5.	Define Network?	L1	CO1
6.	What are the applications of infrared waves?	L1	CO1
7.	Explain Coaxial Cable Types?	L1	CO1
8.	Explain Network Hard ware devices?	L1	CO1
9.	Classify the Un Guided transmission media?	L1	CO1
10.	Describe Types of Twisted Pair Cables?	L1	CO1
	Part – B (5/7 Marks)		
1	What is layered architecture? Explain about the functionalities of each layer in OSI/ISO reference model with a neat sketch.	L2	CO1
2	Explain TCP/IP reference model with a neat sketch. [May-2019]	L2	CO1
3	Describe wireless transmission with neat sketch.	L2	CO1
4	Explain guided transmission media.	L2	CO1
5	Explain about Types of Networks?	L2	CO1
6	Explain about Twisted - Pair cables with neat sketch.	L2	CO1
7	What is fiber optics? Explain fiber cables with neat sketch.	L2	CO1
8	Explain Advantages &Disadvantages of Networking?	L2	CO1
9	Explain ARPANET in detail with diagram.	L2	CO1
10	Differentiate between OSI-ISO &TCP/IP reference Model?	L2	
	Unit – II		

	Part – A (2 Marks)		
1.	Discuss the design issues of data link layer.	L1	CO2
2.	What is the purpose of Hamming code?	L1	CO2
3.	Define Collision?	L1	CO2
4.	List out Types Multiple access protocols?	L1	CO2
5.	Describe types of Error correcting Codes?	L1	CO2
6.	Explain about Elementary data link protocols:	L1	CO2
7.	Describe types of Error Detecting Codes?	L1	CO2
8.	List out types of Framing Methods?	L1	CO2
9.	What is Piggybacking? How does it useful?	L1	CO2
10.	Explain Bit Stuffing Method?	L1	CO2
	Part – B (5/7 Marks)		
1	Explain CRC Method with an Example?	L2	CO2
2	What are the design issues of the data link layer?	L2	CO2
3	Explain simplex, stop and wait protocol.	L2	CO2
4	What is piggybacking? Describe Go back 'N' and selective repeat protocols.	L2	CO2
5	What is Medium Access Control? Explain CSMA with collision detection.	L2	CO2
6	Describe Bit-Map Protocol?	L2	CO2
7	Explain Sliding Window protocol?	L2	CO2
8	Explain CSMA Protocols?	L2	CO2
9	Describe Channel Allocation Problem?	L2	CO2
10	Explain Selective Repeat Protocol?	L2	CO2
	Unit – III	L2	CO2
	Part – A (2 Marks)		
1.	What is Tunneling?	L1	CO3
2.	Explain briefly about flooding algorithm?	L1	CO3
3.	What is Crash Recovery?	L1	CO3
4.	What is Optimality Principle?	L1	CO3
5.	What are the metrics used by routing protocols?	L1	CO3
6.	Define Routing? Explain types of Routing	L1	CO3
7.	Give the advantages of hierarchical routing.	L1	CO3
8.	What is Multi casting?	L1	CO3
9.	Write the responsibilities of network layer.	L1	CO3
10.	List Out Types of Congestion Control Algorithms?		
	Part – B (5/7 Marks)		
1	Explain Distance Vector Routing Algorithm	L2	CO3
2	Explain about Link State Routing Algorithm.	L2	CO3
3	What are the characteristics of Virtual Circuit Networks?	L2	CO3
4	Describe the concepts of Shortest path routing with an example.	L2	CO3
5	Explain About Admission Control Algorithm.?	L2	CO3
6	Give the advantages of Hierarchical Routing.	L2	CO3
7	State the principle of Congestion Control. What are the congestion prevention policies?	L2	CO3
8	Explain about Quality of Service Technique?	L2	CO3
9	Describe Network layer in the internet?	L2	CO3
10	Explain IPV4 Header Format?	L2	CO3
	Unit – IV		
	Part – A (2 Marks)		

1.	Explain about Transport Layer Primitives?	L1	CO4
2.	Define Multiplexing?	L1	CO4
3.	What is Crash Recovery?	L1	CO4
4.	Define quality of service?	L1	CO4
5.	List out different services provided in TCP	L1	CO4
6.	What is Addressing?	L1	CO4
7.	Explain TCP Connection Establishment?	L1	CO4
8.	Explain TCP Connection Release?	L1	CO4
9.	Give types of Internet Transport Protocols?	L1	CO4
10.	Explain About RPC Protocol?	L1	CO4
	Part – B (5/7 Marks)		
1	Describe Transport Layer Services.	L2	CO4
2	Explain the process of Connection Establishment in Transport Layer, addressing various issues involved.	L2	CO4
3	Explain the process of Crash Recovery Mechanism in the Transport Layer.	L2	CO4
4	Explain the protocol scenarios for Establishing Connection Release using two-way army Problem	L2	CO4
5	Explain in brief about various fields of TCP Header with the help of a neat diagram.	L2	CO4
6	Describe UDP in detail.	L2	CO4
7	Explain the protocol scenarios for Establishing Connection using three-way handshake mechanisms.	L2	CO4
8	Why transport layer protocols like TCP and UDP are called end-to-end protocols? What is the difference between them?	L2	CO4
9	Explain Dynamic Host Configuration Protocol (DHCP).	L2	CO4
10	Explain about ARP and RARP Protocol.	L2	CO4
	Unit - V		
	Part – A (2 Marks)		
1	Give the HTTP message Format?	L1	CO5
2	What is DNS? Write its properties.	L1	CO5
3	What are the basic functions of email systems?	L1	CO5
4	What are the MIME content Types??	L1	CO5
5	Define Multimedia?	L1	CO5
6	What is cryptography?	L1	CO5
7	Explain MIME Header.	L1	CO5
8	Explain Streaming Audio and Video.	L1	CO5
9	Discuss about Protocols used between Mail Transfer Agents?	L1	CO5
10	Explain about digital audio?	L1	CO5
	Part – B (5/7 Marks)		
1	Describe the Architecture of Email and its services.	L2	CO5
2	Describe the Architecture of the Web.	L2	CO5
3	Explain different types of MIME.	L2	CO5
4	Write short notes on a) Static web page b) Dynamic web page.	L2	CO5
5	Explain about SMTP protocol?	L2	CO5
6	What is DNS? Explain Domain Resource Records.	L2	CO5
7	What is Real Time Conferencing? Explain H.323 & SIP.	L2	CO5
8	What is the use of DNS? Explain how it works.	L2	CO5
9	Discus about JPEG and MPEG.	L2	CO5
10	Write short notes on a) WWW b) Digital Video	L2	CO5

Guru Nanak Institutions Technical Campus (Autonomous)

Assignment Questions with Blooms Taxonomy Level (BTL)

Academic Year : 2023-24

Subject Name with code : Computer Networks (21PC0CS14)

Class : III ECE Sec-4

Name of the Faculty Member : G.Srujana Bharathi

Blooms Taxonomy Levels (BTL)

1. Remembering
2. Understanding
3. Applying
4. Analyzing
5. Evaluating
6. Creating

Sl. No.	Questions (Select Questions from University question Bank and mention year in bracket or you may give own standard question with (new) in bracket)	BTL level (Please mention L1 or L2 or etc...)	Course Outcome (Please mention CO1 or CO2 etc…)
	Unit - I		
1.	What is layered architecture? Explain about the functionalities of each layer in OSI/ISO reference model with a neat sketch.	L1	CO1
2.	Explain TCP/IP reference model with a neat sketch.	L1	CO1
3.	Describe wireless transmission with neat sketch.	L2	CO1
4.	Explain guided transmission media.	L2	CO1
5.	Explain about Types of Networks?	L2	CO1
	Unit – II		
1.	Explain CRC Method with an Example?	L2	CO2
2.	What are the design issues of the data link layer?	L2	CO2
3.	Explain simplex, stop and wait protocol.	L2	CO2
4.	What is piggybacking? Describe Go back ‘N’ and selective repeat protocols.	L2	CO2
5.	What is Medium Access Control? Explain CSMA with collision detection.	L2	CO2
	Unit – III	L3	CO2
1.	Explain Distance Vector Routing Algorithm	L2	CO3
2.	Explain about Link State Routing Algorithm.	L2	CO3
3.	What are the characteristics of Virtual Circuit Networks?	L3	CO3
4.	Describe the concepts of Shortest path routing with an example.	L3	CO3
5.	Explain About Admission Control Algorithm.?	L3	CO3
	Unit – IV		
1.	Describe Transport Layer Services.	L2	CO4
2.	Explain the process of Connection Establishment in Transport Layer, addressing various issues involved.	L2	CO4
3.	Explain the process of Crash Recovery Mechanism in the	L2	CO4

	Transport Layer.		
4.	Explain the protocol scenarios for Establishing Connection Release using two-way army Problem	L2	CO4
5.	Explain in brief about various fields of TCP Header with the help of a neat diagram.	L2	CO4
	Unit - V		
1.	Describe the Architecture of Email and its services.	L2	CO5
2.	Describe the Architecture of the Web.	L2	CO5
3.	Explain different types of MIME.	L2	CO5
4.	Write short notes on a) Static web page b) Dynamic web page.	L2	CO5
5.	Explain about SMTP protocol?	L2	CO5

TUTORIAL CLASSES

S. No.	Date	Topic delivered	HOD Sign
Tutorial- 1			
1		TCP/IP Protocol Suite	
Tutorial-2			
2		CRC Codes, Elementary Data link Layer protocols	
Tutorial -3			
3		Shortest path flooding, Distance Vector Routing Congestion control algorithms	
Tutorial -4			
4		CIDR, IMCP, ARP, RARP, DHCP	
Tutorial -5			
5		The Connection Establishment, The TCP Connection Release	
Tutorial -6			
6		The TCP Sliding Window, The TCP Congestion Control	

OBJECTIVE QUESTIONS

UNIT:I

1. The physical layer is concerned with _____
a) bit-by-bit delivery
b) process to process delivery
c) application to application delivery
d) port to port delivery
Answer: a

2. Which transmission media provides the highest transmission speed in a network?
a) coaxial cable
b) twisted pair cable
c) optical fiber
d) electrical cable
Answer: c

3. Bits can be sent over guided and unguided media as analog signal by _____
a) digital modulation
b) amplitude modulation
c) frequency modulation
d) phase modulation
Answer: a

4. The portion of physical layer that interfaces with the media access control sublayer is called _____
a) physical signalling sublayer
b) physical data sublayer
c) physical address sublayer
d) physical transport sublayer
Answer: a

5. The physical layer provides _____
a) mechanical specifications of electrical connectors and cables
b) electrical specification of transmission line signal level
c) specification for IR over optical fiber
d) all of the mentioned
Answers: d

6. In asynchronous serial communication the physical layer provides _____
a) start and stop signalling
b) flow control
c) both start & stop signalling and flow control
d) only start signaling
Answer: c

7. The physical layer is responsible for _____
a) line coding
b) channel coding
c) modulation
d) all of the mentioned

Answer: d

8. The physical layer translates logical communication requests from the _____ into hardware specific operations.
a) data link layer
b) network layer
c) trasnport layer
d) application layer
Answer: a

9. A single channel is shared by multiple signals by _____
a) analog modulation
b) digital modulation
c) multiplexing
d) phase modulation
Answer: c

10. Wireless transmission of signals can be done via _____
a) radio waves
b) microwaves
c) infrared
d) all of the mentioned
Answer: d

10.. A list of protocols used by a system, one protocol per layer, is called
a) protocol architecture
b) protocol stack
c) protocol suit
d) none of the mentioned
Answer:b

11. Network congestion occurs
a) in case of traffic overloading
b) when a system terminates
c) when connection between two nodes terminates
d) none of the mentioned
Answer:a

12. Which one of the following extends a private network across public networks?
a) local area network
b) virtual private network
c) enterprise private network
d) storage area network
Answer:b

13) The IETF standards documents are called
a) RFC
b) RCF
c) ID

d) None of the mentioned
Answer: a

14) In the layer hierarchy as the data packet moves from the upper to the lower layers, headers are
a) Added
b) Removed
c) Rearranged
d) Modified
Answer: a

15) The structure or format of data is called
a) Syntax
b) Semantics
c) Struct
d) None of the mentioned
Answer: a

16) Communication between a computer and a keyboard involves _____ transmission
a) Automatic
b) Half-duplex
c) Full-duplex
d) Simplex
Answer: d

17) The first Network
a) CNNET
b) NSFNET
c) ASAPNET
d) ARPANET
Answer: d

18) The _____ is the physical path over which a message travels
a) Ppath
b) Medium
c) Protocol
d) Route
Answer: b

19) Which organization has authority over interstate and international commerce in the communications field?
a) ITU-T
b) IEEE
c) FCC
d) ISOC
Answer: c

20) Which of this is not a network edge device?
a) PC
b) Smartphones
c) Servers
d) Switch
Answer: d.

21) A set of rules that governs data communication
a) Protocols
b) Standards
c) RFCs
d) None of the mentioned
Answer: a

22) Three or more devices share a link in _____ connection
a) Unipoint
b) Multipoint
c) Point to point
d) None of the mentioned
Answer: b

23)OSI stands for
a) open system interconnection
b) operating system interface
c) optical service implementation
d) none of the mentioned
Answer:a.

24). The OSI model has ___ layers.
a) 4
b) 5
c) 6
d) 7
Answer:d

25). TCP/IP model does not have _____ layer but OSI model have this layer.
a) session layer
b) presentation layer
c) application layer
d) both (a) and (b)
Answer:d

26). Which layer links the network support layers and user support layers
a) session layer
b) data link layer
c) transport layer
d) network layer
Answer:c

27). Which address is used in an internet employing the TCP/IP protocols?
a) physical address and logical address
b) port address

c) specific address
d) all of the mentioned
Answer:d

28). TCP/IP model was developed _____ the OSI model.
a) prior to
b) after
c) simultaneous to
d) none of the mentioned
Answer:a

29). Which layer is responsible for process to process delivery?
a) network layer
b) transport layer
c) session layer
d) data link layer
Answer:b.

30). Which address identifies a process on a host?
a) physical address
b) logical address
c) port address
d) specific address
Answer:c

Fill in the blanks

31. Coaxial cables can be used for……
Answer: Both in telephone and cable TV networks.

32. Eavesdropping is not possible in…----------
Answer: fiber optics

33. In digital data transmission baud rate is equal to ----------
Answer: Bit rate

34. In simplex transmission data can be Transmitted in ----------direction.
Answer: One

35. Data networks for the efficiency of communication reasons, uses----------
Answer: Full-duplex transmission

36. PCs connected with ----------can also be used for education, entertainment, etc.
Answer: Modem

37. The meaning of a digital channel means that the channel is ----------.
Answer: Carrying digital data.

38. Fiber optics communication system uses----------.
Answer: Full-duplex

39. A different carrier frequency is used for each channel in ----------. Multiplexing.
Answer: Frequency Division

40. The Ethernet _____ sub layer is responsible for communicating directly with the physical layer.
Answer: Media Access Control(MAC)

UNIT:II

1. The data link layer takes the packets from _____ and encapsulates them into frames for transmission.
a) network layer
b) physical layer
c) transport layer
d) application layer
Answer: a

2. Which of the following tasks is not done by data link layer?
a) framing
b) error control
c) flow control
d) channel coding
Answer: d

3. Which sublayer of the data link layer performs data link functions that depend upon the type of medium?
a) logical link control sublayer
b) media access control sublayer
c) network interface control sublayer
d) error control sublayer
Answer: b

4. Header of a frame generally contains _____
a) synchronization bytes
b) addresses
c) frame identifier
d) all of the mentioned
Answer: d

5. Automatic repeat request error management mechanism is provided by _____
a) logical link control sublayer
b) media access control sublayer
c) network interface control sublayer
d) application access control sublayer
Answer: a

6. When 2 or more bits in a data unit has been changed during the transmission, the error is called _____
a) random error
b) burst error
c) inverted error
d) double error
Answer:b

7. CRC stands for _____

a) cyclic redundancy check
b) code repeat check
c) code redundancy check
d) cyclic repeat check
Answer: a

8. Which of the following is a data link protocol?
a) ethernet
b) point to point protocol
c) hdlc
d) all of the mentioned
Answer: d

9. Which of the following is the multiple access protocol for channel access control?
a) CSMA/CD
b) CSMA/CA
c) Both CSMA/CD & CSMA/CA
d) HDLC
Answer: c

10. The technique of temporarily delaying outgoing acknowledgements so that they can be hooked onto the next outgoing data frame is called _____
a) piggybacking
b) cyclic redundancy check
c) fletcher's checksum
d) parity check
Answer: a

11. The data link layer takes the packets from _____ and encapsulates them into frames for transmission.
a) network layer
b) physical layer
c) transport layer
d) application layer
Answer:a
.

12. Which one of the following task is not done by data link layer?
a) framing
b) error control
c) flow control
d) channel coding
Answer:d

13. Which sublayer of the data link layer performs data link functions that depend upon the type of medium?
a) logical link control sublayer
b) media access control sublayer
c) network interface control sublayer
d) none of the mentioned
Answer:b

14. Header of a frame generally contains
a) synchronization bytes
b) addresses
c) frame identifier
d) all of the mentioned
Answer:d

15. Automatic repeat request error management mechanism is provided by
a) logical link control sublayer
b) media access control sublayer
c) network interface control sublayer
d) none of the mentioned
Answer:a

16. When 2 or more bits in a data unit has been changed during the transmission, the error is called
a) random error
b) burst error
c) inverted error
d) none of the mentioned
Answer:b

17. CRC stands for
a) cyclic redundancy check
b) code repeat check
c) code redundancy check
d) cyclic repeat check
Answer:a

18. Which one of the following is a data link protocol?
a) ethernet
b) point to point protocol
c) HDLC
d) all of the mentioned
Answer:d.

19. Which one of the following is the multiple access protocol for channel access control?
a) CSMA/CD
b) CSMA/CA
c) both (a) and (b)
d) none of the mentioned
Answer:c

20. The technique of temporarily delaying outgoing outgoing acknowledgements so that they can

be hooked onto the next outgoing data frame is called
a) piggybacking
b) cyclic redundancy check
c) fletcher's checksum
d) none of the mentioned
Answer:a

21Which multiple access technique is used by IEEE 802.11 standard for wireless LAN?
a) CDMA
b) CSMA/CA
c) ALOHA
d) none of the mentioned
Answer:b

22. In wireless distribution system
a) multiple access point are inter-connected with each other
b) there is no access point
c) only one access point exists
d) none of the mentioned
Answer: a

23. A wireless network interface controller can work in
a) infrastructure mode
b) ad-hoc mode
c) both (a) and (b)
d) none of the mentioned
Answer:c

Explanation:In infrastructure mode WNIC needs access point but in ad-hoc mode access point is not required.

24. In wireless network an extended service set is a set of
a) connected basic service sets
b) all stations
c) all access points
d) none of the mentioned
Answer:a

25. Mostly _____ is used in wireless LAN.
a) time division multiplexing
b) orthogonal frequency division multiplexing
c) space division multiplexing
d) none of the mentioned
Answer:b

26. Which one of the following event is not possible in wireless LAN.
a) collision detection
b) Acknowledgement of data frames
c) multi-mode data transmission
d) none of the mentioned
Answer:a

27. What is Wired Equivalent Privacy (WEP) ?
a) security algorithm for ethernet
b) security algorithm for wireless networks
c) security algorithm for usb communication
d) none of the mentioned
Answer:b

Explanation:None.

28 What is WPA?
a) wi-fi protected access
b) wired protected access
c) wired process access
d) wi-fi process access
Answer:a

29. What is internet?
a) a single network
b) a vast collection of different networks
c) interconnection of local area networks
d) none of the mentioned
Answer:b

30. To join the internet, the computer has to be connected to a
a) internet architecture board
b) internet society
c) internet service provider
d) none of the mentioned

Fill in the blanks

31. ----------is a set of rules that governs the communications between computers on a network.
Answer: Protocol

32. Each web sites is identified by the --------
Answer: URL

33. Aloha is the type of Random access protocol, It have two types one is -------- and another is----------.
Answer : Pure Aloha and Slotted Aloha

34. ---------- is a flow control protocol.
Answer: Sliding window protocol

35. Sliding Window Protocol. Sliding window protocols are --------- for reliable and sequential delivery of data frames.
Answer: data link layer protocols

36. The sliding window is also used in ----------
Answer: Transmission Control Protocol

37. --------- is an implementation of a sliding window protocol.
Answer: . Go back N protocol

38. In Selective Repeat protocol, sender window size is always same as ----------
Answer: receiver window size

39. ------- protocol uses independent acknowledgements only.
Answer: Selective repeat

40. ---------- protocols are devised so that collisions do not occur
Answer: Collision – free

Unit III

1. The network layer is concerned with _____ of data.
a) bits
b) frames
c) packets
d) bytes
Answer: c

2. Which one of the following is not a function of network layer?
a) routing
b) inter-networking
c) congestion control
d) error control
Answer: d

3. A 4 byte IP address consists of _____
a) only network address
b) only host address
c) network address & host address
d) network address & MAC address
Answer: c

4. In virtual circuit network each packet contains _____
a) full source and destination address
b) a short VC number
c) only source address
d) only destination address
Answer: b

5. Which of the following routing algorithms can be used for network layer design?
a) shortest path algorithm
b) distance vector routing
c) link state routing
d) all of the mentioned
Answer: d

6. Which of the following is not correct in relation to multi-destination routing?
a) is same as broadcast routing
b) contains the list of all destinations
c) data is not sent by packets
d) there are multiple receivers
Answer: c

7. A subset of a network that includes all the routers but contains no loops is called _____
a) spanning tree
b) spider structure
c) spider tree
d) special tree
Answer: a

8. Which one of the following algorithm is not used for congestion control?
a) traffic aware routing
b) admission control
c) load shedding
d) routing information protocol
Answer: d

9. The network layer protocol for internet is _____
a) ethernet
b) internet protocol
c) hypertext transfer protocol
d) file transfer protocol
Answer: b

10. ICMP is primarily used for _____
a) error and diagnostic functions
b) addressing
c) forwarding
d) routing
Answer: a

11. ISP exchanges internet traffic between their networks by
a) internet exchange point
b) subscriber end point

c) ISP end point
d) none of the mentioned
Answer:a

12. Which one of the following protocol is not used in internet?
a) HTTP
b) DHCP
c) DNS
d) none of the mentioned
Answer:d

13. IPv6 addressed have a size of
a) 32 bits
b) 64 bits
c) 128 bits
d) 265 bits
Answer:c

14. Internet works on
a) packet switching
b) circuit switching
c) both (a) and (b)
d) none of the mentioned
Answer:a

15. Which one of the following is not an application layer protocol used in internet?
a) remote procedure call
b) internet relay chat
c) resource reservation protocol
d) none of the mentioned
Answer:c

16. Which protocol assigns IP address to the client connected in the internet?
a) DHCP
b) IP
c) RPC
d) none of the mentioned
Answer:a

17. Which one of the following is not used in media access control?
a) ethernet

b) digital subscriber line
c) fiber distributed data interface
d) none of the mentioned
Answer:d

18. The network layer concerns with
a) bits
b) frames
c) packets
d) none of the mentioned
Answer:c

19. Which one of the following is not a function of network layer?
a) routing
b) inter-networking
c) congestion control
d) none of the mentioned
Answer:d

20. The 4 byte IP address consists of
a) network address
b) host address
c) both (a) and (b)
d) none of the mentioned
Answer:c

21. In virtual circuit network each packet contains
a) full source and destination address
b) a short VC number
c) both (a) and (b)
d) none of the mentioned
Answer:b

22. Which one of the following routing algorithm can be used for network layer design?
a) shortest path algorithm
b) distance vector routing
c) link state routing
d) all of the mentioned
Answer:d

23. Multidestination routing
a) is same as broadcast routing
b) contains the list of all destinations
c) data is not sent by packets
d) none of the mentioned
Answer:c

24. A subset of a network that includes all the routers but contains no loops is called
a) spanning tree
b) spider structure
c) spider tree
d) none of the mentioned
Answer:a

25. Which one of the following algorithm is not used for congestion control?
a) traffic aware routing
b) admission control
c) load shedding
d) none of the mentioned
Answer:d

26. The network layer protocol of internet is
a) ethernet
b) internet protocol
c) hypertext transfer protocol
d) none of the mentioned
Answer:b

27. ICMP is primarily used for
a) error and diagnostic functions
b) addressing
c) forwarding
d) none of the mentioned
Answer:a

28) Ping can
a) Measure round-trip time
b) Report packet loss
c) Report latency

d) All of the mentioned
Answer: d

29) Ping sweep is a part of
a) Traceroute
b) Nmap
c) Route
d) Ipconfig
Answer: b
Explanation: A ping sweep is a method that can establish a range of IP addresses which map to live hosts and are mostly used by network scanning tools like nmap.

30) ICMP is used in
a) Ping
b) Traceroute
c) Ifconfig
d) Both a and b
Answer: d

Fill in the blanks

31. In the ipv4, the data gram is of_____
Answers: variable length

32. The header of the datagram in the ipv4 has_____
Answer: 20 to 60 bytes

33. The network layer at the source is responsible for creating a packet from the data coming from another_____
Answer: protocol

34. A modem is a ---------- de vice.
Answer: Bidirectional

35. A network of networks is known as ----------
Answer: Internet

36. Which level is the network layer in the OSI model _____
Answer: Third

37. Data in network layer is transferred in the form of _____
Answer: Packets

38. The network layer is considered as the _____ of the network layer.
Answer: Back bone

39. The network layer contains which hardware device----------, ---------- and -------
Answer: Routers, Bridges and Switches

40. RIP stands for _____
Answer: Routing Information Protocol

Unit IV

1. Transport layer aggregates data from different applications into a single stream before passing it to _____
a) network layer
b) data link layer
c) application layer
d) physical layer
Answer: a

2. Which of the following are transport layer protocols used in networking?
a) TCP and FTP
b) UDP and HTTP
c) TCP and UDP
d) HTTP and FTP
Answer: c

3. User datagram protocol is called connectionless because _____
a) all UDP packets are treated independently by transport layer
b) it sends data as a stream of related packets
c) it is received in the same order as sent order
d) it sends data very quickly
Answer: a

4. Transmission control protocol _____
a) is a connection-oriented protocol
b) uses a three way handshake to establish a connection
c) receives data from application as a single stream
d) all of the mentioned
Answer: d

5. An endpoint of an inter-process communication flow across a computer network is called _____
a) socket
b) pipe
c) port
d) machine
Answer: a

6. Socket-style API for windows is called _____
a) wsock
b) winsock
c) wins
d) sockwi
Answer: b

7. Which one of the following is a version of UDP with congestion control?
a) datagram congestion control protocol
b) stream control transmission protocol

c) structured stream transport
d) user congestion control protocol
Answer: a

8. A _____ is a TCP name for a transport service access point.
a) port
b) pipe
c) node
d) protocol
Answer: a

9. Transport layer protocols deals with _____
a) application to application communication
b) process to process communication
c) node to node communication
d) man to man communication
Answer: b

10. Which of the following is a transport layer protocol?
a) stream control transmission protocol
b) internet control message protocol
c) neighbor discovery protocol
d) dynamic host configuration protocol
Answer: a

11) TCP is a ..... protocol.
a). stream-oriented
b). message-oriented
c). block-oriented
d). packet-oriented

Answer: a. stream-oriented

12) Which of the following is not the layer of TCP/IP protocol.
A. Physical layer
B. link layer
C. network layer
D. transport layer.

Answer: A. Physical layer

13) TCP groups a number of bytes together into a packet called a ....
A. user datagram
B. segment
C. datagram
D. packet

Answer: **B. segment**

14) The ..... of TCP/IP protocol is responsible for figuring out how to get data to its destination.
A. application layer
B. link layer
C. network layer
D. transport layer.

Answer: **C. network layer**

15) TCP is a(n) ..... transport protocol.
A. protocol delivery
B. reliable
C. best-effort delivery
D. effortless delivery

Answer: B

16) ..... is the protocol that hides the underlying physical network by creating a virtual network view.
A. Internet Protocol(IP)
B. Internet Control Message Protocol(ICMP)
C. Address Resolution Protocol(ARP)
D. Bootstrap Protocol(BOOTP)

Answer:A

17) To use the services of UDP, we need ..... socket addresses.
A. four
B. two
C. three
D. four

Answer: B

18) Which of the following is not the name of Regional Internet Registries(RIR) to administer the network number portion of IP address.
A. American Registry for Internet Numbers(ARIN)
B. Reseaux IP Europeans(RIPE)
C. Europeans Registry for Internet Numbers(ERIN)
D. Asia Pacific Network Information Center(APNIC)

Answer: C

19) UDP packets are called .....
A. user datagrams
B. segments

C. frames
D. packets

Answer: A

20) ..... addresses use 21 bits for the and 8 bits for the portion of the IP address for TCP/IP network.
A. Class A
B. Class B
C. Class C
D. Class D

Answer: C

21) UDP packets have fixed-size header of ..... bytes.
A. 16
B. 8
C. 32
D. 64

Answer: B

22) ..... messages are never sent in response to datagrams with a broadcast or a multicast destination address.
A. ICMP
B. ARP
C. IP
D. BOOTP

Answer: A

23) TCP assigns a sequence number to each segment that is being sent. The sequence number for each segment is number of the ..... byte carried in that segment.
A. first
B. last
C. middle
D. zero

Answer: A

24) ..... is responsible for converting the higher level protocol address (IP addresses) to physical network addresses.
A. Internet Protocol(IP)
B. Internet Control Message Protocol(ICMP)

C. Address Resolution Protocol(ARP)
D. Bootstrap Protocol(BOOTP)

Answer: C

25) UDP and TCP are both ..... layer protocols.
A. data link
B. network
C. transport
D. interface

Answer C

26) ..... is a process-to-process protocol that adds only port addresses, checksum error control, and length information to the data from upper layer.
A. TCP
B. UDP
C. IP
D. ARP

Answer B

27) Which of the following functions does UDP perform?
A. Process-to-process communication
B. Host-to-host communication
C. End-to-end reliable data delivery
D. Interface-to-interface communication.

Answer A

28) A port address in TCP/IP is .....bits long.
A. 32
B. 48
C. 16
D. 64

Answer C

29) When the IP layer of a receiving host receives a datagram, ...
A. delivery is complete
B. a transport layer protocol takes over
C. a header is added
D. a session layer protocol takes over

Answer: B

30) TCP/IP is a ..... hierarchical protocol suite developed before the OSI model.
A. seven-layer
B. five-layer
C. six-layer
D. four-layer

Answer: B. five-layer

Fill in the blanks

31. What are the functions of the transport layer _____
Answer: Multiplexing & De multiplexing

32. Which services are provided by transport layer _____
Answer: Error Control

33. TCP and UDP are called _____
Answer: Transport Protocols

34. Security based connection is provided by which layer_____
Answer: Transport Layer

35. Using which method in transport layer data integrity can be ensured _____
Answer: Check Sum

36. Buffer overrun can be reduced by using _____
Answer: Flow Control

37. Transport layer can identify the symptoms of overload nodes using _____
Answer: Traffic Control

38. Transport layer receives data in the form of _____
Answer: Byte Streams

39. Congestion control can control traffic entry into a telecommunications network, so to avoid _____
Answer: Congestive Collapse

40. UDP packets are called as _____
Answer: Datagram'

Unit V

1. Which is not a application layer protocol?
a) HTTP
b) SMTP
c) FTP
d) TCP
Answer: d

2. The packet of information at the application layer is called _____
a) Packet
b) Message
c) Segment
d) Frame
Answer: b

3. Which one of the following is an architecture paradigms?
a) Peer to peer
b) Client-server
c) HTTP
d) Both Peer-to-Peer & Client-Server
Answer: d

4. Application developer has permission to decide the following on transport layer side
a) Transport layer protocol
b) Maximum buffer size
c) Both Transport layer protocol and Maximum buffer size
d) None of the mentioned
Answer: c

5. Application layer offers _____ service.
a) End to end
b) Process to process
c) Both End to end and Process to process
d) None of the mentioned
Answer: a

6. E-mail is _____
a) Loss-tolerant application
b) Bandwidth-sensitive application
c) Elastic application
d) None of the mentioned
Answer: c

7. Which of the following is an application layer service?
a) Network virtual terminal
b) File transfer, access, and management
c) Mail service
d) All of the mentioned
Answer: d

8. To deliver a message to the correct application program running on a host, the _____ address must be consulted.
a) IP
b) MAC
c) Port
d) None of the mentioned
Answer: c

9. Transport services available to applications in one or another form _____
a) Reliable data transfer
b) Timing

c) Security
d) All of the mentioned
Answer: d

10. Electronic mail uses which Application layer protocol?
a) SMTP
b) HTTP
c) FTP
d) SIP
Answer: a

11) This is not a application layer protocol
a) HTTP
b) SMTP
c) FTP
d) TCP

Answer:d

12) The packet of information at the application layer is called
a) Packet
b) Message
c) Segment
d) Frame
Answer: b

13) This is one of the architecture paradigm
a) Peer to peer
b) Client-server
c) HTTP
d) Both a and b
Answer: d
Explanation: HTTP is a protocol.

14) Application developer has permission to decide the following on transport layer side
a) Transport layer protocol
b) Maximum buffer size
c) Both of the mentioned
d) None of the mentioned
Answer: c

15) Application layer offers _____ service
a) End to end
b) Process to process
c) Both of the mentioned

d) None of the mentioned
Answer: a

16) E-mail is
a) Loss-tolerant application
b) Bandwidth-sensitive application
c) Elastic application
d) None of the mentioned
Answer: c
Explanation: Because it can work with available throughput.

17) Pick the odd one out
a) File transfer
b) File download
c) E-mail
d) Interactive games
Answer: d
Explanation: Internet telephony is Loss-tolerant other applications are not.

18) Which of the following is an application layer service ?
a) Network virtual terminal
b) File transfer, access, and management
c) Mail service
d) All of the mentioned

19) To deliver a message to the correct application program running on a host, the _____ address must be consulted
a) IP
b) MAC
c) Port
d) None of the mentioned
Answer: c

20) This is a time-sensitive service
a) File transfer
b) File download
c) E-mail
d) Internet telephony
Answer: d

21) Transport services available to applications in one or another form
a) Reliable data transfer
b) Timing

c) Security
d) All of the mentioned
Answer: d

22) Electronic mail uses this Application layer protocol
a) SMTP
b) HTTP
c) FTP
d) SIP
Answer: a

23. The entire hostname has a maximum of
a) 255 characters
b) 127 characters
c) 63 characters
d) 31 characters

24. A DNS client is called
a) DNS updater
b) DNS resolver
c) DNS handler
d) none of the mentioned
View Answer Answer:b

25Servers handle requests for other domains
a) directly
b) by contacting remote DNS server
c) it is not possible
d) none of the mentioned
Answer:b
Explanation:None.

26) DNS database contains
a) name server records
b) hostname-to-address records
c) hostname aliases
d) all of the mentioned
Answer:d
Explanation:None.

27. If a server has no clue about where to find the address for a hostname then
a) server asks to the root server
b) server asks to its adjcent server
c) request is not processed
d) none of the mentioned
Answer:a

28) Which one of the following allows client to update their DNS entry as their IP address change?
a) dynamic DNS
b) mail transfer agent
c) authoritative name server
d) none of the mentioned
Answer:a

29. Wildcard domain names start with label
a) @
b) *
c) &
d) #
Answer:b

30) The right to use a domain name is delegated by domain name registers which are accredited by
a) internet architecture board
b) internet society
c) internet research task force
d) internet corporation for assigned names and numbers
Answer:d

Fill in the blanks

31. The _____ translates internet domain and host names to IP address.
Answer: Domain name system

32. Which one of the following allows a user at one site to establish a connection to another site and then pass keystrokes from local host to remote host _____
Answer: telnet

33. Application layer protocol defines _____
Answer: Syntax and semantics

34. Which one of the following protocol delivers/stores mail to receiver server _____
Answer: Simple mail transfer protocol

35. The ASCII encoding of binary data is _____--
Answer: 64 Encoding

36. _____ is an internet standard protocol for managing devices on IP network
Answer: Simple network management protocol

37. _____ is the following is not an application layer protocol
Answer: resource reservation protocol

38. _____ is a signaling communication protocol used for controlling multimedia communication sessions
Answer: session initiation protocol

39. When displaying a web page, the application layer uses the _____
Answer: HTTP protocol
40. DNS stands for _____ Answer: Domain Name System

GURU NANAK INSTITUTIONS TECHNICAL CAMPUS (Autonomous)

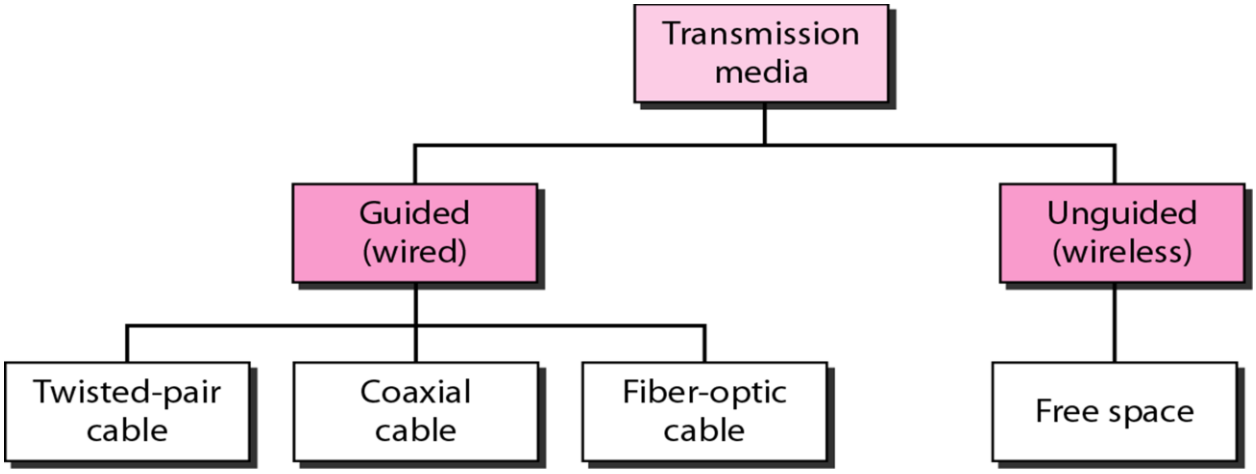
Department of Computer Science & Engineering

Question Bank (Part A with answers)

Unit-I

1. **List out types of Networks.**
   Ans: There are different types of hardware networks. They are
   - Personal Area Networks (PAN)
   - Local Area Networks (LAN)
   - Metropolitan Area Networks (MAN)
   - Wide Area Networks (WAN)
   - Internetworks (Internet)

2. **Brief the Guided Transmission Media**.
   Ans:



- Guided media, which are those that provide a conduit from one device to another, include twisted-pair cable, coaxial cable, and fiber- optic cable.

3. **What is internet? Differentiate it from intranet.**
   Ans: The Internet is a network of networks of interconnected computer networks that uses the Internet protocol suite (TCP/IP) to communicate between networks and devices. It consists of private, public, academic, business, and government networks from local to global.
   An intranet is a private computer network that uses internet protocols, network connectivity to access and share anenterprise information and operations securely with its staff.

4. **List out OSI/ISO reference Model& TCP/IP reference model layers.**

Ans: OSI/ISO reference model layers: There are seven layers. They are

- Application
- Presentation
- Session
- Transport
- Network
- Data link
- Physical

TCP/IP reference model layers: There are four layers. They are

- Application
- Transport
- Internet
- Link

5. Define Network?

Ans: A computer network is a group of computers that use a set of common communication protocols for sharing resources located on network nodes. A node is a computer network may include personal computers, servers, networking hardware, or other specialised or general-purpose hosts connected via communication network technologies, based on physically wired, optical, and wireless radio-frequency. They are identified by hostnames and network addresses.

6. What are the applications of infrared waves?

Ans: Infrared waves are used in industrial, scientific, military, commercial, and medical applications. They are

- Night-vision
- Communications
- Cooling
- Thermal-Imaging
- Thermography
- Tracking
- Hyperspectral imaging
- Spectroscopy
- Thin film metrology
- Meteorology
- Climatology
- Astronomy
- Art conservation and analysis
- Biological systems

7.Explain About Coaxial Cable?

Ans: Coaxial cable is a type of cable that has an inner conductor surrounded by an insulating layer, surrounded by a conductive shielding. Many also have an insulating outer jacket The diagram below illustrates the construction of a typical cable. Electrical signal flows through the center conductor.

8.Explain Network Hard ware devices?

Ans: The common network hardware devices are:

- **Hub** - Hubs connect multiple computer networking devices together. It also acts as a repeater. It can be used with both digital and analog data.
- **Switch** - Switches are more intelligent than hubs. A switch is a multiport device that improves network efficiency over hubs or routers because of the virtual circuit capability. it allows connections to systems like hubs or routers.
- **Router** - Router are also used to divide internal networks into two or more subnetworks.
- **Bridge** - Bridges are used to connect two or more hosts or network segments together. It is used to divide larger networks into smaller sections by sitting between two physical network segments and managing the flow of data between the two.
- **Gateway** - Gateways perform all of the functions of routers and more. Gateways normally work at the Transport and Session layers of the OSI model.
- **Modem** - Modems (modulators-demodulators) are used to transmit digital signals over analog telephone lines.
- **Repeater** -A repeater is an electronic device that amplifies the signal it receives. Repeaters work on the Physical layer.

9.Classify the Un Guided transmission media?

- Ans: transmission and reception are achieved by means of an antenna
- directional
  - transmitting antenna puts out focused beam
  - transmitter and receiver must be aligned
- omnidirectional
  - signal spreads out in all directions

can be received by many antennas

10.Describe Types of Twisted Pair Cables?

Ans: Twisted pairs can be used for transmitting either analog or digital information. Twisted-pair cabling comes in several varieties. They are

- Cat 3 - Category 3 cables consists of two insulated wires gently twisted together. It supports speed of 100-Mbps.
- Category 5 (Cat 5)- Cat 5 replaced earlier Category 3 cables. Four such pairs are typically grouped in a plastic sheath to protect the wires and keep them together. More twists result in less crosstalk and a better-quality signal over longer distances. It supports speed of 1-Gbps.
- Cat 6 or Cat 7- These categories has more stringent specifications to handle signals with greater bandwidths. They have shielding on the individual twisted pairs, as well as around the entire cable. It support speed of 10-Gbps.

Unit-II

1. **Discuss the design issues of data link layer**.
   Ans:

- **Frame synchronization:** Data are sent in blocks called frames. The beginning and end of each frame must be recognizable.

- **Flow control:** The sending station must not send frames at a rate faster than the receiving station can absorb them.
- **Error control:** Bit errors introduced by the transmission system should be corrected.
- **Addressing:** On a shared link, such as a local area network (LAN), the identity of the two stations involved in a transmission must be specified.
- **Access Control:** It is usually not desirable to have a physically separate communications path for control information. Accordingly, the receiver must be able to distinguish control information from the data being transmitted.
- **Link management:** The initiation, maintenance, and termination of a sustained data exchange require a fair amount of coordination and cooperation among stations. Procedures for the management of this exchange are required.

2. **What is the purpose of Hamming code?**
   Ans: Hamming code is a block code that is capable of detecting up to two simultaneous bit errors and correcting single-bit errors. It makes use of the concept of parity and parity bit s, which are bits that are added to data, so that the validity of the data can be checked when it is read or after it has been received in a data transmission.
3. **Define Collision?**
   Ans: Collision theory states that for a chemical reaction to occur, the reacting particles must collide with one another. ... For collisions to be successful, reacting particles must (1) collide with (2) sufficient energy, and (3) with the proper orientation.
4. **List out Types Multiple access protocols?**
   Ans: Following are the various methods to access the channel based on their time, distance and codes
   FDMA (Frequency Division Multiple Access)
   TDMA (Time Division Multiple Access)
   CDMA (Code Division Multiple Access)

5. **Describe types of Error correcting Codes?**
   Ans: There four different error-correcting codes:
   - Hamming Codes − It is a block code that is capable of detecting up to two simultaneous bit errors and correcting single-bit errors.
   - Binary Convolution Code − Here, an encoder processes an input sequence of bits of arbitrary length and generates a sequence of output bits.
   - Reed - Solomon Code − They are block codes that are capable of correcting burst errors in the received data block.
   - Low-Density Parity Check Code − It is a block code specified by a parity-check matrix containing a low density of 1s. They are suitable for large block sizes in very noisy channels.
6. **Explain about Elementary data link protocols:?**
   Ans:
   Simplex protocol
   Stop&Wait protocol
   Go-Back –N protocol
   Selective repeat protocol

7.Describe types of Error Detecting Codes?

Types of Error detection
Parity Checking.
Cyclic Redundancy Check (CRC)
Longitudinal Redundancy Check (LRC)
Check Sum.

8.List out types of Framing Methods?

Ans: The data link layer divides the stream of bits received from the network layer into manageable data units called frames.
Framing can be done in two ways:

1. Fixed Size Framing
2. Variable Size Framing
   - Fixed Size Framing:
     - In fixed-size framing, there is no need for defining the boundaries of the frames; the size itself can be used as a delimiter.

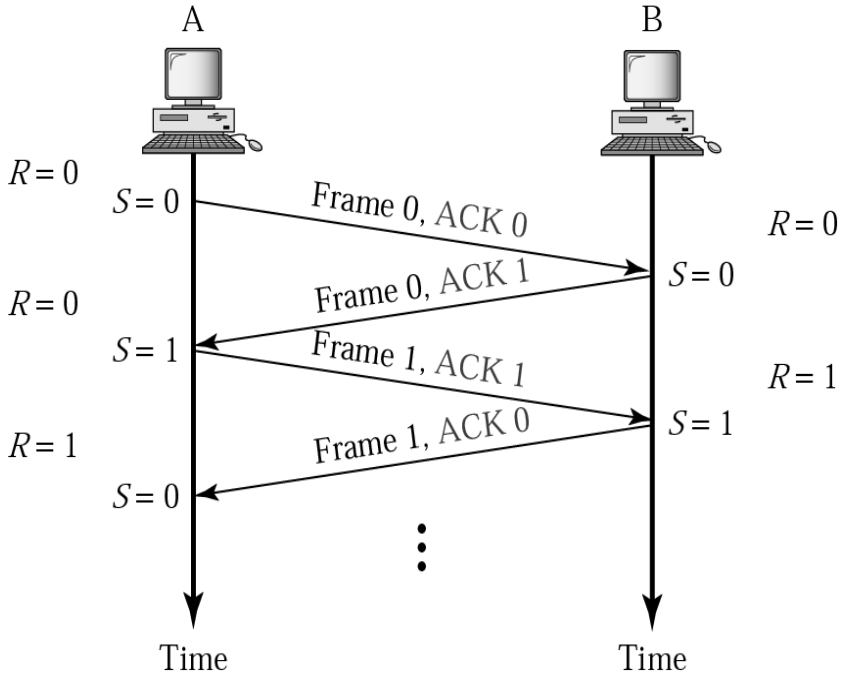
     Ex: ATM Cell which is of 53Bytes.

   - Variable-Size Framing:
     - In variable-size framing, we need a way to define the end of the frame and the beginning of the next.

9.What is Piggybacking? How does it useful?

Ans: **Piggy Backing:**

- A method to combine a data frame with ACK.
- Station A and B both have data to send.
- Instead of sending separately, station A sends a data frame that includes an ACK. Station B does the same thing.
- Piggybacking saves bandwidth.



10.Explain Bit Stuffing Method?

Ans: Bit stuffing is used for various purposes, such as for bringing bit streams that do not necessarily have the same or rationally related bit rates up to a common rate, or to fill buffers or frames. The location of the stuffing bits is communicated to the receiving end of the data link, where these extra bits are removed to return the bit streams to their original bit rates or form. Bit stuffing may be used to synchronize several channels before multiplexing or to rate-match two single channels to each other. he transmitted bit sequence "01111110" containing six adjacent 1 bits is the Flag byte. Bit stuffing ensures

that this pattern can never occur in normal data, so it can be used as a marker for the beginning and end of the frame without any possibility of being confused with normal data.[

Unit-III

1. **What is Tunnelling?**

   Ans: A tunneling is a communication protocol that allows movement of data from one network to another. It involves allowing private network communications to be sent across a public network (such as the Internet) through a process called encapsulation.

2. **Explain briefly about flooding in computer networks?**

   Ans: Flooding is a technique which requires no network information like topology, load condition , cost of diff. paths. Every incoming packet to a node is sent out on every outgoing like except the one it arrived on.

   Characteristics –

   - All possible routes between Source and Destination is tried. A packet will always get through if path exists
   - As all routes are tried, there will be atleast one route which is the shortest
   - All nodes directly or indirectly connected are visited

   Limitations –

   - Flooding generates vast number of duplicate packets
   - Suitable damping mechanism must be used

3. **What is Crash Recovery?**

   Ans: Crash recovery is the process by which the database is moved back to a consistent and usable state. This is done by rolling back incomplete transactions and completing committed transactions that were still in memory when the crash occurred . ... A hardware failure such as memory, disk, CPU, or network failure.

4. **What is Optimality Principle?**]

   Ans: optimality principle states about optimal routes without regard to network topology or traffic. It states that if router J is on the optimal path from router I to router K, then the optimal path from J to K also falls along the same route.

5. **What are the metrics used by routing protocols?**

   Ans: Router metrics can contain any number of values that help the router determine the best route among multiple routes to a destination. A router metric typically based on information like path length, bandwidth, load, hop count, path cost, delay, MTU, reliability and communications cost.

6. **Define Routing? Explain types of Routing.**

   Ans: Routing is a process performed by network layer (devices) in order to deliver the packets by choosing an optimal path from source machine to destination machine.

   There are 3 types of routing:

   1. Static routing: Static routing is a process of adding routes manually in routing table.

   2. Default Routing: In default routing, router is configured to send all packets towards a single router. It doesn't matter to which network the packet belongs, it is forwarded out to router which is configured for default routing.

   3. Dynamic Routing – Dynamic routing makes automatic adjustment of the routes according to the current state of the route in the routing table.

7. **Give the advantages of hierarchical routing.**

Ans: Hierarchical routing is the procedure of arranging routers in a hierarchical manner. A good example would be to consider a corporate intranet. Most corporate intranets consist of a high speed backbone network. Connected to this backbone are routers which are in turn connected to a particular workgroup. These workgroups occupy a unique LAN. The reason this is a good arrangement is because even though there might be dozens of different workgroups, the span (maximum hop count to get from one host to any other host on the network) is 2. Even if the workgroups divided their LAN network into smaller partitions, the span could only increase to 4 in this particular example.

Considering alternative solutions with every router connected to every other router, or if every router was connected to 2 routers, shows the convenience of hierarchical routing. It decreases the complexity of network topology, increases routing efficiency, and causes much less congestion because of fewer routing advertisements. With hierarchical routing, only core routers connected to the backbone are aware of all routes. Routers that lie within a LAN only know about routes in the LAN. Unrecognized destinations are passed to the default route.

8. **What is Multi casting?**

Ans: Multicast is a method of group communication where the sender sends data to multiple receivers or nodes present in the network simultaneously.

- Multicasting is a type of one-to-many and many-to-many communication as it allows sender or senders to send data packets to multiple receivers at once across LANs or WANs.
- It helps in minimizing the data frame of the network.
- Multicasting works in similar to Broadcasting.
- Multicasting allows a single transmission that can be split up among the multiple users; consequently, this reduces the bandwidth of the signal.

9. **Write the responsibilities of network layer.**

Ans: The network layer is responsible for delivery of data packets from the source to the destination across multiple hops or links.

The functions are

- The network layer accepts data from the transport layer, divides and encapsulates it into packets and sends it to the data link layer. The reverse procedure is done during receiving data.
- It also addresses messages and translates logical addresses (i.e., IP addresses) into physical addresses (i.e., MAC addresses).
- The network layer is responsible for routing packets from the source host to the destination host.
- Many networks are partitioned into sub-networks or subnets. The network layer controls the operations of the subnets.

10. **List Out Types of Congestion Control Algorithms?**

Ans: Too many packets present in (a part of) the network causes packet delay and loss that degrades performance. This situation is called congestion.

The network and transport layers share the responsibility for handling congestion.There are different approaches to congestion control. they are

Traffic-Aware Routing

Admission control

Traffic Throttling
Load Shedding

Unit-IV

1. **Explain about Transport Layer Primitives**?

Ans: There are five types of service primitives:

1. LISTEN : When a server is ready to accept an incoming connection it executes the LISTEN primitive. It blocks waiting for an incoming connection.
2. CONNECT : It connects the server by establishing a connection. Response is awaited.
3. RECIEVE: Then the RECIEVE call blocks the server.
4. SEND : Then the client executes SEND primitive to transmit its request followed by the execution of RECIEVE to get the reply. Send the message.
5. DISCONNECT : This primitive is used for terminating the connection. After this primitive one can't send any message. When the client sends DISCONNECT packet then the server also sends the DISCONNECT packet to acknowledge the client. When the server package is received by client then the process is terminated

2. **Define Multiplexing?**

Ans: Multiplexing is the process of combining multiple signals into one signal, over a shared medium. If analog signals are multiplexed, it is Analog Multiplexing and if digital signals are multiplexed, that process is Digital Multiplexing

3. What is Crash Recovery?

Ans: Crash recovery is the process by which the database is moved back to a consistent and usable state. This is done by rolling back incomplete transactions and completing committed transactions that were still in memory when the crash occurred (Figure 1). ... A hardware failure such as memory, disk, CPU, or network failure.

4. **Define quality of service?**

Ans: Quality of Service (QoS) is a set of technologies that work on a network to guarantee its ability to dependably run high-priority applications and traffic under limited network capacity. ... Measurements of concern to QoS are bandwidth (throughput), latency (delay), jitter (variance in latency), and error rate

5. **List out different services provided in TCP.**

Ans: The Transmission Control Protocol is the most common transport layer protocol. It works together with IP and provides a reliable transport service between processes using the:

1. Process-to-Process Communication TCP provides process to process communication, i.e, the transfer of data takes place between individual processes executing on end systems. This is done using port numbers or port addresses. Port numbers are 16 bit long that help identify which process is sending or receiving data on a host.
2. Stream oriented this means that the data is sent and received as a stream of bytes(unlike UDP or IP that divides the bits into datagram's or packets). However, the network layer, that provides service for the TCP, sends packets of information not streams of bytes. Hence, TCP groups a number of bytes together into a *segment* and adds a header to each of these segments and then delivers these segments to the network layer. At the network layer, each of these segments are encapsulated in an IP packet for transmission. The TCP header has information that is required for control purpose which will be discussed along with the segment structure.
3. Connectionorientedservice –

Unlike UDP, TCP provides connection oriented service. It defines 3 different phases:

- Connection establishment

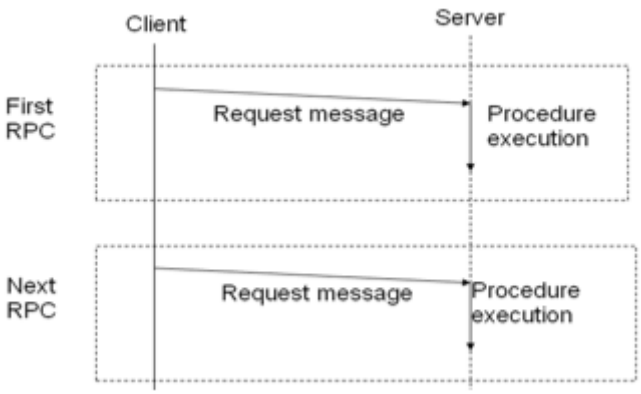
- Data transfer
- Connection termination

6. **What is Addressing?**
   Ans: An IPv6 anycast address is an address that is assigned to more than one interface (typically belonging to different nodes), with the property that a packet sent to an anycast address is routed to the "nearest" interface having that address, according to the routing protocols' measure of distance
7. **Explain TCP Connection Establishment?**
   Ans: To establish a connection, TCP usesa three-way handshake. Before a client attempts to connect with a server, the server must first bind to and listen at a port to open it up for connections: this is called a passive open. ... ACK: Finally, the client sends an ACK back to the server.
8. **Explain TCP Connection Release?**
   Ansr: the normal way of terminating a TCP connection is by using the graceful TCP connection release. This mechanism uses the FIN flag of the TCP header and allows each host to release its own direction of data transfer. ... The first path is when the host receives a segment with sequence number x and the FIN flag set.
9. **Give types of Internet Transport Protocols?**
   Transmission Control Protocol (TCP
   Internet Protocol (IP)
   User Datagram Protocol (UDP)
   Post office Protocol (POP)
   Simple mail transport Protocol (SMTP)
   File Transfer Protocol (FTP)
   Hyper Text Transfer Protocol (HTTP)
   Hyper Text Transfer Protocol Secure (HTTPS)

10. Explain About RPC Protocol?

Ans: In distributed computing a remote procedure call (RPC) is when a computer program causes a procedure (subroutine) to execute in another address space (commonly on another computer on a shared network), which is coded as if it were a normal (local) procedure call, without the programmer explicitly coding the details for the remote interaction.That is, the programmer writes essentially the same code whether the subroutine is local to the executing program, or remote.

Based on the needs of different systems, several communication protocols have been proposed for use in RPC which are mentioned below:



Unit-V

1. **Give the HTTP message Format?**

   Ans: HTTP Message is used to show how data is exchanged between the client and the server. It is based on client-server architecture. An HTTP client is a program that establishes a connection to a server to send one or more HTTP request messages. An HTTP server is a program that accepts connections to serve HTTP requests by sending an HTTP response messages.

   ` HTTP-message = Request | Response ; HTTP/1.1 messages

2. **What is DNS? Write its properties.**

   Ans: The domain name system (DNS) connects URLs with their IP address. With DNS, it's possible to type words instead of a string of numbers into a browser, allowing people to search for websites and send emails using familiar names. When you search for a domain name in a browser, it sends a query over the internet to match the domain with its corresponding IP. Once located, it uses the IP to retrieve the website's content. Most impressively, this whole process takes just milliseconds.

3. **What are the basic functions of email systems?**

   Discussing Business Decisions.
   Evidence in court.
   Get your attachments right. The most common mistake in emailing is clicking "reply all" when you meant to click "reply". ...
   Limit forwarding and pointless email threads. ...
   Try to see the big picture.

4. **What are the MIME content Types?**

   Ans:

Extension	Kind of document	MIME Type
.arc	Archive document (multiple files embedded)	**application**/x-freearc
.avi	AVI: Audio Video Interleave	video/x-msvideo
.azw	Amazon Kindle eBook format	**application**/vnd.amazon.ebook
.bin	Any kind of binary data	**application**/octet-stream

5. **Define Multimedia?**

Ans: Multimedia is a representation of information in an attractive and interactive manner with the use of a combination of text, audio, video, graphics and animation. In other words we can say that Multimedia is a computerized method of presenting information combining textual data, audio, visuals (video), graphics and animations. For examples: E-Mail, Yahoo Messenger, Video Conferencing, and Multimedia Message Service (MMS).

Multimedia as name suggests is the combination of Multi and Media that is many types of media (hardware/software) used for communication of information.

6. **What is cryptography?**

   Ans: Cryptography, or cryptology (from Ancient Greek: κρυπτός, romanized: kryptós "hidden, secret"; and γράφειν graphein, "to write", or -λογία -logia, "study", respectively), is the practice and study of techniques for secure communication in the presence of third parties called adversaries.

7. **Explain MIME Header?**

   The MIME stands for Multi-Purpose Internet Mail Extensions. As the name indicates, it is an extension to the Internet email protocol that allows it's users to exchange different kinds of data files over the Internet such as images, audio, and video. The MIME is required if text in character sets other than ASCII.

8.Explain Streaming Audio and Video

Streaming audio or video is delivered by a streaming server, which can deliver a constant flow of audio and/or video across a network that might be slow or congested. It is much like watching television with an antenna; you will receive only the video that you will be watching immediately. In contrast, video files that reside on a web server will be downloaded for viewing, instead of streamed. Viewers will need to wait for enough of the video to be downloaded before they can view it. This can be a preferable means of transmission if you want to preserve the quality of your video for all viewers

9.Discuss about Protocols used between Mail Transfer Agents?

Email or the SMTP SMTP is the protocol for transferring electronic mail. RFC 5321 describes the protocol for the use of sending mail between mail servers also referred to as mail transfer agents. SMTP has a dedicated well-known port number 25. It is not the protocol for collecting mail by a user.

10.Explain about digital audio?

Digital audio is a representation of sound recorded in, or converted into, digital form. In digital audio, the sound wave of the audio signal is typically encoded as numerical samples in a continuous sequence. For example, in CD audio, samples are taken 44,100 times per second, each with 16-bit sample depth. Digital audio is also the name for the entire technology of sound recording and reproduction using audio signals that have been encoded in digital form..

In a digital audio system, an analog electrical signal representing the sound is converted with an analog-to-digital converter (ADC) into a digital signal, typically using pulse-code modulation (PCM). This digital signal can then be recorded, edited, modified, and copied using computers, audio playback machines, and other digital tools. When the sound engineer wishes to listen to the recording on headphones or loudspeakers (or when a consumer wishes to listen to a digital sound file), a digital-to-analog converter (DAC) performs the reverse process, converting a digital signal back into an analog signal, which is then sent through an audio power amplifier and ultimately to a loudspeaker.

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HANDBOOK OF DIGITAL SIGNAL PROCESSING (21PC0EC16)

B.TECH. [III/ II]

Academic Year: 2023-2024

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHOOL OF ENGINEERING AND TECHNLOGY

HANDBOOK OF

DIGITAL SIGNAL PROCESSING (21PC0EC16)

Syllabus:

UNIT	DETAILS
I	**INTRODUCTION TO DISCRETE TIME SIGNALS AND SYSTEMS:** Discrete time signals: Sequences; representation of signals on orthogonal basis; Sampling and reconstruction of signals; Discrete systems attributes, Application of DSP, Z-Transform, Analysis of LSI systems, frequency Analysis, Inverse Systems
II	**DISCRETE FOURIER TRANSFORM AND FAST FOURIER TRANSFORM** **Discrete Fourier Transforms**: Properties of DFT, Linear Convolution of Sequences using DFT, Computation of Convolution Over-Lap Add Method, Over-Lap Save Method. **FastFourierTransforms(FFT)** – Radix-2, Decimation-in-Time and Decimation-in-Frequency FFT Algorithms, Inverse FFT, and FFT with General Radix-N.
III	**FIR Digital Filters** Characteristics of FIR Digital Filters, Frequency Response, Design of FIR Digital filters: Fourier Method, Window method, Park-McClellan's method.
IV	**IIR Filters** Design of IIR analog filters – Butterworth and Chebyshev, Elliptic Approximations, Design of IIR Digital Filters from Analog Filters by using Impulse Invariant Techniques, Bilinear Transformation Method, Spectral Transformation: Low pass, Band pass, Band stop and High pass filters. Comparison of FIR and IIR filters.
V	**Finite Word length Effects and Multirate Signal Processing** Effect of finite register length in FIR filter design. Parametric and non-parametric spectral estimation. Introduction to multirate signal processing, Decimation, Interpolation, Sampling Rate Conversion

COURSE INFORMATION SHEET

Programme: Electronics and Communication Engineering	Degree: B. Tech
Course: Digital Signal Processing	Semester: III - II Sem Credits: 4
Course Code: 18PC0EC16 Regulation: R18	Course Type: Core
Course Area/Domain: Signal Processing	Contact Hours: 3+1(Tutorial) Hours/Week
Corresponding Lab Course Code: 18PC0EC18	DSP Lab

UNIT	DETAILS	HOURS
I	**Introduction to Discrete time signals and Systems** Discrete time signals: Sequences; representation of signals on orthogonal basis; Sampling and reconstruction of signals; Discrete systems attributes, Application of DSP, Z-Transform, Analysis of LSI systems, frequency Analysis, Inverse Systems	**10**
II	**Discrete Fourier Transform and Fast Fourier Transform** Discrete Fourier Transforms: Properties of DFT, Linear Convolution of Sequences using DFT, Computation of Over-Lap Add Method, Over-Lap Save Method. Fast Fourier Transforms: Fast Fourier Transforms (FFT) – Radix-2 Decimation-in-Time and Decimation-in-Frequency FFT Algorithms, Inverse FFT, and FFT with General Radix-N.	**11**
III	**FIR Digital Filters** Characteristics of FIR Digital Filters, Frequency Response, Design of FIR Digital filters: Fourier Method, Window method, Park-McClellan's method.	**10**
IV	**IIR Filters** Design of IIR analog filters – Butterworth and Chebyshev, Elliptic Approximations, Design of IIR Digital Filters from Analog Filters by using Impulse Invariant Techniques, Bilinear Transformation Method, Spectral Transformation: Low pass, Band pass, Band stop and High pass filters. Comparison of FIR and IIR filters.	**10**
V	**Finite Word length Effects and Multirate Signal Processing** Effect of finite register length in FIR filter design. Parametric and non-parametric spectral estimation. Introduction to multirate signal processing, Decimation, Interpolation, Sampling Rate Conversion.	**08**
Total Hours		49
Tutorial Classes*		12
Special Descriptive Tests		02
Classes for beyond syllabus*		03
Remedial Classes/NPTL		04
Total Number of Classes*		**70**

UNIT-I

2 Marks:

1) What are the applications of digital signal processing? (2 marks) (March 2017)
2) Explain region of convergence and its properties. (3 marks) (March 2017)
3) Define decimation and interpolation. (2 marks) (November 2016)
4) State linear and static system with example. (3 marks) (November 2016)
5) Write four advantages of digital signal processing over analog signal Processing? (2 marks) (May 2016)
6) Show that the frequency response of a discrete system is a periodic function of frequency. (3 marks) (May 2016)
7) Show that $\delta(n) = u(n) - u(n-1)$. (2marks) (April 2018)
8) Find the z-transform of $f(n) = n^2u(n)$ (3marks) (April 2018)
9) Define energy and power signals. (May 2019)
10) Define Z-transform and state any three properties of ROC. (May 2019)

5 Marks:

1) With neat block diagram explain Digital signal Process and list out the advantages and draw backs. (May 2019)
2) Determine the impulse response h(n) for the system described by the second order difference equation y (n) – 4 y (n-1) + 4 y (n-2) = x (n-1) (March 2017)
3) Find the system function and impulse response of the system described by the difference equation $y(n) = x(n) + 2x(n-1) - 4x(n-2) + x(n-3)$. (May 2019)
4) Find the magnitude and phase response for the system characterized by the difference equation y (n) = x (n) + x (n-1) + x (n-2) (March 2017)
5) Check the following filter for time invariant, causal and linear
   i) y (n) = (n-1) x^2 (n+1)
   ii) y(n) = n^2 x (n-2) (March 2017)
6) Draw the structures of cascade and parallel realizations of

   $$H(z) = \frac{(1-z^{-1})}{\left(1-\frac{1}{2}z^{-2}\right)\left(1-\frac{1}{8}z^{-1}\right)}$$

   (March 2017 Nov. 2020)
7) If y(n) = 12x(n-1) + 11x(n-2), Find whether given system is time variant or not?. (November 2016)

8) Find the frequency response of 1st order system y(n) = x(n) + ay(n-1).

(November 2016)

9) y(n)-3y(n-1) – 4y(n-2) = 0 determine zero-input response of the system; Given y(-2) =0 and y(-1) =5 (November 2016)

10) Obtain the cascade and parallel form realization for the system

$y(n) = -0.1\, y(n-1) + 0.2\, y(n-2) + 3x(n) + 3.6x(n-1) + 0.6\, x(n-2)$. (November 2016)

11) Test the following systems for linearity, Time invariance, causality and stability

y(n) = sin(2npif/F)x(n) (May 2016)

12) A digital system is characterized by the following difference equation:

Y(n) = x(n)+ay(n-1). Assuming that the system is relaxed initially, determined its impulse response. (May 2016)

13) By taking an example compute DFT by using overlap save method. (May 2016)

14) A causal system is represented by the following difference equation:

y(n)+(1/4)y(n-1) = x(n)+(1/2)x(n-1). Find the system transfer function H(z), unit sample response, magnitude and phase function of the system. Determine direct form I and II for the second order filter given by:

$Y(n)=2bcosw_o y(n-1)-b^2 y(n-2)+x(n)-bcosw_o y(n-1)$ (May 2015)

15) Determine the range of values of 'n' for which an LTI system represented below is stable,

$h[n] = a^n$ for $n \geq 0$

= 0 otherwise (June 2014)

16) Write whether an LTI system with an impulse response represented below is stable or not? Justify.

$h[n] = 3^n u[-n-1]$ (June 2014)

17) Write whether an LTI system with an impulse response represented below is causal or not? Justify.

h[n] =u[n+2]-u[n-2] (June 2014, Nov. 2020)

18) Write a short note on Time and Frequency domain input-output relationships of an LTI system. (Dec 2013)

19) An LTI system is characterized by its impulse response $h(n) = (½)^n u(n)$. Determine the spectrum and energy density spectrum of the output signal when the system is excited by the signal $x(n) = (¼)^n u(n)$. (Dec 2013)

20) a) An LTI system is characterized by an impulse response

$$h(n) = \left(\frac{3}{4}\right)^n u(n)$$

Find the step response of the system. Also, evaluate the output of the system at n=±5.

(April 2018)

21) Consider a discrete time system characterized by the following input-output relationship $(n) = x(n-2) - 2x(n-17)$. Determine whether the system is memory less, time-invariant, linear, causal and stable. (April 2018)

22) Given the difference equation $y(n) + b^2 y(n-2) = 0$ for n≥0 and |b|<1. With initial conditions y(-1)=0 and y(-2)=-1, show that

$y(n) = b^{n+2}\cos(\frac{n\pi}{2})$ (April 2018)

23) Find the z-transform of the sequence f(n) defined below: (April 2018)

$$f(n) = \begin{cases} 3^n & n < 0 \\ (\frac{1}{3})^n & n = 0,2,4 \ldots \\ \left(\frac{1}{2}\right)^n & n = 1,3,5 \ldots \end{cases}$$

24) Discuss direct form-I and direct form-II IIR realization structures in detail with necessary flow graphs. (Nov. 2020)

25) Define an LSI system and show that the output of an LSI system is given by the convolution of input sequence and impulse response of the system. (August 2021)

26) Derive an expression for a parsevals relation for discrete time periodic signals. (August 2021)

UNIT-II

2 marks:

1) What is zero padding? What are its uses? (2 marks) (March 2017, May 2019)
2) State and prove time shifting property of DFT. (3 marks) (March 2017)
3) If x(n)= $cos\frac{\Pi}{3}n$, find spectra of the signal? (2 marks) (November 2016)
4) How many multiplications and additions are required to compute N-point DFT using radix – 2 FFT? (3 marks) (November 2016)
5) Give the relation between DTFT and Z- Transform. (2 marks) (May 2016)
6) Distinguish between linear convolution and circular convolution. (3 marks) (May 2016)
7) State and prove the any three properties of DFT.(2marks)(April2018)
8) What is the basic operation of DIF algorithm? (3marks)(April2018)
9) Define twiddle factor and give its values for N=4. (May 2019)

5 Marks

1) Determine the 8 point DFT of the sequence

X(n) = $\begin{cases} 1; & -4 \le n \le 4 \\ 0; & otherwise \end{cases}$

(March 2017, Nov. 2020)

2) Compare overlap-save method and overlap-add method. (March 2017)
3) Compute the DFT of the sequence x[n] = {1, 2, 3, 4, 4, 3, 2, 1} using DIF FFT algorithm. (May 2019)
4) How the computational speed of FFT algorithm has been improved over DFT. (May 2019)
5) Perform Linear convolution of the two sequences x(n) = {1, 2, 3, -1, -2, -3, 4, 5, 6,2,1,3,5} and h(n) = {2, 1, -1} using Over-lap save method. (May 2019)
6) Compute 4-point DFT of a sequence x (n) = { 0,1,2,3} using DIT algorithm (March 2017, Nov 2020)
7) Find the IDFT of the sequence using DIF algorithm X (k) = {10, -2-j2, -2, -2+j2} (March 2017)
8) Explain all properties of DTFT. (Nov 2016)
9) Find the DFT of a sequence x(n)= {1,1,0,0} and find the IDFT of Y(k)={1,0,1,0} (Nov 2016)
10) Explain Radix – 2. Decimation in time FFT algorithm with example. (Nov 2016)
11) Compute the circular convolution of the sequences

$X_1(n) = \{1,2,0,1\}$ and

$X_2(n) = \{2,2,1,1\}$ using DFT approach and concentric circles method.

(May 2016)

12) What is FFT? Calculate the number of multiplications needed in the calculation of DFT using FFT algorithm with 32 point sequence. (May 2016)

13) Prove the following properties

$x^*(n) \rightarrow X^*((-K))_N R_N(K)$

$x^*((-n))_N R_N(n) \rightarrow X_{ep}(k) = \frac{1}{2}[X(K)_N + X^*(-K)_N]R_N(K)$ (May 2016)

14) Compute FFT for the sequence

$x(n) = \{1,0,1,1,0,1,1,1\}$ (May 2016)

15) State and prove the following properties of DFT:

(a) Linearity

(b) Frequency shifting (May 2015)

16) Explain the following

(a) Overlap Add Method (August 2021)

(b) Overlap Save Method (May 2015)

17) Develop the DIF FFT algorithm for N=8. Using the resulting signal flow graph compute the 8-point DFT of the sequence x(n) = sin (pi/2 n), $0 \leq n \leq 7$. (May 2015)

18) If $x_2(n) = x_1(-n)$ without performing FFT find $X_2(k)$ using $X_1(k)$. (May 2015)

19) Perform Linear convolution of the $x_1[n]$ and $x_2[n]$ sequences using Over-lap add method

$x_1[n] = \{3,-1,0,1,2,3,0,1,1,2\}$ and $x_2[n] = \{1, 1, 1\}$ (June 2014)

20) Obtain the relationship between DTFT and DFS. (June 2014)

21) Compute the DFT of the sequence $x[n] = \{1,2,3,4,3,4,1,2\}$ using DIT FFT algorithm. Write the signal involved. (June 2014)

22) Compute IDFT of $X(k) = \{4,-1,0,-1\}$ using FFT techniques. (June 2014)

23) Discuss the procedure of computing linear convolution using Over-lap add method. (Dec 2013)

24) Perform Linear convolution of the two sequences $x(n) = \{1, 2, 3, -1, -2, -3, 4, 5, 6\}$ and $h(n) = \{2, 1, -1\}$ using Over-lap add method. (Dec 2013)

25) Give the general procedure of computing FFT using DIF algorithm and develop the basic butterfly structure and necessary equations. (Dec 2013)

26) How the computational speed of FFT algorithm has been improved over DFT.

(Dec 2013)

27) Find the IDFT of the sequence X(k) given below
X(K)={1,0,0,j,0,-j,0,0} (April 2018)

28) Obtain the 10 point DFT of the sequence $x(n) = \delta(n) + 2\delta(n-5)$ (April 2018)
Find the IDFT of the sequence X(k)={20,-5.828-j2.414,0,-0.712-j0.414,0,-0.172+j0.414,0,-5.828+j2.414} using DIT-FFT algorithm. (April 2018)

29) Using FFT and IFFT, determine the output of system if input x(n)={2,2,4} and impulse response h(n)={1,1} (April 2018)

30) Compute circular convolution for X(n)= {1,2,1,1} and h(n)={1,1,2,2} (August 2021)

31) Compute DFT for the sequence X(n)= {1,0,1,1,0,1,1,1} using DITFFT (August 2021)

32) What is FFT? Calculate the number of multiplications needed in the calculation of DFT using FFT algorithm with 32 point sequence. (August 2021)

33) Compare DIT FFT and DIF FFT algorithms. (August 2021)

34) Explain any three properties of Z transform. (August 2021)

35) Explain any three properties of DFT. (August 2021)

UNIT-III

2 Marks

1. What is Gibbs phenomenon? (March 2017)
2. Explain the procedure for designing FIR filters using windows. (March 2017)
3. What is warping effect? What is its effect on magnitude and phase response? (March 2017, May 2019, August 2021)
4. Give the equation for Hamming window and Blackman window. (November 2016)
5. What is dead band of a filter? (November 2016)
6. Define impulse response. (May 2016)
7. Define sampling and Nyquist rate (May 2016)
8. Explain the effects of truncating an infinite Fourier series into a finite series. (April2018)
9. What is the condition for the impulse response of FIR filter to satisfy for constant group and phase delay and for constant group delay? (April2018)
10. Write the characteristics of window in FIR filters. (May 2019)
11. Determine the frequency response of FIR filters defined by

y(n) = 0.5x(n)+x(n-1)+0.5x(n-2). (May 2019)

5 Marks:

1) Explain the type -1 FIR filter design procedure using frequency sampling method. (March 2017, Nov. 2020)
2) List the features of Blackman window spectrum. (March 2017)
3) Explain the design procedure of linear phase FIR filter using Fourier series method. (March 2017)
4) Realize the system function $\frac{2}{3}z + 1 + \frac{2}{3}z^{-1}$ by linear phase FIR structure. (Nov 2016)
5) Explain in detail designing of digital IIR filters using impulse invariant method. (May 2019)
6) Explain linear phase characteristics of FIR filters. (May 2019, Nov.2020)
7) Explain the designing of FIR filters using windows. (Nov 2016)
8) Draw and explain frequency response of FIR digital filter. (May 2016)
9) List the designing steps of FIR filters using fourier method. (May 2016)
10) Design a high pass filter using hamming window with a cut-off frequency of 1.2 radians/second and N=9. (May 2016)
11) Design a low pass digital FIR filter using Kaiser Window satisfying the specifications given below.
    Pass band cut-off frequency = 100 Hz.
    Stop band cut-off frequency = 200 Hz
    Pass band ripple = 0.1dB
    Stop band attenuation =20 dB
    Sampling frequency = 1000 Hz. (May 2016)
12) Determine the transfer function H(z) of an FIR filter to implement h(n) = $\delta(n) + 2\delta(n-1) + \delta(n-2)$ using frequency sampling techniques. (May 2015)
13) Give the comparison between FIR and IIR filters with examples. (May 2015,May 2019)
14) Compare FIR and IIR filters. (June 2014, August 2021)
15) Design a high pass FIR filter whose cut-off frequency is 1.4 rad/sec and N=5 using Hamming window. (June 2014)
16) Compare various windowing techniques with respect to side lobes and beam width. (Dec 2013, Nov 2020)
17) Design an FIR Digital High pass filter using Hanning window whose cutoff freq is 1.2

rad/s and length of window N=9. (Dec 2013)

18) The desired frequency response of a low pass filter is given (April 2018)

$$H_d(e^{j\omega})=\begin{cases} e^{-j\omega} & \frac{-3\pi}{4} \le \omega \le \frac{3\pi}{4} \\ 0 & \frac{3\pi}{4} \le \omega \le \pi \end{cases}$$

Find $H(e^{j\omega})$ for M=7 using a rectangular window.

19) Explain the type II frequency sampling method of designing an FIR digital filter. (April 2018)

18) Design a band pass filter which approximates the ideal filter with cutoff frequencies at 0.2 rad/sec and 0.3 rad/sec. The filter order is M=7. Use the Hanning window function. (April 2018)

20) Design an ideal band pass filter with a frequency response. (April 2018)

$$H_d(e^{j\omega})=\begin{cases} 1 & \frac{\pi}{4} \le |\omega| \le \frac{3\pi}{4} \\ 0 & otherwise \end{cases}$$

21) Design an ideal high pass filter using Hanning window with a frequency response.

$$H_d(e^{jw}) = 1 \quad ; \quad \frac{\pi}{4} \le \omega \le \pi$$
$$= 0 \quad |\omega| \le \frac{\pi}{4}$$

Find the values of h(n) for N=11.Find H(z). (May 2019)

36) 22) Compare various windowing techniques with respect to side lobes and beam width. (August 2021)

UNIT-IV

2 Marks:

1) Give any two properties of Butterworth low pass filter. (2 marks) (March 2017)
2) State the properties of IIR filter. (2 marks) (November 2016)
3) State the methods used to prevent overflow. (3 marks) (November 2016)
4) What are the advantages of Butterworth filter? (2 marks) (May 2016)
5) What are the advantages and disadvantages of Chebyshev filter. (3 marks) (May 2016)
6) What are the properties of Butterworth Low pass filter? (2marks)(April2018)
7) Discuss the stability of the impulse invariant mapping technique. (3marks)(April2018)

8) Compare Butterworth and Chebyshev filters. (May 2019)

5 Marks:

1) What are the steps to design an analog Chebyshev low pass filter. (March 2017)
2) Apply bilinear transformation to (March 2017)

$$H(s) = \frac{2}{(s+1)(s+2)}$$

with T=1 Sec and find H (z).

3) Consider an analog filter with transfer function $H(s) = \frac{1}{(s+1)(s^2+s+1)}$ Is this a Butterworth or Chebyshev filter? Obtain the transfer function of an IIR digital filter using impulse invariant transformation. Assume T = 1 Sec. (March 2017, Nov 2020)
4) Design a Butterworth high pass filter satisfying:
   $f_p = 0.32$Hz ; $\alpha_p = 0.5$ dB
   $f_s = 0.16$Hz ; $\alpha_s = 30$ dB ; F = 1 Hz (Nov 2016)
5) Discuss the steps in design of IIR filter using bilinear transformation for any one type of filter. (Nov 2016, Nov 2020)
6) Discuss in detail about spectral transformations. (May 2016)
7) Explain how IIR digital filters are designed from analog filters. (May 2016)
8) Compare the impulsive invariance and bilinear transformation methods. (May 2016)
9) Find the order and poles of a low pass Butterworth filter that has a -3dB bandwidth of 400 Hz and an attenuation of 20dB at 1 KHz. (May 2016)
10) Design a digital IIR low pass Butterworth filter that has a 2dB pass band attenuation at a frequency of 300pi rad/sec and at least 60dB stop band attenuation at 4500pi rad/sec. Use backward reference transformation. (May 2015)
11) Determine the order and the poles of a type-I low pass Chebyshev filter that satisfies the following constrains
    $0.8 \leq |H(w)| \leq 1$; $0 \leq W \leq 0.2$pi;
    And $|H(w)| \leq 0.2$; $0.6\text{pi} \leq W \leq \text{pi}$. (May 2015)
12) Determine the system function of IIR Butterworth LPF that satisfies the following constrains
    $0.9 \leq |H(j\Omega)| \leq 1$; $0 \leq \Omega \leq 0.2\pi$;
    $|H(j\Omega)| \leq 0.2$; $0.4\pi \leq \Omega \leq \pi$. (May 2019)

13) For the analog filter with transfer function H(s) = 2(s+1)(s+3), determine H(z) using bilinear transformation technique. Use T =0.1sec. (June 2014)

14) Explain impulse invariant method of IIR filter design. (June 2014)

15) Explain briefly the frequency response of LTI systems. (Dec 2013)

16) Discuss direct form-I & II IIR realization structures in detail with necessary flow graphs. (Dec 2013)

17) List out the merits and demerits of Butterworth and Chebyshev filter approximation techniques. (Dec 2013)

18) Prove that the relationship between analog (Ω) and digital (ω) frequency in bilinear transformation is given by Ω = (2/T) Tan(ω/2) (Dec 2013)

19) Design a digital low pass filter using Chebyshev filter that meets the following specifications: Pass band magnitude characteristics that is constant to within 1 dB for recurrences below ω=0.2π and stop band attenuation of at least 15dB for frequencies between ω=0.3π and π. Use bilinear transformation. (April 2018)

20) An analog filter has the following system function. Convert this filter into a digital filter by using the impulse invariant technique: (April 2018)

$$H(s) = \frac{1}{(s+0.1)^2+9}$$

21) Using a bilinear transformation, design a Butterworth filter which satisfy the following conditions: (April 2018)

$$0.8 \leq |H(e^{j\omega}) \leq 1 \qquad 0 \leq \omega \leq 0.2\pi$$

$$|H(e^{j\omega}) \leq 0.2 \qquad 0.6\pi \leq \omega \leq \pi$$

22) Determine H(z) using impulse invariance method for the following system function: (April 2018)

$$H(s) = \frac{1}{(s+0.5)(s^2+0.5s+2)}$$

23) What are the steps to design an analog Chebyshev low pass filter? (May 2019)

37) Sketch and explain the magnitude responses of the chebyshev type-1 and type-2 filters. (August 2021)

UNIT-V

2 Marks:

1) What is over flow oscillations? (March 2017)
2) What is the need for anti-aliasing filter prior to down sampling? (March 2017)
3) Give the steps in multistage sampling rate converter design. (November 2016)
4) Write any four applications of Multi – rate signal processing. (November 2016)
5) Define Decimation. (May 2016)
6) What is the need for Multi rate Digital Signal Processing? (May 2016)
7) What is the need for MultiMate Digital Signal Processing? (April2018)
8) What do you mean by quantization step size? (April2018)
9) Define limit cycle oscillations and give its types. (May 2019)
10) Write a short note on dead band. (May 2019)

5 MARKS:

1) What are the effects of finite word length in digital filters? (March 2017)
2) Explain limit cycles in recursive structures. (March 2017)
3) Explain interpolation process with an example. (March 2017)
4) Explain with block diagrams how can sampling rate be converted by a rational factor M/L both in time domain and frequency domain. (March 2017)
5) With respect to finite word length effects in digital filters, explain over flow limit cycle oscillation with example. (Nov 2016)
6) Explain the applications of Multi rate signal processing. (Nov 2016, Nov 2020)
7) What is meant by signal scaling? Explain. (Nov 2016)
8) What are the dead band effects? Discuss. (May 2016)
9) What is mean by sampling rate conversion? Explain. (May 2016)
10) What are limit cycles and discuss various types of limit cycles in brief. (May 2016)
11) Discuss the process of performing sampling rate conversion by an rational factor I/D. (May 2016, August 2021)
12) Explain the characteristics of a limit cycle oscillation with respect to the system described by the equation Y(n)=0.85y(n-2)+0.72y(n-1)+x(n)
Determine the dead band of the filter x(n) = ¾ δ(n). (May 2015)
13) Explain about multi rate signal processing and gives its examples. (May 2015)
14) Consider a single stage interpolator with the following specifications:
Original sampling rate = 1KHz
Interpolation factor L = 2

Frequency of interest = 0 – 150 Hz

Passband ripple = 0.02 dB

Stopband attenuation = 45 db

(i) Draw the block diagram for the interpolator.

ii) Determine the window type filter length and cutoff frequency, if the window method is used for the anti imaging FIR filter design. (May 2015)

15) Explain the process of decimation using relevant expression and block diagram. (June 2014)

16) Explain the implementation of polyphase filter structure for interpolator. (June 2014)

17) Write notes on:

(a) Limit cycles

(b) Over flow oscillations

© Dead band effects. (June 2014, August 2021)

18) Discuss the process of Interpolation by a factor I with a neat block diagram (Dec 2013)

19) Explain the process of Interfacing of digital systems with different sampling rates with a neat block diagram. (Dec 2013, Nov 2020)

20) Discuss quantization errors occuring in the computation of DFT. (Dec 2013, Nov 2020)

21) What are limit cycles and explain the types of it and also give their remedies. (Dec 2013)

22) Explain the interpolation process for an integer factor I with an example. (April 2018, Nov 2020)

23) Given the limit cycle behavior $y(n) = 0.7y(n-2) + 0.52y(n-1) + x(n)$. Find the dead band of the above two systems. (April 2018)

24) The signal x(n) is defined by (April 2018)

$$g(n) = \begin{cases} A^n & n > 0 \\ 0 & otherwise \end{cases}$$

i) Obtain the decimated signal with a factor of 3

ii) Obtain the interpolated signal with a factor of 3

25) Given the system $y(n) = \frac{1}{2}y(n-1) + x(n)$ (April 2018)

i) Calculate the system response to the input x(n)=$(\frac{1}{4})^n$u(n) assuming infinite precision arithmetic.

ii) Calculate the response y(n), $0 \le n \le 5$ to the same input assuming finite precision with five bits, one sign bit plus four fractional bits. The quantization is performed by truncation. Discuss the results.

(26) Explain the process of decimation using relevant expression and block diagram. (May 2019)

(27) Explain with block diagrams how can sampling rate be converted by a rational factor M/L both in time domain and frequency domain. (May 2019)

PART-A answers

UNIT-1

1. Show that $\delta(n) = u(n) - u(n-1)$. (2 marks) (April 2018)

The unit impulse function, δ(n), also known as the Dirac delta function, is defined as:

δ(n) = 0 for n≠0;

= undefined for n= 0

and has the following special property: $\delta(n) = u(n) - u(n-1)$

Unit step function is defined as

$u(n)$ =1 for n≥0

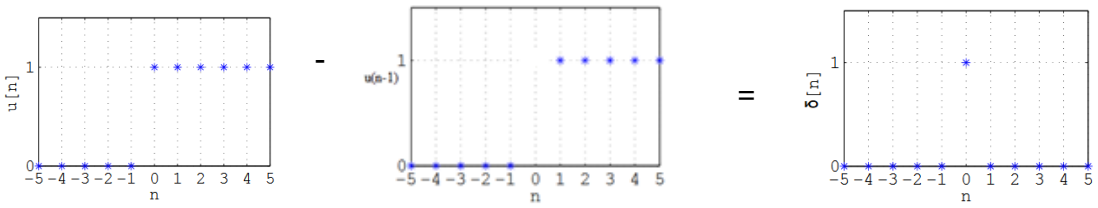
= 0 for n≤0

Shifted unit step function is defined as

$u(n-1)$ =1 for n≥1

= 0 for n≤1

u(n) – u(n-1)=



2. Find the z-transform of $f(n) = n^2u(n)$ (3 marks) (April 2018)

Ans: Given $f(n) = n^2u(n)$

z-transform of u(n) is

$Z[u(n)]=\frac{z}{z-1}$

Using differentiation property

$Z[nu(n)] = -z\frac{d}{dz}[\frac{z}{z-1}]$

$=\frac{z}{(z-1)^2}$

Similarly

$$Z[n^2u(n)] = -z\frac{d}{dz}[\frac{z}{(z-1)^2}]$$

$$=-z\{\frac{(-z-1)(z-1)}{(z-1)^4}\}$$

$$\therefore Z[n^2u(n)] = \frac{z(z+1)}{(z-1)^3}$$

3. What are the applications of digital signal processing? (2 marks) (March 2017)

Digital signal processing (**DSP**) is the use of digital processing, such as by computers, to perform a wide variety of signal processing operations. The signals processed in this manner are a sequence of numbers that represent samples of a continuous variable in a domain such as time, space, or frequency.

Digital signal processing and analog signal processing are subfields of signal processing. DSP applications include audio and speech processing, sonar, radar and other sensor array processing, spectral density estimation, statistical signal processing, digital image processing, signal processing for telecommunications, control systems, biomedical engineering, seismology, among others.

DSP can involve linear or nonlinear operations. Nonlinear signal processing is closely related to nonlinear system identification and can be implemented in the time, frequency, and spatiotemporal domains.

The application of digital computation to signal processing allows for many advantages over analog processing in many applications, such as error detection and correction in transmission as well as data compression. DSP is applicable to both streaming data and static (stored) data.

4. Explain region of convergence and its properties. (3 marks) (March 2017)

The ROC for a given x[n] , is defined as the range of z for which the z-transform converges. Since the z-transform is a power series, it converges when $\sum x[n]z^{-n}$ is absolutely summable.

Properties of the Region of Convergence: The Region of Convergence has a number of properties that are dependent on the characteristics of the signal, x[n].

- **The ROC cannot contain any poles.** By definition a pole is a where X(z) is infinite. Since X(z) must be finite for all z for convergence, there cannot be a pole in the ROC.
- **If** x[n] **is a finite-duration sequence, then the ROC is the entire z-plane, except possibly** z=0 **or** |z|=∞.

6. Define decimation and interpolation. (2 marks) (November 2016)?

In digital signal processing, **decimation** is the process of reducing the sampling rate of a signal. The term **down sampling** usually refers to one step of the process, but sometimes the terms are used interchangeably. Complementary to upsampling, which increases sampling rate, decimation is a specific case of sample rate conversion in a multi-rate digital signal processing system. A system component that performs decimation is called a decimator.

When decimation is performed on a sequence of samples of a signal or other continuous function, it produces an approximation of the sequence that would have been obtained by sampling the signal at a lower rate (or density, as in the case of a photograph). The decimation factor is usually an integer or a rational fraction greater than one. This factor multiplies the sampling interval or, equivalently, divides the sampling rate. For example, if compact disc audio at 44,100 samples/second is decimated by a factor of 5/4, the resulting sample-rate is 35,280.

7. State linear and static system with example. (3 marks) (November 2016)

Static systems: Some systems have feedback and some do not. Those, which do not have feedback systems, their output depends only upon the present values of the input. Past value of the data is not present at that time. These types of systems are known as **static systems**. It does not depend upon future values too.

Since these systems do not have any past record, so they do not have any memory also. Therefore, we say all static systems are memory-less systems. Let us take an example to understand this concept much better.

Ex: i. $y(n)=x(n)+x(n-1)$ --- it is not static
ii. $y(n)=\sin[x(n)]$ ---- it is static

A **linear system** follows the laws of superposition. This law is necessary and sufficient condition to prove the linearity of the system. Apart from this, the system is a combination of two types of laws −

- Law of additivity
- Law of homogeneity

i. $y(n)=x(n+1)+x(n-1)$ ----it is linear
ii. $y(n)= x(n)+C$ ----- it is nonlinear

8. Write four advantages of digital signal processing over analog signal Processing? (2 marks) (May 2016)

Advantages of DSP: The advantages of DSP over Analog Signal Processing are:
1. High Accuracy: The accuracy of the analog filter is affected by the tolerance of the circuit components used for design the filter, but DSP has superior control of accuracy.
2. Cheaper: The digital realization is much cheaper than the analog realization in many applications.
3. Flexibility in Configuration: For reconfiguring an analog system, we can only do it by redesign of system hardware; where as a DSP System can be easily reconfigured only by changing the program.
4. Ease of Data Storage: On magnetic media, without the loss of fidelity the digital signals can be stored and can be processed off-line in a remote laboratory.
5. Time Sharing: The cost of the processing signal can be reduced in DSP by the sharing of a given processor among a number of signals.

9. Show that the frequency response of a discrete system is a periodic function of frequency. (3 marks) (May 2016)

Note first that H(Ω) repeats periodically on the frequency (Ω) axis, with period 2π, because a sinusoidal or complex exponential input of the form in Equation

x[n] = cos(Ω0n + θ0) ,

or

x[n] = A0.exp(Ω0n+θ0) for all n .

is unchanged when its frequency is increased by any integer multiple of 2π. This can also be seen from Evaluation, the defining equation for the frequency response. It follows that only the interval $|\Omega| \leq \pi$ is of interest

UNIT-II

1) State and prove the any three properties of DFT. (3marks)(April 2018)

Time Shifting

$$\mathcal{F}[x[m-m_0]] = e^{-jm_0\omega}X(e^{j\omega})$$

Proof:

$$\mathcal{F}[x[m-m_0]] = \sum_{m=-\infty}^{\infty} x[m-m_0]e^{-j\omega m}$$

If we let $m' = m - m_0$, the above becomes

$$\mathcal{F}[x[m-m_0]] = \sum_{m=-\infty}^{\infty} x[m']e^{-j\omega(m'+m_0)} = e^{-j\omega m_0}X(e^{j\omega})$$

Differencing

Differencing is the discrete-time counterpart of differentiation.

$$\mathcal{F}[x[m]-x[m-1]] = (1-e^{-j\omega})X(e^{j\omega})$$

Proof:

$$\mathcal{F}[x[m]-x[m-1]] = \mathcal{F}[x[m]] - \mathcal{F}[x[m-1]]$$

$$: \quad X(e^{j\omega}) - X(e^{j\omega})e^{-j\omega} = (1-e^{-j\omega})X(e^{j\omega})$$

Differentiation in frequency

$$\mathcal{F}^{-1}[j\frac{d}{d\omega}X(e^{j\omega})] = m\ x[m]$$

proof: Differentiating the definition of discrete Fourier transform with respect to ω, we get

$$\frac{d}{d\omega}X(e^{j\omega}) \quad : \quad \frac{d}{d\omega}\sum_{m=-\infty}^{\infty} x[m]e^{-j\omega m} = \sum_{m=-\infty}^{\infty} x[m]\frac{d}{d\omega}e^{-j\omega m}$$

$$: \quad \sum_{m=-\infty}^{\infty} -jmx[m]e^{-j\omega m}$$

2) What is the basic operation of DIF algorithm? (2marks)(April 2018)

- DIFFFT algorithms are based upon decomposition of the output sequence into smaller and smaller sub sequences.
- In this output sequence X(k) is considered to be splitted into even and odd numbered samples
- Splitting operation is done on frequency domain sequence.
- In DIFFFT, input sequence is in natural order. And DFT should be read in bit reversed order.

Example:_In DIF N Point DFT is splitted into N/2 points DFT s. X(k) is splitted with k even and k odd this is called Decimation in frequency(DIF FFT).

N point DFT is given as

$$X(k) = \sum_{n=0}^{N-1} x(n)\, W_N^{kn} \quad (1)$$

Since the sequence x(n) is splitted N/2 point samples, thus

$$X(k) = \sum_{m=0}^{N/2-1} x(n)\, W_N + \sum_{m=0}^{N/2-1} x(n+N/2)\, W_N$$

$$X(k) = \sum_{m=0}^{N/2-1} x(n)\, W_N^{kn} + W_N^{kN/2} \sum_{m=0}^{N/2-1} x(n+N/2)\, W^{kn}$$

$$X(k) = \sum_{m=0}^{N/2-1} x(n)\, W_N^{kn} + (-1)^k \sum_{m=0}^{N/2-1} x(n+N/2)\, W^{kn}$$

$$X(k) = \sum_{m=0}^{N/2-1} \left[x(n) + (-1)^k x(n+N/2) \right] W_N^{k}$$

Let us split X(k) into even and odd numbered samples

$$X(2k) = \sum_{m=0}^{N/2-1} \left[x(n) + (-1)^{2k}\, x(n + N/2)\, W_N^{2kn} \right] \quad (4)$$

$$X(2k+1) = \sum_{m=0}^{N/2-1} \left[x(n) + (-1)^{(2k+1)}\, x(n + N/2) W_N^{(2k+1)n} \right] \quad (5)$$

Equation (4) and (5) are thus simplified as

$$g1(n) = x(n) + x(n + N/2)$$
$$g2(n) = x(n) - x(n + N/2)\, W_N^{n}$$

Fig 1 shows **Butterfly computation** in DIF FFT.

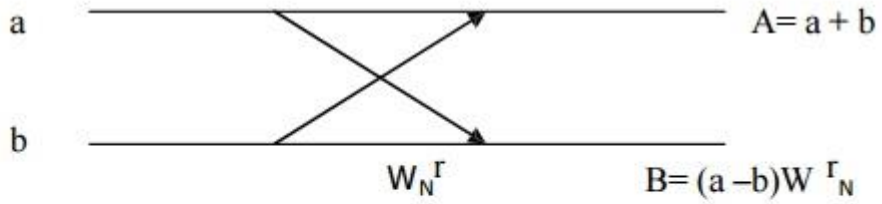


Fig 1. BUTTERFLY COMPUTATION

3) What is zero padding? What are its uses? (2 marks) (March 2017)

Zero-padding a signal increases its **period**. This decreases the spacing(the inverse of the fundamental period) between the DFS(Discrete Fourier Series) coefficients of the signal's periodic summation.

Advantages:

- If length of your sequence doesn't correspond to the size that can be handled efficiently with FFT routine (usually powers of prime numbers) then you might want to add some extra zeros to the nearest power in order to get the maximum speed-up. In worst case you double the memory you need for your signal.
- Adding zeros is equal to interpolating samples of your spectrum with sinc function. Therefore you will find it looking more smoothly. It is not affecting frequency resolution in any way.
- If some peaks were split between two bins, these can be interpolated to some extend and you might be able to retrieve some amplitude information thanks to that.
- If you are trying to plot frequency response of some FIR filter from it's impulse response then you need to add zeros to it. Otherwise you will get as many samples as the length of filter is.

- If you are trying to convolve your signal with some pattern using FFT, then you need to pad your signals with zeros to the appropriate length. Otherwise result of convolution will be incorrect (replicas in frequency domain will overlap).

4) State and prove time shifting property of DFT. (3 marks) (March 2017)

Timeshifting Property:

$$\mathcal{F}[x[m-m_0]] = e^{-jm_0\omega}X(e^{j\omega})$$

Proof:

$$\mathcal{F}[x[m-m_0]] = \sum_{m=-\infty}^{\infty} x[m-m_0]e^{-j\omega m}$$

If we let $m' = m - m_0$, the above becomes

$$\mathcal{F}[x[m-m_0]] = \sum_{m=-\infty}^{\infty} x[m']e^{-j\omega(m'+m_0)} = e^{-j\omega m_0}X(e^{j\omega})$$

5) If x(n)= $\cos\frac{\Pi}{3}$n, find spectra of the signal? (2 marks) (November 2016)

$x(n) = \cos\frac{\pi n}{3}$ $\omega_0 = \frac{\pi}{3}$ $f_0 = \frac{1}{6}$

Hence x(n) is periodic with fundamental period N=6

$$c_k = \frac{1}{N}\sum_{n=0}^{N-1} x(n)e^{-j2\pi kn/N} = \frac{1}{6}\sum_{n=0}^{5} x(n)e^{-j2\pi kn/6} \quad ,k = 0,1,...,5$$

$$x(n) = \cos\frac{\pi n}{3} = \frac{1}{2}e^{j2\pi n/6} + \frac{1}{2}e^{-j2\pi n/6}$$

$e^{j2\pi n/6} = e^{j2\pi(5-6)n/6} = e^{j2\pi 5n/6}$ which means that $c_{-1} = c_5$

$$c_k = \frac{1}{6}\sum_{n=0}^{5}\cos(\frac{n\pi}{3})e^{-j2\pi kn/6} \quad ,k = 0,1,...,5$$

$$\frac{1}{6}\left(1+\cos\frac{\pi}{3}e^{-j2\pi k/6}+\cos\frac{2\pi}{3}e^{-j2\pi k2/6}+\cos\frac{3\pi}{3}e^{-j2\pi k3/6}\right.$$

$$\left.+\cos\frac{4\pi}{3}e^{-j2\pi k4/6}+\cos\frac{5\pi}{3}e^{-j2\pi k5/6}\right),\quad k=0,1,\ldots,5$$

$c_0=0$ $c_1=\frac{1}{2}$ $c_2=0$ $c_3=0$ $c_4=0$ $c_5=\frac{1}{2}$

6) How many multiplications and additions are required to compute N-point DFT using radix – 2 FFT? (3 marks) (November 2016)

Assume N being the no of samples to be present in DFT

1. Complex multiplications = N/2 $\log_2 N$

2. Complex additions = N $\log_2 N$

7) Give the relation between DTFT and Z- Transform? **m. (2 marks) (May 2016)**

Relationship between DTFT and z-transform

Recall that

- The Discrete-time Fourier transform (DTFT) is $X(\omega)=F[x(n)]=\sum x[n]e^{-j\omega n}$.
- The z-transform is $X(z)=ZT[x(n)]=\sum x[n]z^{-n}$
- So we get X(w) when we replace z with exp(jw) in ZT.

One can obtain the DTFT from the z-transform X(z) by as follows:

$X(z)|z=ejw=X(\omega)$

In other words, if you restrict the z-transoform to the unit circle in the complex

plane, then you get the Fourier transform (DTFT).

8) Distinguish between linear convolution and circular convolution. (3 marks) (May 2016)

Convolution is a formal mathematical operation, just as multiplication, addition, and integration. Addition takes two numbers and produces a third number, while convolution takes two signals and produces a third signal. Convolution is used in the mathematics of many fields, such as probability and statistics. In linear systems, convolution is used to describe the relationship between three signals of interest: the input signal, the impulse response, and the output signal. Convolution is an integral concatenation of two signals. It has many applications in numerous areas of signal processing. The most popular application is the determination of

the output signal of a linear time-invariant system by convolving the input signal with the impulse response of the system.

Linear convolution is the main function used to calculate the output for the linear time with respect to it's input as well as the impulse response.This convolution is used for infinitesignal.

Circular convolution is also used to calculate output but in this case the system support is always periodic. As the name indicate this is used for finite signal.

Define twiddle factor and give its values for N=4. (2 marks) (May 2019)

Ans: A twiddle factor, in fast Fourier transform (FFT) algorithms, is any of the trigonometric constant coefficients that are multiplied by the data in the course of the algorithm.

$WN=e^{-j2\pi/N}$

For n=4

$W_N=-j$

Unit III

1) **Explain the effects of truncating an infinite Fourier series into a finite series.(2marks)(April 2018)**

Ans. The desired frequency response $H_d(e^{j\omega})$ of a filter is periodic in frequency and can be expressed in fourier series. The resultant series is given by

$$H_d(e^{j\omega}) = \sum_{n=-\alpha}^{n=\alpha} h_d(n)e^{-j\omega n}$$

Where

$$h_d(n) = \frac{1}{2\pi}\int_{-\pi}^{\pi} H_d(e^{j\omega})\, e^{j\omega n}.\, d\omega$$

And known as Fourier coefficient having infinite length. One possible way of obtaining FIR filter is to truncate the infinite Fourier series at n=± ($\frac{N-1}{2}$), where N is the length of the desired sequence. But abrupt truncation of the Fourier series results in oscillations in the pass band and stop band. These oscillations are due to slow convergence of the Fourier series and this effect is known as Gibb's phenomenon. To reduce these oscillations, the Fourier coefficient of the filter are modified b multiplying the infinite impulse response with a finite weighing sequence w(n) called a window where

ω (n)= ω (-n) ≠ 0 for $|n| \le \frac{N-1}{2}$

=0 for $|n| > \frac{N-1}{2}$

After multiplying window sequence w(n) with $h_d(n)$, we get a finite duration sequence h(n) that satisfies the desired magnitude response

h(n)= $h_d(n)$ ω (n) for all $|n| \le \frac{N-1}{2}$

=0 for $|n| > \frac{N-1}{2}$

2) **What is the condition for the impulse response of FIR filter to satisfy for constant group and phase delay and for constant group delay? (3marks)(April 2018)**

Ans. For linear phase FIR filter to have both constant group delay and constant phase delay

$\Theta(\omega) = -\alpha\omega \quad -\pi \le \omega \le \pi$

For satisfying above condition

h(n)=h(N-1-n),

i.e. the impulse response must be symmetrical about n=$\frac{N-1}{2}$.
If only constant group delay is desired then Θ(ω) = β-αω
For satisfying the above condition
H(n)=-h(N-1-n)
i.e. the impulse response is antisymmetrical about n=$\frac{N-1}{2}$

3) What is Gibbs phenomenon? (2 marks) (March 2017)

Answer: One possible way of finding an FIR filter that approximates H(ejω)would be to truncate the infinite Fourier series at n= ± (N-1/2).Abrupt truncation of the series will lead to oscillation both in pass band and is stop band .This phenomenon is known as Gibbs phenomenon.

4) Explain the procedure for designing FIR filters using windows. (3 marks) (March 2017)

Answer: a) Choose the desired frequency response Hd(w)

b) Take the inverse fourier transform and obtain Hd(n)
c) Convert the infinite duration sequence Hd(n) to h(n)
d) Take Z transform of h(n) to get H(Z)

5) Give the equation for Hamming window and Blackman window. (2 marks) (November 2016)

Answer: Hamming Window - $w(n) = \alpha - \beta(2\pi n/(N-1))$, with α = 0.54 and $\beta = 1 - \alpha = 0.46$.

Blackman Window – $w(n) = \alpha_0 - \alpha_1 \cos\left(\frac{2\pi n}{N-1}\right) + \alpha_2 \cos\left(\frac{4\pi n}{N-1}\right), \alpha_0 = \frac{1-\alpha}{2}; \alpha_1 = \frac{1}{2}; \alpha_2 = \alpha/2.$

6) What is dead band of a filter? (3 marks) (November 2016)

Answer: The limit cycle occur as a result of quantization effect in multiplication. The amplitudes of the output during a limit cycle are confined to a range of values called the dead band of the filter.

7) Define impulse response. (2 marks) (May 2016)

Answer: The impulse response, or impulse response function (IRF), of a dynamic system is its output when presented with a brief input signal, called an impulse. More generally, an impulse response is the reaction of any dynamic system in response to some external change.

8) Define sampling and Nyquist rate. (3 marks) (May 2016)

Answer: The process of converting a continuous-time signal into a discrete – time signal is known as sampling.

Nyquist rate is the theoretical minimum sampling rate at which a signal can be sampled and still be recovered from its samples without any distortion.

Unit IV

1) **Discuss the stability of the impulse invariant mapping technique.(2marks)(April 2018)**

Impulse invariance is a technique for designing discrete-time infinite-impulse-response (IIR) filters from continuous-time filters in which the impulse response of the continuous-time system is sampled to produce the impulse response of the discrete-time system.

Performing a z-transform on the discrete-time impulse response produces the following discrete-time system function

$$H(z) = T\sum_{k=1}^{N}\frac{A_k}{1-e^{s_k T}Z^{-1}}$$

Thus the poles from the continuous-time system function are translated to poles at $z = e^{s_k T}$. The zeros, if any, are not so simply mapped.

Since poles in the continuous-time system at $s = s_k$ transform to poles in the discrete-time system at $z = \exp(s_k T)$, poles in the left half of the *s*-plane map to inside the unit circle in the *z*-plane

2) **Give any two properties of Butterworth low pass filter. (2 marks) (March 2017 &April 2018)**

Answer: Properties of Butterworth low pass filter are:

1. It has monotonic amplitude response in both passband and stopband.
2. Quick roll-off around the cutoff frequency, which improves with increasing order.

3) **What is warping effect? What is its effect on magnitude and phase response? (3 marks)**
(March 2017)

Answer: For smaller values of w there exist linear relationship between w and but for larger values of w the relationship is nonlinear. This introduces distortion in the frequency axis. This effect compresses the magnitude and phase response. This effect is called **warping effect.**

The effect of the non linear compression at high frequencies can be compensated. When the desired magnitude response is piecewise constant over frequency, this compression can be compensated by introducing a suitable rescaling or prewar ping the critical frequencies.

4) **State the properties of IIR filter. (2 marks) (November 2016)**

Answer: a) The physically realizable IIR filters do not have linear phase.

b) The IIR filter specifications include the desired characteristics for the magnitude response only.

5) State the methods used to prevent overflow. (3 marks) (November 2016)

Answer: There are two methods used to prevent overflow-

a) Saturation arithmetic
b) Scaling

6) What are the advantages of Butterworth filter? (2 marks) (May 2016)

Answer: The advantage of Butterworth filters is the smooth, monotonically decreasing frequency response in the transition region.

7) What are the advantages and disadvantages of Chebyshev filter. (3 marks) (May 2016)

Answer: Advantages are:

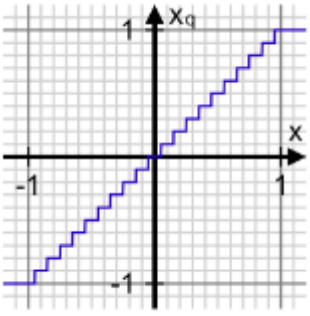
a) Chebyshev filters have steeper decline in the band.
b) Chebyshev filters are used all over the place in electronics.
c) This type of filter has an all-pole amplitude response with the poles distributed round an ellipse in the complex frequency plane.
d) This is a simple easy to design filter that has an excellent performance.

Disadvantages are having more distortion in the wavelength frequency available.

UNIT-V

1) What do you mean by quantization step size? (2marks)(April 2018)

After the sampling we have a sequence of numbers which can theoretically still take on any value on a continuous range of values. Because this range in continuous, there are infinitely many possible values for each number, in fact even uncountably infinitely many. In order to be able to represent each number from such a continuous range, we would need an infinite number of digits - something we don't have. Instead, we must represent our numbers with a finite number of digits, that is: after discretizing the time-variable, we now have to discretize the amplitude-variable as well. This discretization of the amplitude values is called quantization.



2) What is over flow oscillations? (2 marks) (March 2017)

With fixed-point arithmetic it is possible for filter calculations to overflow. This happens when two numbers of the same sign add to give a value having magnitude greater than one. Since numbers with magnitude greater than one are not representable, the result overflows. For example, the two's complement numbers 0.101 (5/8) and 0.100 (4/8) add to give 1.001 which is the two's complement representation of −7 / 8.

3) What is the need for anti-aliasing filter prior to down sampling? (3 marks) (March 2017)

An **anti-aliasing filter** (AAF) is a filter used before a signal sampler to restrict the bandwidth of a signal to approximately or completely satisfy the sampling theorem over the band of interest. Since the theorem states that unambiguous reconstruction of the signal from its samples is possible when the power of frequencies above the Nyquist frequency is zero, a real anti-aliasing filter trades off between bandwidth and aliasing. A realizable anti-aliasing filter will typically either permit some aliasing to occur or else attenuate some in-band frequencies close to the Nyquist limit. For this reason, many practical systems sample higher than required to ensure that all frequencies of interest can be reconstructed, a practice called oversampling.

4) Give the steps in multistage sampling rate converter design. (2 marks) (November 2016)

Multiple stages for decimation (or interpolation) can reduce the number of filter coefficients in the filter specifications. The signal can be decimated more than once, using a gradual change in sampling frequency.

Conventional decimation:

x(n)------→ Anti Aliasing Filter(h[n])-------→ Decimation by D----→ y[n]

Decimation in mutliple stages (multistage):

x(n)---→h_1 [n]---→ D_1 ----→ h_2 [n] ----→D_2 ----→h_3 [n] -----→D_3 -------→ y[n].

5) Write any four applications of Multi – rate signal processing. (3 marks) (November 2016)

Applications of Multirate digital signal processing

1) Used for the design of phase shifters
2) Interfacing of digital systems with different sampling rates
3) Implementation of digital filter banks
4) Subband coding of speech signals.

6) Define Decimation. (2 marks) (May 2016)

Multirate DSP consists of:

1. Decimation: It is a process to decrease the sampling rate.

2. Interpolation: It is a process to increase the sampling rate.

"Downsampling" is a process of removing some samples, without the lowpass filtering. A signal is downsampled only when it is "oversampled"(i.e. sampling rate > Nyquist rate). This combined operation of filtering and downsampling is called “Decimation”. To downsample by a factor of M, we must keep every Mth sample as it is and remove the (M-1) samples in between. Ex: To decimate by 4, keep every fourth sample, and remove three out of every four samples.

7) **What is the need for Multi rate Digital Signal Processing? (3 marks) (May 2016 & April 2018)**

Multirate systems are building blocks commonly used in digital signal processing (DSP). Their function is to alter the rate of the discrete-time signals, which is achieved by adding or deleting a portion of the signal samples. "Multirate" simply means "multiple sampling rates". A multirate DSP system simply uses more than one sampling rate within the system. In many systems, multrate DSP increases processing efficiency, which reduces DSP hardware requirements. Also, a few systems are inherently multirate, for example, a "sampling rate converter" system that converts an input sampling rate to a different output sampling rate. Multirate systems play a central role in many areas of signal processing, such as filter bank theory and multiresolution theory, they are essential in various standard signal-processing techniques such as signal analysis, denoising, compression and so on.

8) Define limit cycle oscillations and give its types. (2 marks) (May 2019)

In some systems, when the input is zero or some non zero constant value the nonlinearities due to the finite precision arithmetic operations often cause periodic oscillations to occur in the output. Such oscillations in recursive systems are called limit cycle oscillations. These oscillations will continue to remain in limit cycle even when the input is made zero. Hence, these limit cycle are also called zero input limit cycles.

Limit cycle operations are of two types –

Limit cycle with fixed output

Limit cycle with oscillatory output

9) Write a short note on dead band.(2 marks) (May 2019)

The limit cycles occur as a result of the quantization effects in multiplications. The amplitude of the output during a limit cycle are confined to a range of values that is called the dead band of the filter.

The dead band is given by

$$Dead\ band = \pm\frac{2^{-b}}{1-|a|} = \left[\frac{-2^{-b}}{1-|a|}, \frac{2^{-b}}{1-|a|}\right]$$

Multiple Choice Questions

UNIT I : INTRODUCTION TO DISCRETE TIME SIGNALS AND SYSTEMS

1. y (n) = x (2n) [ ]
   a) Causal b) Non-Causal c) Time invariant d) none

2. x(-n + 2) is obtained using following operation [ ]
   a) x (-n) is delayed by two samples b) x (-n) is advanced by two samples
   c) x (n) is shifted left by two samples d) none

3. The output of anti causal LTI system is [ ]
   a) y (n) = $\sum_{K=0}^{\infty} h(k)x(n-k)$ b) y (n) = $\sum_{K=0}^{n} h(k)x(n-k)$
   c) y (n) = $\sum_{-\infty}^{-1} h(k)x(n-k)$ d) y (n) = $\sum_{-\infty}^{\infty} h(k)x(n-k)$

4. δ(n-k) * x (n-k) is equal to [ ]
   a) x(n-2k) b) x(n-k) c) x(k) d) none

5. Given x(n) the y(n) = x(2n – 6) is [ ]
   a) x(n) is Compressed by 2 and shifted by 6 b) x(n) is Compressed by 2 and shifted by 3
   c) x(n) is Expanded by 2 and shifted by 3 d) none

6. Decimation by a factor N is equivalent to [ ]
   a) Sampling x(t) at intervals t_s / N b) Sampling x(t) at intervals t_sN
   c) N fold increase in sampling rate d) none

7. In fractional delay, x(n-M/N), specify the order of operation. [ ]
   a) Decimation by N, shift by M, Interpolation by N
   b) Shift by M, Decimation by N and Interpolation by N
   c) Interpolation by N, Shift by M and Decimation by N
   d) All are correct

8. Given g(n) = $\{1, \underset{\uparrow}{2}, 3\}$, find x(n) = g (n / 2), using linear interpolation [ ]
   a) 1, 0, 2, 0, 3 b) 1, 1, 2, 2, 3, 3 c) 1, 3/2, 2, 5/2, 3 d) none

9. The h(n) is periodic with period N, x(n) is non periodic with M samples, the output y(n) is
   a) Periodic with period N b) Periodic with period N+M [ ]
   c) Periodic with period M d) none

10. Determine the non causal system [ ]
    a) $y(n) = x(n^2)$ b) $y(n) = \sum_{k=-\infty}^{n} x(k)$
    c) $y(n) = x(n) - x(n-1)$ d) $y(n) = nx(n)$

11. Two signals $x_1(n)=\{1,2,3,4\}$ and $x_2(n)=\{4,3,2,1\}$, then $x_1(n) + x_2(n)$= [ ]

a) {2,2,2,2} b) {3,2,4,1} c) {1,1,1,1} d) {5,5,5,5}

12.Identify the dynamic system [ ]
a) $y(n) = ax^2(n)$ b) $y(n) = ax(n)$ c) $y(n) = ax^2(n) + x(n)$ d) $y(n) = x(n)+x(n-1)$

13.Find the ROC of signal x(n)=u(n-2) [ ]
a) $|z| < 1$ b) $|z| > 10$ c) $|z| < 0$ d) $|z| > 1$

14.What is the speed improvement factor in calculating 64 – point DFT of a sequence using direct computation and FFT algorithm [ ]
a) 40.33 b) 30.33 c) 10.33 d) 21.33

15.Find the linear convolution of two sequences $x_1(n)=\{1,2\}$ and $x_2(n)=\{3,4\}$ [ ]
a) {3,10} b) {10,3,8} c) {3,10,8} d) {3,8,10}

16.Number of complex additions required to calculate Radix – 2 FFT is [ ]
a) $N-1$ b) $\frac{N}{2}log_2N$ c) $Nlog_2N$ d) N

17 In the design a IIR Digital filter for the conversion of analog filter in to Digital domain the desirable property is [ ]
a. The axis in the s - plane should map outside the unit circle in the z - Plane
b. The Left Half Plane(LHP) of the s - plane should map in to the unit circle in the Z - Plane
c. The Left Half Plane(LHP) of the s-plane should map outside the unit circle in the z-Plane
d. The Right Half Plane(RHP) of the s-plane should map in to the unit circle in the Z - Plane

18 The I I R filter design method that overcomes the limitation of applicability to only Lowpass filter and a limited class of bandpass filters is [ ]
a. Approximation of derivatives b. Impulse Invariance
c. Bilinear Transformation d. Frequency sampling

19 In the Frequency Transformations of the analog domain the transformation is [ ]
a. Low Pass to Lowpass b. Lowpass to Highpass
c. Lowpass to Bandpass d. Lowpass to Bandreject

20 In the Frequency Transformations of the analog domain the transformation is [ ]
a. Low Pass to Lowpass b. Lowpass to Highpass
c. Lowpass to Bandpass d. Lowpass to Bandreject

ANSWERS

1.b	2.b	3.c	4.b	5.c	6.b	7.c	8.a	9 a	10.a
11.d	12.c	13.d	14.a	15.c	16.b	17.a	18.c	19.b	20a

REALIZATION OF DIGITAL FILTERS:

1. In direct –form II realization the number of memory locations required is more than that of direct form –I realization [ ]

2. An LTI system having system function H(z) is stable if and only if all poles of H(z) are out side the unit circle. [ ]

3. Relation ship between x(n) and x(z) is ……..

4. The inverse Z – transform of z/z-a is a^n u(n) [ ]

5. Digital filters are not realizable for ideal case [ ]

6.The z-transform of a discrete time signal x(n) is defined as……
7.Relation ship between x(n) and x(z) is ……..
8.z-transform and roc of the anticausal sequence x(n)={-3,-2,-1,0,1} is ……
9.A LTI system with the BIBO stable if and only if ROC contains the…….
10.The ROC cannot contain any ……
11.If x(n) is a finite duration ,two sided sequence the ROC is entire Z-plane except at …….&……
12.parsevals relation is…….
13.relation between s-plane and z-plane is……..
14……. Method is used for evaluation of the inverse Z-transform
1. caushy residue theorem is stated as……

2. ROC of a causal signal is the ……. Of a circle of same radius r

17.The ROC must be a …….region
18.multiplication property of Z-transform is……..
19 .Application of z-transform are ……..
20.Inverse of x(z)= z/(z-a)^3 is …….
Answers:

1. true	2. false	3. true	4. false	5. false	6. x(z)	7. ture	8. x(z)	9. r=1	10. poles
11. cz=0 and 1	12. magnitude square function	13. mapping	14. residue theorem	15. multiple poles	16. greater than	17. unit circle	18. X(z)h(z)	19. cascde and df-1	20. n2an

<u>UNIT II DISCRETE FOURIER TRANSFORM</u>:

1. Power signal is

a) Periodic b) aperiodic c) Continuous d) none [ ]

2. W_N^{nK} *is*

a) $e^{\frac{-j2\Pi K}{N}}$ b) $e^{-j2\Pi nK}$ c) $e^{\frac{-j2\Pi Kn}{N}}$ d) $e^{\frac{2\Pi Kn}{N}}$ [ ]

3. When the sequence is circularly shifted in time domain by 'm' samples i.e. $x((n-m))_N$ then on applying DFT, it is equivalent multiply sequence in frequency domain by

a) $e^{\frac{j2\Pi Km}{N}}$ b) $e^{\frac{-j2\Pi Km}{N}}$ c) $e^{-j2\Pi Km}$ d) $e^{\frac{-2\Pi Km}{N}}$ [ ]

4. Multiplication of sequence in time domain, on apply DFT, it corresponds to circular convolution in frequency domain and is given as
[ ]

a) $x_1(n)\ x_2(n) \xleftrightarrow{DFT} X_1(K)\quad X_2(K)$ b) $x_1(n)\ x_2(n) \xleftrightarrow{DFT} X_1(K)X_2(K)$

c) $x_1(n) * x_2(n) \xleftrightarrow{DFT} X_1(K)\quad X_2(K)$ d) $x_1(n)\ x_2(n) \xleftrightarrow{DFT} \sum_{K=0}^{N-1} X_1(K)X_2(K)$

5. Linear convolution of two sequences N_1 and N_2 produces an output sequence of length

a) $N_1 - N_2 + 1$ b) $N_1 + N_2 - 1$ c) $N_1 + N_2 + 1$ d) $2N_1 - N_2 + 1$[ ]

6. The basic signal flow graph for butterfly computation of DIT-FFT is ……

7. The Fourier transform of discrete time signal is called ……

8. FFT's are based on the …… of an N-point DFT into successively smaller DFT's.

9. The Fourier transform of x(n)*h(n) is equal to ……

10. Appending zeros to a sequence in order to increase the size or length of the sequence is called ……

11. In N-point DFT using radix 2 FFT, the decimation is performed …… times.

12. In 8-point DFT by radix 2 FFT, there are …… stages of computations with …… butterflies per stage.

13. If DFT of x(n) is X(K), then DFT of W_N^{ln} x(n) is …….

14. If xp(n) is periodic sequence with period N and DFS[xp(n)]=xp(k) then DFS[xp(n-m)]Is ……

15.The magnitude and phase angle of is …….. & ……
16. In linearity property DFT[ax1(n)+bx2(n)]= …….
17. Fourier transform gives …… for an A periodic signal
18. Aperiodic sequence xp(n) with fundamental period N can be represented in Fourier transform as ……..
19……. & …… are methods used for circular convolution
20.If X(k) is DFT of a sequence x(n),then DFT of imaginary part of x(n) is …….

ANSWERS

1.a	2.a	3.b	4.b	5.b	6.b	7.adder	8. dierct computation	9. DTFT	10.appending
11.n/2 logn	12.3,2	13.twiddle factor	14.dfs	15.iamg & real	16.a1x1(k)+a2x2(k))	17.energy signal	18.dfs	19.using dft and dft	20.real

FAST FOURIER TRANSFORMS:

1. The DFT of sequence can be evaluated using ……
2. In DFT radix-2 FFT … is the name of domain to be decimated
3. 8. DFS is used to find out the spectrum of ……Signals
4. 9. Number of complex multiplication required to calculate Radix-2 FFT is……..
5. 10…….. is a natural signal
6. 11.A first order LTI system is behaved as……
7. 12.X(n)*[h(n1)+h(n2)]=……
8. 13.Determine step response of the causal system described by difference equation y(n)=y(n-1)+x(n) is …….
9. 14.Idft of x(k)=(1,0,1,0) is ……
10. 15…… is the system function described by the difference equation y[n]=x(n)+2x(n-1)-4x(n-2)+x(n-3)
11. 16. FFT reduces the computation time required to compute ……
12. 17. For DIT, the input is …… while the output is in natural order
13. 18……..&…… Are the applications of FFT algorithm
14. 19.The Twiddle factor exponents are a function of the stage index m and is given by …
15. 20.The number of sets or sections of butterflies in each stage is given by …….

UNIT III: FIR DIGITAL FILTERS :

1. The Linear Phase symmetric Impulse response having even number of samples cannot be used to design the following filter [ ]
   a) Lowpass b) Highpass c) Bandpass d) Bandstop
2. The following filter is always stable [ ]
   a) Butterworth filter b) Chebyshev filter c) II R filter d) FIR filter
3. Which of the filter can be realized in both recursive and non recursive structure?
   a) Butterworth filter b) Chebyshev filter c) II R filter d) FIR filter [ ]
4. Which filter is free of Limit cycle oscillations when implemented on a finite word length digital system [ ]
   a) Butterworth filter b) Chebyshev filter c) II R filter d) FIR filter
5. In which filter the memory requirement and execution time are very high[ ]
   a) Butterworth filter b) Chebyshev filter c) II R filter d) FIR filter

6. Which of the following window is used instead of Hanning window for the same main lobe width [ ]

a) Rectangular window b) Triangular window

c) Hamming window d) Kaiser Window

7. The cascaded form of realization is used [ ]

a) When complex poles with absolute magnitude less than one

b) When complex poles with absolute magnitude greater than one

c) When complex zeros with absolute magnitude less than one

d) When complex zeros with absolute magnitude greater than one

8. In the following window the amplitude of the side lobes is unaffected by the length of the window [ ]

a) Rectangular window b) Triangular window

c) Hamming window d) Kaiser Window

9. In which of the following windows the transition region is more and stop-band attenuation is less [ ]

a) Rectangular window b) Triangular window

c) Hamming window d) Kaiser Window

10. The mainlobe width of the Hanning window is twice that of [ ]

a) Rectangular window b) Triangular window

c) Hamming window d) Kaiser window

11. The Gibbs oscillations are due to [ ]

a) Abrupt truncation of the Fourier series b) No truncation of the Fourier series

c) Abrupt termination of the Fourier transform d) Slow termination of the Fourier series

12. One of the desirable characteristic of the window is that the central lobe of the frequency response of the window should contain [ ]

a) Most of the energy and should be narrow

b) Lowest energy and should be narrow

c) Most of the energy and should be broad

d) Lowest of the energy and should be broad

13. In a window the desirable characteristic is that the sidelobes of the frequency response should [ ]

a) Increase in energy rapidly as ω tends to π

b) Decrease in energy rapidly as ω tends to π

c) Increase in frequency response

d) Contain most of the energy and should be narrow

14. Which window has the advantage of flexibility of sidelobe level and N ? [ ]

a) Rectangular window b) Triangular window

c) Hamming window d) Kaiser window

15. In which filter closed form design equations exist [ ]

a) FIR Filter b) II R Filter c) Butterworth d) Chebyshev

16. In which filter all the poles are located at origin [ ]

a) FIR Filter b) II R Filter c) Butterworth d) Chebyshev

17. In which filter high selectivity can be achieved by using higher order[ ]

a) FIR Filter b) II R Filter c) Butterworth d) Chebyshev

18. Which filter has less flexibility specially for obtaining non-standard frequency response? [ ]

a) FIR Filter b) II R Filter c) Butterworth d) Chebyshev

19. Which filter design methods are iterative procedures that require powerful Computational facilities for Implementation [ ]

a) FIR Filter b) II R Filter c) Butterworth d) Chebyshev

20. Frequency sampling method is suitable for [ ]

a) Broad band frequency selective filters b) Narrow band frequency selective filters

b) Passband frequency selective filters d) Stopband frequency selective filters

21. The frequency sample method can be improved by [ ]

a) Introducing the stopband b) Introducing ripples

c) Introducing the transition samples d) Eliminating the transition samples

22. In the frequency sampling method the Peak sidelobe level can be reduced by

a) Increasing Transition width b) Decreasing Transition width [ ]

c) Increasing Ripples d) Decreasing Ripples

23. In which of the following filter the errors due to round off noise are more [ ]

a) FIR Filter b) II R Filter c) Butterworth d) Chebyshev

24. In which of the following filter the poles are placed any where inside the Unit circle and not always stable is [ ]

a) FIR Filter b) II R Filter c) Butterworth d) Chebyshev

ANSWERS

1.b	2.d	3.d	4.d	5.d	6.c	7.c	8.a	9.b	10.a	11.a	12.a

13.b	14.d	15.b	16.a	17.a	18.b	19.a	20.b	21.c	22.a	23.b	24.b

UNIT IV :IIR FILTERS:

1. The magnitude response of the following filter decreases monotonically as frequency increases [ ]

   a)Butterworth Filter b)Chebyshev type – 1 c)Chebyshev type – 2 d) FIR Filter

2. The transition band is more in [ ]

   a)Butterworth Filter b) Chebyshev type - 1 c) Chebyshev type - 2 d) FIR Filter

3. The poles of Butterworth filter lies on [ ]

   a)sphere b) circle c)ellipse d)parabola

4. I I R digital filters are of the following nature [ ]

   a)Recursive b)Non Recursive c)Reversive d)Non Reversive

5. In I I R digital filter the present output depends on [ ]

   a)Present and previous Inputs only b)Present input and previous outputs only

   c)Present input only d) Present Input, Previous input and output

6. Which of the following is best suited for I I R filter when compared with the FIR filter

   a)Lower sidelobes in stopband b)Higher Sidelobes in stopband [ ]

   c)Lower sidelobes in Passband d)No sidelobes in stopband

   In the case of I I R filter which of the following is true if the phase distortion is tolerable [ ]

   a)More parameters for design b) More memory requirement c)Lower computational Complexity d)Higher computational complexity

7. A causal and stable I I R filter has [ ]

   a)Linear phase b)No Linear phase c)Linear amplitude d) No Amplitude

8. Neither the Impulse response nor the phase response of the analog filter is Preserved in the digital filter in the following method [ ]

   a)The method of mapping of differentials b)Impulse invariant method

   c)Bilinear transformation d)Matched Z - transformation technique

9. Out of the given I I R filters the following filter is the efficient one [ ]

   a)Circular filter b)Elliptical filter c)Rectangular filter d)Chebyshev filter

10. What is the disadvantage of impulse invariant method [ ]

    a)Aliasing b)one to one mapping c) anti aliasing d) warping

11. Which of the I I R Filter design method is antialiasing method? [ ]

a)The method of mapping of differentials b) Impulse invariant method

c) Bilinear transformation d) Matched Z - transformation technique

12. The nonlinear relation between the analog and digital frequencies is called [ ]

a) aliasing b) warping c) prewarping d) antialiasing

13. The most common technique for the design of I I R Digital filter is [ ]

a) Direct Method b) In direct method c) Recursive method d) non recursive method

14. In the design a IIR Digital filter for the conversion of analog filter in to Digital domain the desirable property is [ ]

a)The axis in the s - plane should map outside the unit circle in the z - Plane

b)The Left Half Plane(LHP) of the s - plane should map in to the unit circle in the Z - Plane

c) The Left Half Plane(LHP) of the s-plane should map outside the unit circle in the z-Plane

d) The Right Half Plane(RHP) of the s-plane should map in to the unit circle in the Z - Plane

15. The I I R filter design method that overcomes the limitation of applicability to only Lowpass filter and a limited class of bandpass filters is [ ]

a) Approximation of derivatives b) Impulse Invariance

c) Bilinear Transformation d) Frequency sampling

16. In the Frequency Transformations of the analog domain the transformation is [ ]

a) Low Pass to Lowpass b) Lowpass to Highpass

c) Lowpass to Bandpass d) Lowpass to Bandreject

17. Frequency Transformations in the Analog domain and in the Digital domain will yield

a) Same Results c) Different results for Bilinear Transformation [ ]

b) Different Results d) Different Results except Bilinear Transformation

18. In the Impulse Invariance method the mapping from analog frequency Ω to the digital frequency ω is [ ]

a) one to one b) one to many c) many to many d) many to one

19. A discrete impulse function is applied to the inputs of four different filters. The output sequences of these filters are listed below. Which one of these filters has a pole outside the unit circle? [ ]

a) {1, 2, 3, 4, 5, 6, 0, 0, 0, ... } b) {1, - 1, 1, - 1, 1, - 1, ... }

c) {1, 2, 4, 8, 16, ... } d) {1, 0.5, 0.25, 0.125, ... }

20. A discrete impulse function is applied to the inputs of four different filters. For each of the output sequences that follow, state whether the filter is nonrecursive. [ ]

a) {1, 2, 3, 4, 5, 6, 0, 0, 0 ..... } b) {1, -1, 1, -1, 1, -1 ..... }

c) {1, 2, 4, 8, 16 ..... } d) {1, 0.5, 0.25, 0.125, ... }

21. A filter has the difference equation: y(nt-2T)+x(nT)+x(nT-T). What traditional filter type best describes this filter? [ ]

a) Integrator b) differentiator c) subtractor d) multiplier

ANSWERS

1.a	2.a	3.b	4.a	5.d	6.a	7.c	8.b	9.c	10.b	11.a
12.c	13.b	14.b	15.b	16.b	17.b	18.d	19.d	20.c	21.a	22.a

UNIT V: MULTIRATE SIGNAL PROCESSING:

1. When the input rate F_X is greater than the output rate F_Y in the sampling rate Conversion the Lowpass filter acts as
   a) anti - aliasing pre filter b) anti - imaging post filter
   c) anti - aliasing post filter d) anti - imaging pre filter

2. When the input rate F_X is greater than the output rate F_Y in the sampling rate Conversion the Lowpass filter removes the spectral replicas at multiples of
   a)F_X b) I F_X c) F_Y d) I F_Y

3. An Increase in the sampling rate by an integer factor I can be accomplished by interpolating
   a)I - 1 samples between successive values b) I - 1 samples between alternate values
   c) I - 2 samples between successive values d) I - 2 samples between alternate values

4. For the sampling rate conversion process by a factor of the processes are
   a) First Interpolation and then decimation
   b) First Decimation and then Interpolation
   c) First Extrapolation and then Decimation
   d) First Decimation and then Extrapolation

5. In the Sampling rate conversion both the up sampling filter and down sampling filters can be replaced with a single
   a) Highpass filter b) Bandpass filter c) Lowpass filter d) Bandstop

6. Sampling rate conversion by any rational factor can be obtained with
   a) only decimation b) only interpolation
   c) only extrapolation d) decimation and Interpolation

7. The Process of sampling rate conversion is
   a) Only Resampling b) Only Reconstruction

c) Resampling after Reconstruction d) Reconstruction after Resampling

8. In the decimation process, the down sampling operation in combination with filtering on a linear time invariant system results in
   a) linear time invariant b) Linear time variant
   c) Non Linear time invariant d) Nonlinear time - invaraint

9. The Implementation of sampling rate conversion requires the use of the following Filter
   a) Linear time - invariant filter b) Linear time - variant filter
   c) Non Linear time - Invariant filter d) Non Linear time - variant filter

10. In the Down sampling process the frequency range of the input signal
    a) stretches by a factor D b) compresses by a factor D
    c) stretches by a factor 2D d) compresses by a factor 2D

11. Which of the following is not an application of multirate Digital signal processing?
    a) Digital filter banks b) Subband coding
    c) Broadband filters d) Transmultiplexers

12. The CIC filter structure is
    a) Combinational Impulse Cascade b) Cascade Integrator Comb
    c) Cascade Impulse Comb d) Combinational Integarted Impulse

13. For the development of Polyphase decimator which of the following is used
    a) Commutator b) Decommutator c) Communicator d) Transmitter

14. For the efficient software Implementation of Rational sampling rate conversion the following filter is used
    a) II R filter b) FIR filter c) Butterworth filter d) Chebyshev filter

15. When the output rate F_y is greater than the output rate F_x in the sampling rate Conversion the Lowpass filter removes the spectral replicas at multiples of
    a) F_x b) I F_x c) F_y d) I F_y

16. When the output rate F_y is greater than the output rate F_x in the sampling rate Conversion the Lowpass filter acts as
    a) anti - aliasing prefilter b) anti - imaging postfilter
    c) anti - aliasing postfilter d) anti - imaging prefilter

17. Polyphase filter Structures are used for
    a) Up sampling b) Down sampling
    c) Sampling Rate Conversion d) anti - aliasing

18. The Polyphase filter structures are suitable for
    a) FIR Filters b) II R Filter c) FIR and II R filters d) analog filter

19. The order of the sampling rate converter and a linear time - invariant system can be interchanged by changing
    a) Upsampling rate b) Down sapling rate
    c) Filter system function d) Input function

20. Polyphase filter Structures are used for

a) Up sampling b) Down sampling
c) Sampling Rate Conversion d) anti - aliasing

ANSWERS

1.a	2.c	3.a	4.a	5.c	6.d	7.c	8.b	9. b	10.a
11.c	12b	13a	14.b	15.a	16.b	17.c	18.c	19.c	20.c

FINITE WORD LENGTH EFFECTS:

1. Conversion of a continuous time signal into a digital value produces ……..
2. Errors arising from quantization are ……. & ……
3. In two's compliment numbers negative number is obtained by …….. all the bits of the positive number and adding one to…….
4. Common methods of quantization are …….&……..
5. From the assumptions of the effects of rounding in digital filter error sequence e(N) is …….. signal
6. Quantization step size …….
7. Three quantization errors in finite word length registers are…….
8. …… realization is less sensitive to process of quantization
9. Methods used to prevent over flow are……..
10. A/D converter output is sum of ……&……
11. for two's complement truncation p(e)=……
12. The quantization error is given by……..
13. In one's compliment representation the error for truncation of positive values of the mantissa is……
14. (11)2*11(2)=……
15. the finite coefficients are computed to …….. in the theory
16. the quantization error leads to……..
17. ……. Occurs as a result of the quantization effects in multiplication
18. The amplitudes of the outputs during limit cycles are confined to range of values called as……
19. when a stable IIR digital filter is excited by a finite input sequence the output will ideally decay to……..
20. Application of DFT in Dsp are……

ANSWERS

1.Input quantization error	2.Round off ,Limit cycle oscillations	3.complementing ,least	4.truncation ,rounding	5.white noise

		significant bit		
6.(range of noise)/(no. of quantization levels)	7.i/p quantization errors, coefficient quantization errors, product quantization errors	8.cascade form	9.saturation arthimatic,scaling	10.input signal x(n),error signal
11.p(e)=1/q	12.e(N)=x.q(n)-x(n)	13.0>=mt-m>-2^b	14.(1001)2	15.infinite precision
16.instability	17.limit cycles	18.dead band	19.zero	20spectral analysis and digital filtering

Fundamentals of Artificial Intelligence (21MC0CS01)

III B. Tech II Semester
Academic Year 2023-2024

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(AUTONOMOUS)

III Year B.Tech. II-Sem

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FUNDAMENTALS OF ARTIFICIAL INTELLIGENCE (21MC0CS01)
(Common to CSE, IT, ECE, EEE, ME, CE)

UNIT I: Introduction: What is artificial intelligence, foundations of artificial intelligence, history of artificial intelligence Intelligent Agents – agents and environments, the structure, good behavior: the concept of rationality, the nature of environments, the structure of agents.

UNIT II: Solving Problem by Searching – Problem solving agents, example problems, searching for solutions. Uninformed Search Strategies – Breadth first search, uniform-cost search, depth first search, depth limited search, iterative deepening search, bidirectional search, comparing uninformed search strategies.

UNIT III: Logical Agents – Knowledge-based agents, the Wumpus world, logic, propositional logic: the very simple logic. Knowledge Representation – Introduction, approaches to knowledge representation-relational knowledge, knowledge represented as logic, procedural knowledge, knowledge representation using semantic networks, inheritance in semantic net.

UNIT IV: Expert System & Applications – Introduction, phases in building expert systems-knowledge engineering, knowledge representation, expert systems architecture-knowledgebase, inference engine, knowledge acquisition, expert systems versus traditional systems-characteristics of expert systems, evolution of expert systems, advantages and disadvantages of expert systems, languages for es development., applications of expert systems.

UNIT V: Learning: Machine Learning Paradigm – Introduction, machine learning system-components of learning system, rote learning, learning by taking advice. Supervised & Unsupervised Learning – supervised concept learning, unsupervised concept learning, reinforcement learning.

Text Books (to be acquired by the Students)

Book 1: Artificial Intelligence-A Modern Approach, 3rd Edition, Stuart J. Russel, Peter Marvin, Pearson Education.

Book 2: Artificial Intelligence, Saroj Kaushik, Cengage Publication.

Reference Books

Book 3: Artificial Intelligence, Elaine Rich, Kevin Knight, Shivashankar B. Nair, 3rd Edition, McGraw Hill.

Book 4: Principles of Artificial Intelligence, Nils J. Nilson, Morgan Kaufmann Publishers.

Book 5: Artificial Intelligence, 3rd Edition, Patric Henry Winston, Pearson Education.

Book 6: Artificial Intelligence Illuminated, Ben Coppin, Narosa Publication

Vision & Mission

Vision of the Institution: GURU NANAK INSTITUTIONS TECHNICAL CAMPUS

To be an internationally renowned institution in Engineering, Management, Pharmacy and related fields to produce scientists, engineers, entrepreneurs, leaders, academicians and thinkers of tomorrow with exemplary professional conduct and adherence to ethical values to serve for changing needs of industry and society.

Mission of the Institution: GNITC

M1: Imbibe soft skills, technical skills, creatively and passion in students.

M2: Develop the faculty to reach the International standards.

M3: Maintain outcome based student centric teaching learning with high academic standards and quality that promotes the analytical thinking and independent judgment.

M4: Promote research, innovation, product development by collaborating with reputed industries & reputed universities in India and abroad. Offer collaborative industry programs in emerging areas and instill the spirit of enterprising.

M5: To instill the ethical values in the faculty and students to serve the society.

Department of Electronics and Communications Engineering

Vision of the Department:

To be a premier Department of Electronics and Communication Engineering in the region by providing high quality Education, Research and Employability.

Mission of the Department:

M1: Nurture young individuals into knowledgeable, skillful, and ethical professionals in their pursuit of Electronics and Communication Engineering.

M2: Transform the students through soft skills, excellent teaching learning process and sustain high performance by innovations.

M3: Extensive MoUs with National & Foreign universities to enrich the knowledge of the students & faculty and active participation in Research..

M4: Develop industry-interaction for innovations and product design & development to provide to make the students as innovators, set up the start up units and get good placements

PRE-REQUISITE:

1. A course on "Data Structures

C.CODE	COURSE NAME	DESCRIPTION	SEM
21PC0CS02	Data Structures	As a subset of artificial intelligence, computers' ability to reason, machine learning implies algorithms that learn through training data instead of programming. Specifically, the purpose of machine learning is to add business value via predictions and resolutions by giving computers the ability to learn using data.	II-I

COURSE OBJECTIVES:

1.	The course is introduced to familiarize the basic concepts of artificial intelligence, its relevance in the modern era and various applications.

COURSE OUTCOMES:

SNO	DESCRIPTION
CO1	Identify the importance of artificial intelligence.
CO2	Apply various search strategies to provide efficient solutions for problem space.
CO3	Comprehend various approaches for knowledge representation.
CO4	Employ expert systems for knowledge engineering applications.
CO5	Develop models using machine learning techniques.

TEACHING SCHEDULE

Subject	(21MC0CS01) FUNDAMENTALS OF ARTIFICAL INTELLIGENCE (Mandatory)
Faculty	Mr. B. Samirana Acharya (Assistant.Professor)
Text Books (to be acquired by the Students)	
Book 1	Artificial Intelligence-A Modern Approach, 3rd Edition, Stuart J. Russel, Peter Marvin, Pearson Education.
Book 2	Artificial Intelligence, Saroj Kaushik, Cengage Publication.
Reference Books	
Book 3	Artificial Intelligence, Elaine Rich, Kevin Knight, Shivashankar B. Nair, 3rd Edition, McGraw Hill.
Book 4	Principles of Artificial Intelligence, Nils J. Nilson, Morgan Kaufmann Publishers.
Book 5	Artificial Intelligence, 3rd Edition, Patric Henry Winston, Pearson Education.
Book 6	Artificial Intelligence Illuminated, Ben Coppin, Narosa Publication

Unit	Topic	Chapters					No of Classes
		Book 1	Book 2	Book 3	Book 4	Book 5	
I	Introduction, Intelligent Agents	Ch 1,2	Ch 1	--	--	--	08
II	Solving Problem by Searching, Uninformed Search Strategies	Ch 2	Ch 2	--	--	--	08
III	Logical Agents, Knowledge Representation	Ch 7	Ch 7	--	--	--	08
IV	Expert System & Applications	Ch 16	Ch 8	--	--	--	08
V	Machine Learning Paradigm, Supervised & Unsupervised Learning	Ch 18,21	Ch 11	--	--	--	08
						Contact classes for syllabus coverage	40
Classes for beyond syllabus :02 Descriptive tests: 02 Gaps in the syllabus:02 Tutorial classes: 04							10
Tutorial classes							
Total classes							**50**

COURSE INFORMATION SHEET

PROGRAMME: **CSE**	DEGREE: **B. Tech**
COURSE: **Fundamentals of Artificial Intelligence**	SEMESTER: **II** CREDITS: **0**
COURSE CODE**: 21MC0CS01** REGULATION: **R21**	COURSE TYPE: **Mandatory**
COURSE AREA/DOMAIN: **CSE**	CONTACT HOURS: **3 hours**
CORRESPONDING LAB COURSE CODE (IF ANY): NIL	LAB COURSE NAME: NIL

Mapping of COs with POs and PSOs:

	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2
CO1	0	3	0	1	0	0	0	0	0	0	0	0	0	1
CO2	3	2	2	0	2	3	2	3	0	1	2	0	2	0
CO3	1	1	1	2	0	2	2	0	0	3	1	0	0	2
CO4	3	2	2	1	3	2	1	0	0	1	2	0	2	1
CO5	1	1	3	1	2	0	0	1	0	1	1	3	2	0

GAPS IN THE SYLLABUS - TO MEET INDUSTRY/PROFESSION REQUIREMENTS:

SNO	DESCRIPTION	PROPOSED ACTIONS
1	Automation	Seminar
2	Neural Networks	Seminar

ACTIONS: TOPICS BEYOND SYLLABUS/ASSIGNMENT/INDUSTRY VISIT/GUEST LECTURER/NPTEL ETC

TOPICS BEYOND SYLLABUS/ADVANCED TOPICS/DESIGN:

1	Machine Learning
2	Deep Learning

WEB SOURCE REFERENCES:

1	www.techopedia.com/definition/190/artificial-intelligence-ai
2	www.britannica.com/technology/artificial-intelligence
3	www.investopedia.com/terms/a/artificial-intelligence-ai.asp
4	www.edx.org/micromasters/columbiax-artificial-intelligence
5	https://www.tutorialspoint.com/artificial_intelligence/index.htm
6	https://stfalcon.com/en/blog/post/artificial-intelligence-in-website-developmen

DELIVERY/INSTRUCTIONAL METHODOLOGIES:

✓ PPT & TALK	✓ STUD. ASSIGNMENT-	✓ WEB RESOURCES	✓ VIDEO LECTURES
✓ LCD/SMART BOARDS	✓ STUD. SEMINARS	☐ ADD-ON COURSES	

ASSESSMENT METHODOLOGIES-DIRECT:

✓ASSIGNMENTS	√ STUD. SEMINARS	√ TESTS/MODEL EXAMS	√ UNIV. EXAMINATION
☐ STUD. LAB PRACTICES	☐STUD. VIVA	☐MINI/MAJOR PROJECTS	☐ CERTIFICATIONS
☐ ADD-ON COURSES	☐ OTHERS		

ASSESSMENT METHODOLOGIES-INDIRECT:

√ASSESSMENT OF COURSE OUTCOMES (BY FEEDBACK, ONCE)	✓ STUDENT FEEDBACK ON FACULTY (TWICE)-YES
☐ ASSESSMENT OF MINI/MAJOR PROJECTS BY EXT. EXPERTS	☐ OTHERS

MICROLESSON PLAN

S. No.	Name of the Topic	BTL	Cumulative	Teaching AID	Date
UNIT-1					
1	Introduction – What is artificial intelligence	1	1	Talk & PPT	
2	Foundations of artificial intelligence	2	2	Talk & PPT	
3	History of artificial intelligence	2	3	Talk & PPT	
4	Intelligent Agents	2	4	Talk & PPT	
5	Agents and environments	2	5	Talk & PPT	
6	Good behaviour	2	6	Talk & PPT	
7	The concept of rationality	2	7	Talk & PPT	
8	The nature of environments	2	8	Talk & PPT	
9	The structure of agents	2	9	Talk & PPT	
10	Applications of AI.	1	10	Talk & PPT	
UNIT-2					
11	Solving Problem by Searching	2	11	Talk & PPT	
12	Problem solving agents	2	12	Talk & PPT	
13	Example problems	2	13	Talk & PPT	
14	Searching for solutions	2	14	Talk & PPT	
15	Uninformed Search Strategies	2	15	Talk & PPT	
16	Breadth first search	2	16	Talk & PPT	
17	Uniform-cost search	2	17	Talk & PPT	
18	Depth first search	2	18	Talk & PPT	
19	Depth limited search	2	19	Talk & PPT	
20	Iterative deepening search	2	20	Talk & PPT	
21	Bidirectional search	2	21	Talk & PPT	
22	Comparing uninformed search strategies	4	22	Talk & PPT	
UNIT-3					
23	Logical Agents	2	23	Talk & PPT	
24	Knowledge-based agents	2	24	Talk & PPT	
25	The wumpus world, logic	2	25	Talk & PPT	
26	Propositional logic: the very simple logic	2	26	Talk & PPT	
27	Logical Agents	2	27	Talk & PPT	
28	Knowledge-based agents	2	28	Talk & PPT	
29	The wumpus world, logic	2	29	Talk & PPT	
30	Propositional logic: the very simple logic	2	30	Talk & PPT	
31	Logical Agents, Knowledge-based agents, The wumpus world, logic	2	31	Talk & PPT	
32	Propositional logic: the very simple logic,	2	32	Talk & PPT	

	Knowledge representation – introduction, Approaches to knowledge representation-relational knowledge				
33	Knowledge represented as logic, Procedural knowledge, Knowledge representation using semantic networks,	2	33	Talk & PPT	
34	Inheritance in semantic net	2	34	Talk & PPT	
UNIT-4					
35	Expert System & Applications – Introduction , Phases in building expert systems-knowledge engineering	2	35	Talk & PPT	
36	Knowledge representation, Expert systems architecture-knowledgebase, Inference engine, knowledge acquisition	2	36	Talk & PPT	
37	Expert systems versus traditional systems, Characteristics of expert systems, Evolution of expert systems	2	37	Talk & PPT	
38	Advantages and disadvantages of expert systems, Languages for expert system development, applications of expert systems	1	38	Talk & PPT	
UNIT-5					
39	Machine Learning Paradigm – Introduction, machine learning system	2	39	Talk & PPT	
40	components of learning system, rote learning,	2	40	Talk & PPT	
41	learning by taking advice,	2	41	Talk & PPT	
42	Supervised & Unsupervised Learning	2	42	Talk & PPT	
43	supervised concept learning,	2	43	Talk & PPT	
44	unsupervised concept learning,	2	44	Talk & PPT	
45	Reinforcement learning.	2	45	Talk & PPT	
46	Discussion of previous question papers	5	46	Talk & Chalk	
47	Revision of Unit 1,2	5	47	Talk & PPT	
48	Revision of Unit 3	5	48	Talk & PPT	
49	Revision of Unit 4	5	49	Talk & PPT	
50	Revision of Unit 5	5	50	Talk & PPT	

QUESTION BANK WITH BLOOMS TAXONOMY

Name of the Subject: Fundamentals of Artificial Intelligence
Subject Code : **21MC0CS01**
Name of the Faculty**:** Mr. B. Samirana Acharya
Class: III year II Semester CSE-2,3

BTL- Blooms Taxonomy Level:

Level 1: Remembering
Level 2: Understanding
Level 3: Applying
Level 4: Analyzing
Level 5: Evaluating
Level 6: Creating

PART - A			
Q. No.	**Question**	**BTL**	**Course Outcome**
UNIT - 1			
1	Generalize what is a rational agent?	1	CO1
2	Define Artificial Intelligence?	1	CO1
3	What are the applications of AI?	1	CO1
4	Define an agent? Give example.	1	CO1
5	List the agent types.	1	CO1
6	Write the limitations of AI.	3	CO1
7	Access what is meant by Turing Test?	1	CO1
8	What is specialty of Total Turing Test?	1	CO1
9	Analyze how to measure the performance of an agent?	4	CO1
10	List he properties of environments.	1	CO1
UNIT - 2			
1	State the advantages of Breadth First Search.	1	CO2
2	Define the following terms: 1)Goal test 2) Path 3) Successor function 4) Abstraction	1	CO2
3	What is search? What are the steps for problem solving?	1	CO2
4	Define 1) Initial state 2) state space 3) Path cost	1	CO2
5	Compare BFS and DFS.	4	CO2
6	List the properties of DFS.	1	CO2
7	Give examples for Real World and Toy problems.	1	CO2
8	Express the ways to formulate a problem.	1	CO2
9	List the uninformed search techniques.	1	CO2
10	Write about depth limited search.	3	CO2
UNIT - 3			
1	What is Tautology? Give example.	1	CO3
2	List the elements of propositional logic.	1	CO3
3	Write about parts of knowledge-based agent.	3	CO3
4	Write the properties of good knowledge representation.	3	CO3
5	Give steps to apply declarative for KBA.	1	CO3

6	Express 'I will visit my friend's house if and only if she visits me' in propositional logic	1	CO3
7	Define semantic net. Give example.	1	CO3
8	What are the various approaches for knowledge representation?	1	CO3
9	Translate the sentence into proposition formulae: I spend money only when I buy clothes or I buy vegetables.	1	CO3
10	List the operations knowledge-based agent	1	CO3
UNIT - 4			
1	List out the expert system applications	1	CO4
2	Give characteristics of an expert system.	1	CO4
3	What is knowledge acquisition?	1	CO4
4	Define expert system with components.	1	CO4
5	What is case history?	1	CO4
6	Summarize the capabilities of expert system.	2	CO4
7	How inference engine different from knowledge base? Give reasons.	1	CO4
8	How many phases in building expert systems? Justfy with one example.	1	CO4
9	List the tasks and responsibilities of knowledge Engineer.	1	CO4
10	Write the advantaged and disadvantages of expert systems.	3	CO4
UNIT - 5			
1	Define Rote learning	1	CO5
2	What is learning by taking advice?	1	CO5
3	Define supervised learning.	1	CO5
4	Define unsupervised learning.	1	CO5
5	Define reinforcement learning.	1	CO5
6	What do you understand by training set and test set?	1	CO5
7	What do you understand by machine learning?	1	CO5
8	What is memorization?	1	CO5
9	How is classification different from regression?	1	CO5
10	What is learning?	1	CO5

	PART - B		
Q. No.	**Question**	**BTL**	**Course Outcome**
	UNIT - 1		
1	Design a medical diagnosis system using PEAS factors.	2	CO1
2	Illustrate utility- based agent with an example.	2	CO1
3	Explain environment types with an example.	2	CO1
4	Describe the fundamental concepts of AI.	2	CO1
5	Explain the history of AI.	2	CO1
6	Describe learning agents.	2	CO1
7	a) Differentiate between fully observable Vs. partially observable.	4	CO1
	b) Explain simple reflex agents with example.	2	CO1
8	What is agent program? Discuss different types of agent programs.	2	CO1
9	Summarize Model-based reflex agent.	2	CO1
10	a) Write about goal-based agent.	3	CO1
	b) Distinguish between deterministic Vs. Stochastic.	4	CO1
	UNIT - 2		
1	Explain BFS with an example?	2	CO2
2	Explain DFS with an example?	2	CO2
3	Explain Depth limited search with an example?	2	CO2
4	Describe iterative deepening depth first search.	2	CO2
5	Explain 8-Queen problem	2	CO2
6	Illustrate the Vaccum world problem formulation?	3	CO2
7	Explain infrastructure for search algorithms.	2	CO2
8	Discuss about solution tree with example.	2	CO2
9	Write short notes on: a) Touring problem b) VLSI Layout c) Robot Navigation	3	CO2
10	a) Write about Problem-solving agent	3	CO2
	b) Compare informed and uninformed search.	4	CO2
	UNIT - 3		
1	Differentiate Procedural and Declarative Knowledge.	4	CO3
2	Explain knowledge-based agents.	2	CO3
3	Describe Wumpus world.	2	CO3
4	Explain in detail the connectives used in propositional logic.	2	CO3
5	Draw and describe the semantics network representation with example	2	CO3
6	Write short notes on: a) completeness b) grounding c) soundness	3	CO3
7	Write short notes on: a) Syntax b) Semantics c) Model	3	CO3
8	Describe inheritance in semantic network.	2	CO3
9	Explain knowledge represented as logic with example.	2	CO3
10	Write about programming languages used for knowledge	3	CO3

	representation.		
UNIT - 4			
1	Draw the Expert systems architecture. Explain in detail.	3	CO4
2	List out development languages for system development along with example.	1	CO4
3	Explain applications of Expert systems with example.	2	CO4
4	Write short notes on i. Capabilities of the Expert System ii. Limitations of Expert System	3	CO4
5	Write short notes on i) Inference engine ii) knowledge acquisition iii) Knowledge base System	3	CO4
6	Describe phases in building expert systems.	2	CO4
7	Discuss different knowledge representation schemes for Expert systems.	2	CO4
8	Distinguish between Expert systems Vs Traditional system.	4	CO4
9	Discuss guidelines for Expert system.	2	CO4
10	Explain key characteristics of Expert System.	3	CO4
UNIT - 5			
1	What are the differences between supervised and unsupervised learning	4	CO5
2	Explain Reinforcement learning concept with the help of example	2	CO5
3	Write the various application of machine learning	3	CO5
4	Describe the different types of methods in the learning.	2	CO5
5	How is artificial intelligence and machine learning related? Justify with examples.	4	CO5
6	Draw the diagram of learning system and explain its components.	2	CO5
7	Write short notes on: a) inductive methodology b) deductive methodology	3	CO5
8	Write short notes on: a) clustering b) self-organizing map c) ART	3	CO5
9	Explain supervised concept learning with example.	2	CO5
10	Describe unsupervised concept learning with example.	2	CO5

OBJECTIVE TYPE QUESTIONS

UNIT-1

1. Which particular generation of computers is associated with artificial intelligence?
   a. Second
   b. Fourth
   c. Fifth
   d. Third
2. The characteristics of the computer system capable of thinking, reasoning and learning is known as
   a. machine intelligence
   b. human intelligence
   c. artificial intelligence
   d. virtual intelligence
3. Which of the following is not Properties of Environment?
   a. Discrete / Continuous
   b. Static / Dynamic
   c. Deterministic / Non-deterministic
   d. No agent / Multiple agents
4. What among the following is/are not the example of the intelligent agents?
   a. Human
   b. Robot
   c. Autonomous spacecraft
   d. Hardware
5. Chess is example of which properties?
   a. Discrete
   b. Continuous
   c. Episodic
   d. Non-deterministic
6. The conference that launched the AI revolution in 1956 was held at:
   a. Dartmouth
   b. Harvard
   c. New York
   d. Stanford

7. An agent is composed of _____
    a. Architecture
    b. Agent Function
    c. Perception Sequence
    d. Architecture and Program
8. What of the following is considered to be a pivotal event in the history of AI
    a. 1949, Donald O, The organization of Behaviour,
    b. 1950, Computing Machinery and Intelligence.
    c. 1956, Dartmouth University Conference Organized by John McCarthy
    d. 1961, Computer and Computer Sense.
9. Which of the given language is not commonly used for AI?
    a. LISP
    b. PROLOG
    c. Python
    d. Perl
10. Turing Test is an example of _____.
    a. Systems that think like human
    b. Systems that think rationally.
    c. Systems that act like human
    d. Systems that act rationally
11. What is an AI?
    a. Making a Machine intelligent
    b. Putting your intelligence into Computer
    c. Programming with your own intelligence
    d. putting more memory into Computer
12. What is meant by agent's percept sequence?
    a. Used to perceive the environment
    b. Complete history of actuator
    c. Complete history of perceived things
    d. Input steps
13. Which environment is called as semi dynamic?
    a. Environment does not change with the passage of time
    b. Agent performance changes
    c. Environment will be changed

d. Environment does not change , Agent performance changes

14. What kind of environment is crossword puzzle?
    a. Static
    b. Dynamic
    c. Semi Dynamic
    d. discrete
15. The first AI programming language was called:
    a. BASIC
    b. FORTRAN
    c. IPL
    d. LISP
16. Rational agent always does the right things.
    a. Yes
    b. No
17. A.M. Turing developed ___ technique for testing a computer could or could not demonstrate the artificial Intelligence.
    a. Turing Test
    b. Algorithm
    c. Boolean Algebra
    d. Logarithm
18. _____is the action of task environment in artificial intelligence?
    a. Problem
    b. Solution
    c. Agent
    d. Observation
19. Which of these is agent's perceptual inputs at a given instance.
    a. Behavior of Agent
    b. Percept
    c. Percept Sequence
    d. Agent Function
20. In Artificial Intelligence (AI), which agent deals with happy and unhappy state?
    a. Simple reflex agent
    b. Model based agent
    c. Learning agent

d. Utility based agent

21. ____ were built in such a way that humans had to supply the inputs and interpret the outputs.
    a. Agents
    b. AI system
    c. Sensor
    d. Actuators
22. In _____ year John McCarthy coined the term Artificial Intelligence.
    a. 1950
    b. 1953
    c. 1956
    d. 1959
23. What is Artificial intelligence?
    a. Making a Machine intelligent
    b. Playing a Game
    c. Putting your intelligence into Computer
    d. Programming with your own intelligence
24. A major thrust of AI is in the development of computer functions associated with human intelligence.
    a. TRUE
    b. FALSE
25. The main tasks of an AI agent are_____.
    a. Input and Output
    b. Moment and Humanly Actions
    c. Perceiving, thinking, and acting on the environment
    d. Only percept
26. The conference that launched the AI revolution in 1956 was held at_____
    a. Dartmouth
    b. Harvard
    c. New York
    d. Stanford
27. Chess is example of which properties?
    a. Discrete
    b. Continuous

c. Episodic
d. Non-deterministic

28. Satellite Image Analysis System is
    a. Episodic
    b. Semi-Static
    c. Single agent
    d. Partially Observable
29. Rationality of an agent does not depend on?
    a. performance measures
    b. Percept Sequence
    c. reaction
    d. actions
30. Which of the following areas can not contribute to build an intelligent system?
    a. Neuron science
    b. Maths
    c. Computer Science
    d. Geology
31. Healthy patient is performance measure in _____system.
    a. Human
    b. Robot
    c. Medical diagnostic
    d. Hardware
32. An AI agent perceives and acts upon the environment using___.
    a. Sensors
    b. Perceiver
    c. Actuators
    d. Data
33. _____ is anything that can perceive its environment through sensors.
    a. An agent
    b. Environment
    c. Sensor
    d. Input

34. If a robot is able to change its own trajectory as per the external conditions, then the robot is considered as the__

a. Mobile
b. Non-Servo
c. Open Loop
d. Intelligent

35. How many types of agents are there in artificial intelligence?

a. 1
b. 2
c. 3
d. 4

36. "**A**" in the term PEAS stands for _____

a. Angle
b. Acid
c. Actuator
d. Agent

37. Which of the following is not an application of AI?

a. Intelligent robot
b. data security
c. social media
d. content mining

38. Keyboard entry is _____ in Interactive English Tutor

a. Actuator
b. Sensor
c. environment
d. Algorithm

39. The _____ is application of Artificial Intelligence.

a. social media
b. arrival
c. science
d. source

40. LISP was developed by _____

a. **John McCarthy**
b. Marvin Minsky
c. Alan Turing
d. Allen Newell and Herbert Simon

UNIT-II

1. Which search is implemented with an empty first-in-first-out queue?

a. Depth-first search
b. Breadth-first search
c. Bidirectional search
d. Uniform Cost

2. Which search implements stack operation for searching the states?

a. Depth-limited search
b. Depth-first search
c. Breadth-first search
d. Bidirectional

3. State space is used in representing problem with variable and _____

a. parameter
b. design
c. Definition
d. constant

4. Breadth-first search always expands the _____ node in the current fringe of the search tree.

a. Shallowest
b. Child node
c. Deepest
d. Minimum cost

5. The main function of problem-solving agent is to_____.

a. Solve the given problem and reach the goal
b. not leading to goal state
c. Traveling salesman problem
d. Search environment

6. Which data structure conveniently used to implement BFS?

a. Stacks
b. Queues
c. Priority Queues
d. Trees

7. Another name for uninformed search is

a. Heuristic search
b. Uniform-cost search
c. Blind search
d. Depth limited search

8. Is optimality and completeness exist in bidirectional search algorithm?

a. Yes, Yes
b. No, Yes
c. Yes, No
d. No, No

9. Goal-based agents use more advanced _____representation.

a. Simple-action rule.
b. Structured
c. Condition-action rule
d. No rule

10. A _____cost is assigned to each path in path cost function.

a. step
b. uniform
c. numeric
d. path

11. The Process of deciding what actions and states to consider given a goal is called ____

a. Problem formulation
b. Goal formulation
c. Solution
d. Goal-seeking

12. In _____ problem, to find the shortest path, each city must be visited once only.

    a. Map coloring Problem
    b. Depth-first search traversal on a given map represented as a graph
    c. Finding the shortest path
    d. Travelling Salesman problem

13. What is the space complexity of Depth-first search?

    a. O(b)
    b. O(bl)
    c. O(m)
    d. O(bm)

14. The process of looking for a sequence of actions that reaches the goal is called _____

    e. assumption
    f. Model
    g. Learning
    h. search

15. Which of the following searching technique takes less memory?

    a. Optimal search
    b. Breadth-First Search
    c. Linear Search
    d. Depth-First Search

16. The starting position of "Play Chess" can be described as an _____.

    a. 8X8 array
    b. 16X16 array
    c. 9X9 array
    d. 10X10 array

17. People actually care about_____ problems.

    a. Toy
    b. Real-world
    c. dummy
    d. game

18. One definition of AI focuses on problem solving methods that process:

a. smell

b. symbols

c. touch

d. algorithms

19. Which search algorithm imposes a fixed depth limit on nodes?

a. Depth-limited search

b. Depth-first search

c. Iterative deepening search

d. Bidirectional search

20. LIFO is _____ where as FIFO is _____

a. Stack, Queue

b. Queue, Stack

c. Priority Queue, Stack

d. Stack. Priority Queue

21. ___ algorithm searches forward from initial state and backward from goal state till both meet to identify a common state?

a. Uniform Cost Search

b. Iterative Deepening Depth-First Search

c. Bidirectional Search

d. Breadth First Search

22. Uniform-cost search expands the node n with the _____

a. Lowest path cost

a. Heuristic cost

b. Highest path cost

c. Average path cost

23. _____quality is measured by the path cost function.

a. search

b. Solution

c. problem

d. environment

24. Iterative Deepening Search is a form of

a. Depth limited Search

b. Breadth First Search

c. Best First Search

d. Linear search

25. The 8-puzzle problem consists of _____ board.

a. 4X4

b. 3X3

c. 2X4

d. 8X8

26. _____is used to provide the feedback to the learning element.

a. Critic

b. Actuators

c. Sensor

d. Environment

27. Example for route-finding problems is _____ system.

a. Out-car

b. Agent Program

c. In-car

d. In-out car

28. 8-puzzle belongs to the family of _____puzzles

a. Hybrid

b. Sliding-block

c. Relational

d. complete

29. There are _____ kind of formulation.

a. 3

b. 4

c. 2

d. 5

30. What is Branching Factor?

a. Length of the shortest path from initial state to goal state.
b. **The average number of child nodes in the problem space graph**.
c. A property of an algorithm to always find an optimal solution.
d. None of the Above

31. The Travelling Salesman problem is a touring problem in which each city must be visited exactly _____

a. Twice
b. Once
c. Thrice
d. 4 times

32. The VLSI Layout problem usually split into _____parts.

a. Three
b. Four
c. Two
d. Five

33. How many types are available in uninformed search method?

a. 3
b. 4
c. 5
d. 6

34. A search algorithm takes _____ as an input and returns _____ as an output.

a. Input, output
b. Problem, solution
c. Solution, problem
d. Parameters, sequence of actions

35. Depth-first search always expands the _____ node in the current fringe of the search tree.

a. Shallowest
b. Child node
c. Deepest
d. Minimum cost

36. _____ is Initial state + Goal state in Search Terminology.

a. Problem Space

b. Problem Instance

c. Problem Space Graph

d. Admissibility

37. When is breadth-first search is optimal?

a. When there is less number of nodes

b. When all step costs are equal

c. When all step costs are unequal

d. When path costs are equal

38. Depth-limited search can be implemented as a _____algorithm.

a. iterative

b. simple-recursive

c. fixed

d. Utility

39. The process of removing detail from a given state representation is called _____

a. Extraction

b. Abstraction

c. Information Retrieval

d. Mining of data

40. No information given about the problems in _____ search algorithms.

a. informed

b. Semi-Static

c. iterative

d. Uninformed

UNIT-III

1. The central component of knowledge-based agent is ___.

   a. logic

   b. **Knowledge-base**

   c. language

   d. database

2. _____ is deriving new sentences from old.

a) results

b) phrases

c) pages

d) inference

3. The _____ world is cave consisting of rooms connected by passageways.

   a) Vaccum

   b) Wumpus

   c) 8-puzzle

   d) toy

4. The terrible Wumpus is a _____ that eats anyone who enters its room.

   a) **beast**

   b) wild animal

   c) killer tree

   d) Shark

5. The agent perceives stench means, there is Wumpus in nearby _____.

   a) Fillers

   b) pillars

   c) rooms

   d) values

6. The semantics define the _____of each sentence w.r.t. each possible world.

   a) table

   b) relation

   c) case

   d) truth

7. Real world problems can be easily represented as _____ propositions.

   a. logical

   b. physical

   c. predicate

   d. not

8. The relation between a sentence and another sentence is called_____.

   a. Logic

   b. Completeness

   c. Entailment

   d. grounding

9. _____ is connection between logical reasoning and real-world.
    a. Preserving
    b. Checking
    c. Understanding
    d. grounding
10. _____sentences are constructed from simpler sentences.
    a. Complex
    b. Common
    c. Uncommon
    d. allowable
11. A square is _____there exists a pit in neighboring square.
    a. Stench
    b. Breezy
    c. Non-breezy
    d. Non-stenchy
12. An algorithm that derives only entailed sentences is called _____
    a. Check
    b. Beck
    c. Sound
    d. ground
13. _____ is used to construct the complex sentences.
    a) Symbols
    b) Connectives
    c) Logical connectives
    d) All of the mentioned
14. How many logical connectives are there in artificial intelligence?
    a) 2
    b) 3
    c) 4
    d) 5
15. Which is used to compute the truth of any sentence?
    a) Semantics of propositional logic
    b) Alpha-beta pruning

c) First-order logic

d) Both Semantics of propositional logic & Alpha-beta pruning

16. _____bases consist of sentences.

a) Data

b) **knowledge**

c) military

d) tutorial

17. Soundness is a highly _____property.

a. Not desirable

b. basic

c. desirable

d. moderate

18. Function _____is used to add sentence into KB.

a. ask

b. query

c. verify

d. Tell

19. In the _____ approach one can verify the correctness of new statements.

a. Graphical

b. Logical

c. Model

d. Table

20. The details of the inference mechanism are hidden inside TELL and_____.

a. ASK

b. Make

c. Query

d. Entailment

21. Instance and isa are two important attributes which supports property of ____

a) Inheritance

b) polymorphism

c) encapsulation

d) none

22. A Semantic network is _____.

a) **A way of representing knowledge**

b) Data Structure

c) Data Type

d) None of the mentioned

23. The _____ theory provides a good basis for understanding frame systems.

a) Goal

b) set

c) strong

d)weak

24. The semantics define the _____of each sentence w.r.t. each possible world.

a) table

b) relation

c) case

d) truth

25. There exists _____way to infer using semantic networks.

a) 1

b)2

c)3

d)4

26. Prolog is developed in the year_____.

b. 1975

c. 1972

d. 1976

e. 1978

27. In _____, information is represented as a set of nodes connected by arcs.

a. Syntax

b. Graph

c. Table

d. Semantic net

28. _____ handles electronic documents in web systems.

a. SGML

b. Prolog

c. Lisp

d. KL-One

29. _____ is used to construct the complex sentences.

a) Symbols

b) Connectives

c) Logical connectives

d) All of the mentioned

30. _____ Quantifiers are there in artificial intelligence.

a) 1

b) 2

c) 3

d) 4

31. How many logical connectives are there in artificial intelligence?

a) 2

b) 3

c) 4

d) 5

32. Which is used to compute the truth of any sentence?

a) Semantics of propositional logic

b) Alpha-beta pruning

c) First-order logic

d) Both Semantics of propositional logic & Alpha-beta pruning

33. In the _____logic, knowledge is represented in the form of rules and facts.

a. Propositional

b. Predicate

c. First-order

d. relational

34. The main function of knowledge structures is to provide_____.

a. Domain

b. Expertise

c. Represent

d. infer

35. _____ is part of relational knowledge.

a. Row

b. Column

c. Table

d. graph

e.

36. Knowledge base can be organized into _____ structure in extended KR.

a**. hierarchical**

b. graphical

c. table

d. model

37. ____ in semantic net represents concepts.

a. arc

b. **node**

c. label

d. edge

38. _____node represents objects in the semantic net.

a. Oval

b. Rectangle

c. Circle

d. square

39. Property links are shown as_____ lines for more clarity in semantic net.

a. Solid

b. Dotted

c. Dashed

d. simple

40. ____ language is used to implement semantic net.

a. **Prolog**

b. KL-one

c. SGML

d. lisp

UNIT-IV

1. Which of the following is not a Capabilities of Expert Systems?
   a. Advising
   b. Demonstrating
   c. Explaining
   d. **Expanding**

2. Which of the following are Components of Expert Systems?

   a. Knowledge Base
   b. Inference Engine
   c. User Interface
   d. All of the above

3. Which of the following is incorrect application of Expert System?

   A. Design Domain
   B. Monitoring Systems
   C. Knowledge Domain
   D. Systems domain

4. Which of the following is not a benefits of Expert Systems?

   A. Availability
   B. Speed
   C. Time
   D. Less Error Rate

5. What is the form of Knowledge representation?

   A. IF-THEN
   B. IF-THEN-ELSE
   C. IF-ELSE
   D. All of the above

6. Which of the following is not a Characteristics of Expert Systems?

   A. Understandable
   B. Highly responsive
   C. Unreliable
   D. High performance

7. Which of the following is Capabilities of Expert Systems?

   A. Possessing human capabilities
   B. Suggesting alternative options to a problem
   C. Refining their own knowledge
   D. Substituting human decision makers

8. How many Components of Knowledge Base are there?

A. 2
B. 3
C. 4
D. 5

9. Which of the following is incorrect Expert Systems Limitations?

A. Limitations of the technology
B. Difficult knowledge acquisition
C. Easy to maintain
D. High development costs

10. A _____ is nothing but an expert system without knowledge base.

A. Tools
B. shell
C. Expert System
D. knowledge

11. Data, information, and past experience combined together are termed as _____.

A.Inference
B. Acquisition
C. vision
D. knowledge

12. Expert systems are meant to solve _____ problems.
a. Real-world
b. toy
c. maths
d. chemistry

13. The application/applications of Artificial Intelligence is/are

a) Expert Systems
b) Gaming
c) Vision Systems
d) All of the above

14. Among the given options, which is not the required property of Knowledge representation?

a. Inferential Efficiency

b. Inferential Adequacy

c. Representational Verification

d. Representational Adequacy

15. Which of the following is an advantage of using an expert system development tool?
a) imposed structure
b) knowledge engineering assistance
c) rapid prototyping
d) all of the mentioned

16. An expert system is __

a. **a computer that can answer questions like a human expert**

b. a group of scientists who design computer programs

c. a method of producing new words
d. a computer that can feel emotion

17. The explanation facility of an expert system may be used to _____
a) construct a diagnostic model
b) expedite the debugging process
c) explain the system's reasoning process
d) explain the system's reasoning process & expedite the debugging process

18. ----------are knowledge based system to which present rules are applied to solve a particular problem.
a. Expert System
b. AI
c. KBS
d.Base Rule 0

19. Which of the following is not true about expert systems ?

a. Expert systems are collection of human knowledge.

b. Expert systems are expensive too design.

c. Expert system are usually designed to run on small general purpose computers.

d. Maintenance support may be difficult to obtain for an expert system.

20. ---------- attempt to provide the same judgmental advice that human experts such as doctors provide.

1. Expert System

2. AI

3. KBS

4. RAND

21. Expert system are part of the general area of research known as ----------

a. AI

b. ES

c. STUDENT

d. RAND

22. _____ system is used to diagnose bacterial infection.

a. Miner

b. **MYCIN**

c. EMYCIN

d. Puff

23. ____Phases are there in ES.

a. 4

b. 6

c. **5**

d. 7

24. _____ phase is used by knowledge engineer to determine important features.

a. testing

b. conceptualization

c. formalization

d. **identification**

25. Building an ES process is often referred as _____ engineering.

a. chemical

b. **knowledge**

c. computer science

d. electrical

26. _____ phase involves evaluating performance of system.

a. modeling

b. identification

c. **testing**

d. verification

27. There are ___ ways of knowledge engineering.

a. **different**

b. same

c. logical

d. modeling

28. Knowledge engineer and domain expert _____to produce an ES.

a. fight

b. **interacts**

c. phase

d. creates

29. Domain expert receives _____ from knowledge engineer.

a. responses

b. rules

c. **queries**

d. test

30. The knowledge engineer extracts ____rules from discussion held with experts.

a. specific

b. **general**

c. facts and

d. goal

31. Close collaboration with _____users are must in ES.

a. multiple

b. single

c. **end**

d. no

32. The _____of ES is the powerful corpus of knowledge.

a. brain

b. database

c. work

d. **heart**

33. The ____ is another widely used representation in ES.

a. **unit**

b. digit

c. number

d. network

34. The current knowledge acquisition methods are _____and tedious.

a. fast

b. **slow**

c. moderate

d. weak

35. Case specific data is included in _____ memory.

a. volatile

b. non-volatile

c. **working**

d. fixed

36. ___ knowledge consists of facts and rules.

a. dynamic

b. movable

c. process

d. **static**

37. Forward chaining is also known as _____ method.

a. **data-driven**

b. goal

c. specific

d. inference

38. OPS5 is based on _____reasoning.

a. backward-chaining

b. **forward-chaining**

c. both

d. none

39. Different cases with solutions are stored in _____Base System.

a. data

b. logic

c. **Case**

d. word

40. LISP is based on _____calculus.

a. Differential

b. integral

c. beta

d. **lambda**

UNIT-5

1. What is Machine learning?

a) The autonomous acquisition of knowledge through the use of computer programs

b) The autonomous acquisition of knowledge through the use of manual programs

c) The selective acquisition of knowledge through the use of computer programs

d) The selective acquisition of knowledge through the use of manual programs

2. Which of the factors affect the performance of the learner system does not include?

a) Representation scheme used

b) Training scenario

c) Type of feedback

d) Good data structures

3. Different learning methods does not include?

a) Memorization

b) Analogy

c) Deduction

d) Introduction

4. How many things are concerned in the design of a learning element?

a) 1

b) 2

c) 3

d) 4

5. What is used in determining the nature of the learning problem?

a) Environment

b) Feedback

c) Problem

d) All of the mentioned

6. Automated vehicle is an example of _____

a) Supervised learning

b) Unsupervised learning

c) Active learning

d) Reinforcement learning

7.Which of the following is an example of active learning?

a) News Recommender system

b) Dust cleaning machine

c) Automated vehicle

d) None of the mentioned

8. In which of the following learning the teacher returns reward and punishment to learner?

a) Active learning

b) Reinforcement learning

c) Supervised learning

d) Unsupervised learning

9.Which of the following is the component of the learning system?

a) Goal

b) Model

c) Learning rules

d) All of the mentioned

10.Which of the following is also called exploratory learning?

a) Supervised learning

b) Active learning

c) Unsupervised learning

d) Reinforcement learning

11. In an Unsupervised learning _____

a) Specific output values are given

b) Specific output values are not given

c) No specific Inputs are given

d) Both inputs and outputs are given

12. How many types of Machine Learning are there?

a) 1

b) 2

c) 3

d) 4

13. What is Machine learning?

a) The autonomous acquisition of knowledge through the use of computer programs

b) The autonomous acquisition of knowledge through the use of manual programs

c) The selective acquisition of knowledge through the use of computer programs

d) The selective acquisition of knowledge through the use of manual programs

14.Which of the factors affect the performance of the learner system does not include?
a) Representation scheme used

b) Training scenario

c) Type of feedback

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15.Different learning methods does not include?
a) Memorization

b) Analogy

c) Deduction

d) Introduction

16.How many things are concerned in the design of a learning element?
a) 1

b) 2

c) 3

d) 4

17. What is used in determining the nature of the learning problem?
a) Environment

b) Feedback

c) Problem

d) All of the mentioned

18.The components of learning systems are_____
a. **6**

b. 5

c. 7

d. 4

19.The job of _____is to inform performance to learning component.
a. user

b. **critic**

c. manager

d. tester

20. In which of the following learning the teacher returns reward and punishment to learner?
a) Active learning

b) Reinforcement learning

c) Supervised learning

d) Unsupervised learning

21.Which of the following is the component of the learning system?
a) Goal

b) Model

c) Learning rules

d) All of the mentioned

22.Which of the following is also called exploratory learning?
a) Supervised learning

b) Active learning

c) Unsupervised learning

d) Reinforcement learning

23. In an Unsupervised learning _____
a) Specific output values are given

b) Specific output values are not given

c) No specific Inputs are given

d) Both inputs and outputs are given

24.How many types of Machine Learning are there?

a. 1

b. 2

c. 3

d. 4

25. _____learning involves one-to-one mapping.

a. **Rote**

b. supervised

c. unsupervised

d. none

26. Which ONE of the following are regression tasks?

A) Predict the age of a person

B) Predict the country from where the person comes from

C) Predict whether the price of petroleum will increase tomorrow

D) Predict whether a document is related to science

27. Which of the following is a supervised learning problem?

A) Grouping people in a social network.

B) Predicting credit approval based on historical data

C) Predicting rainfall based on historical data

D) all of the above

28. One of the most common uses of Machine Learning today is in the domain of _____.

A) Expert system

B) Unsupervised learning

C) Combination of supervised and unsupervised learning

D) Robotics

29. To make the _____manageable information is generalized.

a. solution

b. **problem**

c. program

d. system

30. In regression the output is

A) Discrete.

B) Continuous and always lies in a finite range.

C) Continuous.

D) May be discrete or continuous.

31. What category of machine learning algorithm finds patterns in the data when the data is not labeled?

a) Data prophecy
b) Unsupervised learning
c) Supervised learning
d) Semi Supervised learning

32. ML is the field of AI consisting of learning algorithm that

a) Improve their performance
b) At executing come task
c) Over time with experience
d) All of above

33. There are ___ basic approaches to advice taking.

a. three

b. four

c. **two**

d. five

34. In many programs, ____evaluation functions can be used to reduce search space.

a. **static**

b. dynamic

c. maths

d. engineering

35. Both inputs and ____are observed in supervised learning.

a. learning

b. testing

c. **outputs**

d. middle nodes

36. There is no information available about the _____outputs in the unsupervised learning.

a. wrong

b. **correct**

c. no

d. more

37. Arthur Samuel developed _____playing program.

a. Chess

b Tic-tac-toe

b. Checker

c. Go

38. In the ____model, the number of clusters can be varied according to the problem size.

a. SOM

b. Back-Prop

c. CNN

d. **ART**

39. _____ function is part of reinforcement learning.

a. goal

b. math

c. **utility**

d. sigmoid

40. ART networks are used in _____recognition tasks.

a. **pattern**

b. task

c. goal

d. letter

Guru Nanak Institutions Technical Campus

School of Engineering and Technology

Ibrahimpatnam, R R District, Telangana – 501506

MICROCONTROLLERS AND APPLICATIONS (21ES0EC30) HANDBOOK

B.TECH. [III/ II]

Academic Year: 2023-2024

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHOOL OF ENGINEERING AND TECHNLOGY

HANDBOOK -MCA

SUBJECT: **MICROCONTROLLERS AND APPLICATIONS**

PROGRAMME: Electronics and Communication Engineering	DEGREE: BTECH
COURSE: Microcontrollers And Applications	SEMESTER: II CREDITS: 3
COURSE CODE: 21ES0EC30 REGULATION: R21	COURSE TYPE: CORE
COURSE AREA/DOMAIN: CORE	CONTACT HOURS: 4+1(Tutorial)
CORRESPONDING LAB COURSE CODE (IF ANY): 21PC0EC17	LAB COURSE NAME: Microcontrollers And Applications Lab

SYLLABUS

GURU NANAK INSTITUTIONS TECHNICAL CAMPUS

(AUTONOMOUS)

III Year B. Tech. Sem-II **L T P C**

3 0 0 3

MICRO CONTROLLERS AND APPLICATIONS

PRE-REQUISITES

1. A course on “Computer Organization and Architecture”
2. A course on “Analog and Digital Electronics”

COURSE OBJECTIVE

This course is intended to make familiar with the architecture and the instruction set of an Intel microprocessor and Assembly language programming will be studied as well as the design of various types of digital and analog interfaces with understanding the architecture of Microcontrollers.

SYLLABUS

UNIT - I

Introduction to Microprocessor: 8086 Architecture: 8086 Architecture-Functional diagram, Register Organization, Memory Segmentation, Programming Model, Memory addresses, Physical Memory Organization, Architecture of 8086, Signal descriptions of 8086, interrupts of 8086.

Instruction Set and Assembly Language Programming of 8086: Instruction formats, addressing modes, Instruction Set and Simple Programs involving Logical, Branch and Call Instructions, Sorting, String Manipulations.

UNIT - II

Introduction to Microcontrollers: Overview of 8051 Microcontroller, Architecture, I/O Ports, Memory Organization, Addressing Modes and Instruction set of 8051.

8051 Real Time Control: Programming Timer Interrupts, Programming External Hardware Interrupts, Programming the Serial Communication Interrupts, Programming 8051 Timers and Counters.

UNIT - III

I/O And Memory Interface: LCD, Keyboard, External Memory RAM, ROM Interface, ADC, DAC Interface to 8051.

Serial Communication and Bus Interface: Serial Communication Standards, Serial Data Transfer Scheme, On board Communication Interfaces-I2C Bus, SPI Bus, UART; External Communication Interfac11es-RS232, USB.

UNIT - IV

ARM Architecture: ARM Processor fundamentals, ARM Architecture – Register, CPSR, Pipeline, exceptions and interrupts interrupt vector table, ARM instruction set – Data processing, Branch instructions, load store instructions, Software interrupt instructions, Program status register instructions, loading constants, Conditional execution, Introduction to Thumb instructions.

UNIT - V

Advanced ARM Processors: Introduction to CORTEX Processor and its architecture, OMAP Processor and its Architecture.

TEXT BOOKS

1. Douglas V Hall, Microprocessors Interfacing, Tata McGraw Hill, 1991.
2. Microcontrollers programming by Tularam M. Bansod Pratik Tawde.

REFERENCE BOOKS:

1. D A Patterson and J H Hennessy, "Computer Organization and Design The

hardware and software interface. Morgan Kaufman Publishers.
2. Kenneth J. Ayala, The 8051 Microcontroller, Penram International Publishing, 1996.

COURSE OUTCOMES

By the end of the course, students will be able to:

CO 1: Understand microprocessor and micro controller architectures.

CO 2: Do assembly language programming.

CO 3: Do interfacing design of peripherals like, I/O, A/D, D/A, timer etc.

CO 4: Develop systems using different microcontrollers.

CO 5: Understand RSIC processors and design ARM microcontroller-based systems.

Vision & Mission

Vision of the Institution: GURU NANAK INSTITUTIONS TECHNICAL CAMPUS

To be an internationally renowned institution in Engineering, Management, Pharmacy and related fields to produce scientists, engineers, entrepreneurs, leaders, academicians and thinkers of tomorrow with exemplary professional conduct and adherence to ethical values to serve for changing needs of industry and society.

Mission of the Institution: GNITC

M1: Imbibe soft skills, technical skills, creatively and passion in students.

M2: Develop the faculty to reach the International standards.

M3: Maintain outcome based student centric teaching learning with high academic standards and quality that promotes the analytical thinking and independent judgment.

M4: Promote research, innovation, product development by collaborating with reputed industries & reputed universities in India and abroad. Offer collaborative industry programs in emerging areas and instill the spirit of enterprising.

M5: To instill the ethical values in the faculty and students to serve the society.

Department of Electronics and Communications Engineering

Vision of the Department:

To be a premier Department of Electronics and Communication Engineering in the region by providing high quality Education, Research and Employability.

Mission of the Department:

M1: Nurture young individuals into knowledgeable, skillful, and ethical professionals in their pursuit of Electronics and Communication Engineering.

M2: Transform the students through soft skills, excellent teaching learning process and sustain high performance by innovations.

M3: Extensive MoUs with National & Foreign universities to enrich the knowledge of the students & faculty and active participation in Research..

M4: Develop industry-interaction for innovations and product design & development to provide to make the students as innovators, set up the start up units and get good placements

Model Lesson Plan/Consolidated Unit Wise Lesson Plan

Subject	MICROCONTROLLERS AND APPLICATIONS (21ES0EC30)				
Faculty	R. SANDEEP REDDY				
Text Books (to be acquired by the students)					
Book-1	Douglas V Hall, Microprocessors Interfacing, Tata McGraw Hill, 1991.				
Book-2	Microcontrollers programming by Tularam M. Bansod Pratik Tawde				
Reference Books					
Book-3	D A Patterson and J H Hennessy, "Computer Organization and Design The hardware and software interface. Morgan Kaufman Publishers.				
Book-4	Kenneth J. Ayala, The 8051 Microcontroller, Penram International Publishing, 1996.				
Unit	Topic	Chapters			No of Classes
		Book 1	Book 2	Book 3	
I	8086 Architecture: Instruction Set and Assembly Language Programming of 8086	1		1,4,5	15
II	Introduction to Microcontrollers 8051 Real Time Control	2		6	10
III	I/O And Memory Interface Serial Communication and Bus Interface	2		6	12
IV	ARM Architecture	3,6	7	8	10
V	Advanced ARM Processors	3	7	8	08
Contact classes for syllabus coverage					55
Tutorial Classes					15
Descriptive Tests					02
Classes for beyond syllabus					03

Remedial Classes/NPTEL	05
Total Number of Classes	**80**

MICRO LESSON PLAN

Lecture Plan with Blooms Taxonomy

Name of the Subject : **MICROCONTROLLERS AND APPLICATIONS**
Subject Code : **(**21ES0EC30**)**
Name of Faculty : R.SANDEEP REDDY
Class & section : III year IOT

BTL- Blooms Taxonomy Level
Level 1 - Remembering
Level 2- Understanding
Level 3- Applying
Level 4- Analyzing
Level 5- Evaluating
Level 6- Creating

Cumulative Periods	Time (Min)	Topics	BTL	Teaching – Learning Method
Unit-I: Introduction to Microprocessor				
1	10	Evaluation of microprocessor and introduction of 8085 microprocessor	1	Chalk & Talk/PPT
	20	**8086 Architecture:** 8086 Architecture-Functional diagrams	1	Chalk & Talk/PPT
	20	BIU, EU	1	Chalk &Talk/PPT
2	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	Register Organization	2	Chalk & Talk/PPT
	20	General purpose & special purpose registers	3	Chalk &Talk/PPT
3	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	Memory Segmentation	2	Chalk & Talk/PPT

	20	Overlapping & non overlapping segments	3	Chalk &Talk/PPT
4	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Programming Model	2	Chalk & Talk/PPT
	20	Memory addresses	2	Chalk &Talk/PPT
5	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Physical Memory Organization,	2	Chalk & Talk/PPT
	20	Even address bank & odd address bank	3	Chalk &Talk/PPT
6	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Signal descriptions of 8086,	3	Chalk & Talk/PPT
	20	Minimum mode & maximum mode pins	3	Chalk &Talk/PPT
7	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	interrupts of 8086.	2	Chalk & Talk/PPT
	20	External interrupt & Internal interrupt	3	Chalk &Talk/PPT
8	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	**Instruction Set and Assembly Language Programming of 8086**	2	Chalk & Talk/PPT
	20	Instruction formats	3	Chalk &Talk/PPT
9	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Addressing modes	2	Chalk & Talk/PPT
	20	Direct,indirect addressing modes	2	Chalk &Talk/PPT
10	10	Revision of previous topic	1	Chalk & Talk/PPT
	20	Instruction Set	1	Chalk & Talk/PPT
	20	Data transfer instructions	1	Chalk &Talk/PPT
11	10	Revision of previous topic	1	Chalk & Talk/PPT
	20	Simple Programs involving Logical instructions	2	Chalk & Talk/PPT

	20	Simple Programs involving Branch Instructions.	2	Chalk & Talk/PPT
12	10	Revision of previous topic	2	Chalk &Talk/PPT
	20	Simple Programs involving Sorting, String Manipulations	3	Chalk & Talk/PPT
	20	Simple programs	3	Chalk & Talk/PPT
UNIT II: **Introduction to Microcontrollers**				
13	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	**Introduction to Microcontrollers:** Overview of 8051 Microcontroller,	3	Chalk & Talk/PPT
	20	Features of 8051 microcontroller	3	Chalk &Talk/PPT
14	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	Architecture of 8051	2	Chalk & Talk/PPT
	20	Functional diagram	3	Chalk &Talk/PPT
15	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	I/O Ports	2	Chalk & Talk/PPT
	20	Memory Organization	3	Chalk &Talk/PPT
16	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	Addressing Modes	2	Chalk & Talk/PPT
	20	Direct & indirect addressing mode	3	Chalk &Talk/PPT
17	10	Revision of previous topic	1	Chalk & Talk/PPT
	20	Instruction set of 8051.	2	Chalk & Talk/PPT
	20	Data transfer instructions	2	Chalk &Talk/PPT
18	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	**8051 Real Time Control**	2	Chalk & Talk/PPT
	20	Programming Timer Interrupts	3	Chalk &Talk/PPT
19	10	Revision of previous topic	0	Chalk & Talk/PPT

	20	Programming Timer Interrupts	2	Chalk & Talk/PPT
	20	Programs	2	Chalk &Talk/PPT
20	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Programming External Hardware Interrupts	2	Chalk & Talk/PPT
	20	Programs	2	Chalk & Talk/PPT
21	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Programming 8051 Timers	2	Chalk &Talk/PPT
	20	and Counters	2	Chalk & Talk/PPT
22	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Programming 8051 Timers and Counters	1	Chalk &Talk/PPT
	20	and Counters	2	Chalk & Talk/PPT
23	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Programming the Serial Communication Interrupts	2	Chalk &Talk/PPT
	20	programs	2	Chalk & Talk/PPT
24	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Programming the Serial Communication Interrupts	2	Chalk &Talk/PPT
	20	programs	2	Chalk & Talk/PPT
UNIT III: **I/O And Memory Interface**				
25	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	**I/O And Memory Interface** .	1	Chalk & Talk/PPT
	20	LCD interface	2	Chalk &Talk/PPT
26	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Keyboard	3	Chalk & Talk/PPT

	20	Keyboard interface	2	Chalk &Talk/PPT
27	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	External Memory RAM	2	Chalk & Talk/PPT
	20	ROM Interface	2	Chalk &Talk/PPT
28	10	Revision of previous topic	1	Chalk & Talk/PPT
	20	ADC Interface to 8051.	2	Chalk & Talk/PPT
	20	DAC Interface to 8051.	2	Chalk &Talk/PPT
29	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	**Serial Communication and Bus Interface:**	2	Chalk & Talk/PPT
	20	Serial Communication Standards	2	Chalk &Talk/PPT
30	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Serial Data Transfer Scheme	2	Chalk & Talk/PPT
	20	Serial Data Transfer Scheme	3	Chalk &Talk/PPT
31	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	On board Communication Interfaces-	2	Chalk & Talk/PPT
	20	-I2C Bus	1	Chalk &Talk/PPT
32	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	SPI Bus	2	Chalk & Talk/PPT
	20	SPI Bus	2	Chalk &Talk/PPT
33	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	UART	2	Chalk & Talk/PPT
	20	UART	2	Chalk &Talk/PPT
34	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	External Communication Interfaces-	2	Chalk & Talk/PPT
	20	RS232	2	Chalk &Talk/PPT

35	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	USB.	2	Chalk & Talk/PPT
	20	External Communication Interfaces-	3	Chalk &Talk/PPT
36	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	RS232, USB.	2	Chalk & Talk/PPT
	20	RS232, USB.	2	Chalk & Talk/PPT
UNIT IV: **ARM Architecture:**				
37	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	**ARM Architecture:**	2,3	Chalk & Talk/PPT
	20	ARM Processor fundamentals	3	Chalk &Talk/PPT
38	10	Revision of previous topic	1	Chalk & Talk/PPT
	20	ARM Architecture –	2	Chalk & Talk/PPT
	20	ARM Architecture –	2	Chalk &Talk/PPT
39	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	Register	2	Chalk & Talk/PPT
	20	RAM, ROM memory	2	Chalk &Talk/PPT
40	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	CPSR	2	Chalk & Talk/PPT
	20	Pipeline	2	Chalk &Talk/PPT
41	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	exceptions	2	Chalk & Talk/PPT
	20	interrupts interrupt vector table	2	Chalk &Talk/PPT
42	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	ARM instruction set	2,3	Chalk & Talk/PPT

	20	Data processing, Branch instructions	3	Chalk &Talk/PPT
43	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	load instructions	3	Chalk & Talk/PPT
	20	Store instructions	3	Chalk &Talk/PPT
44	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Software interrupt instructions	3	Chalk & Talk/PPT
	20	Software interrupt instructions	3	Chalk &Talk/PPT
45	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Program status register instructions	2	Chalk & Talk/PPT
	20	Program status register instructions	3	Chalk &Talk/PPT
46	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	loading constants	2	Chalk & Talk/PPT
	20	loading constants	3	Chalk &Talk/PPT
47	10	Revision of previous topic	0	Chalk & Talk/PPT
	20	Conditional execution	2	Chalk & Talk/PPT
	20	Conditional execution	3	Chalk &Talk/PPT
48	10	Revision of previous topic		Chalk & Talk/PPT
	20	Introduction to Thumb instructions	3	Chalk & Talk/PPT
	30	Introduction to Thumb instructions	3	Chalk &Talk/PPT
UNIT V: **Advanced ARM Processors**				
49	20	Revision of previous topic	3	Chalk & Talk/PPT
	30	**Advanced ARM Processors**	3	Chalk & Talk/PPT
50	10	Revision of previous topic	1	Chalk &Talk/PPT
	20	Introduction to CORTEX Processor	2	Chalk & Talk/PPT
	20	features	2	Chalk & Talk/PPT

51	10	Revision of previous topic	2	Chalk &Talk/PPT
	20	architecture	2	Chalk & Talk/PPT
	20	architecture	2	Chalk & Talk/PPT
52	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	OMAP Processor	2	Chalk & Talk/PPT
	20	features	2	Chalk &Talk/PPT
53	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	Architecture	2	Chalk & Talk/PPT
	20	Architecture	2	Chalk &Talk/PPT
54	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	OMAP Processor and its Architecture	2	Chalk & Talk/PPT
	20	Simple programs	2	Chalk &Talk/PPT
55	10	Revision of previous topic	2	Chalk & Talk/PPT
	20	OMAP Processor and its Architecture	3	Chalk & Talk/PPT
	20	Simple programs	2	Chalk &Talk/PPT
56	10	**Test I**	2	Chalk & Talk/PPT
	20	**Test II**	2	Chalk & Talk/PPT
	20	**Tutorial Class UNIT I**	2	Chalk &Talk/PPT
57	10	**Tutorial Class UNIT I**	2	Chalk & Talk/PPT
	20	**Tutorial Class UNIT I**	2	Chalk & Talk/PPT
	20	**Tutorial Class UNIT II**	2	Chalk &Talk/PPT
58	10	**Tutorial Class UNIT II**	2	Chalk & Talk/PPT
	20	**Tutorial Class UNIT II**	2	Chalk & Talk/PPT
	20	**Tutorial Class UNIT III**	2	Chalk &Talk/PPT
59	50	**Tutorial Class UNIT III**	4	Chalk & Talk/PPT

60	50	**Tutorial Class UNIT III**	4	Chalk & Talk/PPT
61	50	**Tutorial Class UNIT IV**	4	Chalk &Talk/PPT
62	50	**Tutorial Class UNIT IV**	4	Chalk & Talk/PPT
63	50	**Tutorial Class UNIT IV**	4	Chalk & Talk/PPT
64	50	**Tutorial Class UNIT V**	4	Chalk & Talk/PPT
65	50	**Tutorial Class UNIT V**	4	Chalk &Talk/PPT
66	50	**Tutorial Class UNIT V**	4	Chalk & Talk/PPT
67	50	**Tutorial Class UNIT V**	4	Chalk & Talk/PPT
68	50	**Remedial Classes/NPTL**	4	Chalk &Talk/PPT
69	50	**Remedial Classes/NPTL**	4	Chalk & Talk/PPT
70	50	**Remedial Classes/NPTL**	4	Chalk & Talk/PPT
71	50	**Remedial Classes/NPTL**	4	Chalk &Talk/PPT
72	50	**Tutorial Class UNIT IV**	4	Chalk & Talk/PPT
73	50	**Tutorial Class UNIT V**	4	Chalk & Talk/PPT
74	50	**Tutorial Class UNIT V**	4	Chalk &Talk/PPT
75	50	**Tutorial Class UNIT V**	4	Chalk & Talk/PPT
76	50	**Tutorial Class UNIT V**	4	Chalk & Talk/PPT
77	50	**Remedial Classes/NPTL**	1,2,3,5	Chalk &Talk/PPT
78	50	**Remedial Classes/NPTL**	1,2,3,5	Chalk & Talk/PPT
79	50	**Remedial Classes/NPTL**	1,2,3,5	Chalk & Talk/PPT
80	50	**Remedial Classes/NPTL**	1,2,3,5	Chalk &Talk/PPT

ASSIGNMENT QUESTIONS

UNIT-I

1.Write the Difference Between Microprocessor &Microcontroller**(2016-may)**

2.Draw & explain the functional diagram of 8086 Microprocessor. **(JULY-2023)**.

3. Draw & explain the pin diagram of 8086 Microprocessor. (**GNITC-May – 2019)**

4.Explain the Addressing Modes Of 8086 Microprocessor. **(JULY-2023)**

5.Explain the Instruction Set Of 8086 Microprocessor. (**GNITC-May – 2019)**

UNIT-II

1.Draw and Explain the Architecture Of 8051 Microcontroller. (**GNITC-May – 2019)**

2.Explain the Addressing Mode Of 8051 Microcontroller (**GNITC-May – 2019)**

3.Explain TMOD & TCON Registers. (**GNITC-May – 2019)**

4.Explain the Interrupt Structure Of 8051 Microcontroller**(2017-may)**

5.Draw the Pin Diagram Of 8051 Microcontroller

UNIT-III

1Explain Serial Communication Protocols **(JULY-2023)**

2.Draw the Interfacing Diagram of LCD With 8051 Microcontroller. **(R13-2016-may)**

3.Explain the Memory Organization Of 8051 Microcontroller.

4.Draw the Interfacing Diagram of Memory With 8051 Microcontroller**. (R13-2016-may)**

5.Explain ADC & DAC Interfacing with 8051 Microcontroller. (**GNITC-May – 2019)**

UNIT-IV

1.Draw and Explain ARM Processor Architecture **(JULY-2023)**.

2.Write differences between CISC & RISC processor. **(JULY-2023)**.

3.Explain the register file of ARM processor.

4.Explain ARM processor & THUMB instruction set.

5.write features of ARM processor and 3-stage pipeline architecture.

UNIT-V

1.Explain CORTEX Processor Architecture.

2.Explain OMAP Processor Architecture. **(GNITC-MAY-2019)**

3.List the Features and Applications of CORTEX Processor. **(GNITC-MAY-2019)**

4.List the Features &Applications of OMAP Processor.

Question Bank / Previous Question Papers questions

Question Bank with Blooms Taxonomy Level (BTL)

Subject Name with code: MC & A(21ES0EC30) Class: IOT III Yr-II Sem
Name of the Faculty Member : R. SANDEEP REDDY Academic Year: 2023-24(I sem)

Blooms Taxonomy Levels (BTL)

1. Remembering
2. Understanding
3. Applying
4. Analyzing
5. Evaluating
6. Creating

SI.No	Questions	Marks	BTL level	Course Outcome
	Unit - 1 **Part – A (2 Marks)**			
1	List different types of 8086 hardware interrupts. (R13-2016-oct/nov)	2	1	Co1
2	List out different segmentations presented in 8086 microprocessors. (R13-2016-may)	2	1	Co1
3	Draw the flag register of 8086 microprocessor and explain the function of each flag. (R13-2016-may) (**GNITC- May – 2019**)	2	1	Co1
4	Name the fourteen-register used in 8086 microprocessors. (R13-2017-may)	2	1	Co1
5.	List the advantages of memory segmentation. (oct-2016)	2	1	
6	List different addressing modes of 8086. **(JULY-2023)**	2	1	Co1
7	What is the use of MN/MX signals in 8086. **(JULY-2023)**	2	1	
8	What are instruction formats? (may-2017)	2	1	Co1
9	List the data transfer instruction set of 8086 microprocessor (**GNITC-May – 2019)**	2	1	Co1

10	List the logical instruction set of 8086 microprocessors. (R13-2018-April)	2	1	Co1
11	Write a program to find the factorial of four using 8086 microprocessors. (R13-2017-may)	2	1	Co1
12	What is the data and address bus size in 8086? (**GNITC- May – 2019)**	2	1	Co1
13	Explain memory organization of 8086? (**GNITC- May – 2019)**	2	2	Co1
14	What is offset & physical address? Explain with an example **(GNITC May – 2019)**	2	1	
	Unit - 1 **Part – B (5 Marks)**			
1	Explain the internal hardware architecture of 8086 microprocessor with neat diagram. (R13-2016-oct/nov) (**GNITC-May – 2019) (JULY-2023)**	5	2	Co1
2	Explain instruction set of 8086. (R13-2016-oct/nov) (**GNITC-May – 2019)**	5	2	Co1
3	Explain segmentation. Discuss the physical address formation in 8086. (R13-2016-oct/nov) (**GNITC-May – 2019)**	5	2	Co1
4	Define queue and explain the need for queue in 8086 microprocessors with respect to pipelining. (R09-2015-nov)	5	2	Co1
5	Draw the register organization of 8086 microprocessor and explain it. (R13-2016-may) **(JULY-2023)**	5	2	Co1
6	Explain the concept of physical address calculation of 8086 microprocessor. (R13-2016-may)	5	2	Co1
7	Explain the pin Architecture 8086 microprocessor with a neat sketch. (R13-2017-may) (**GNITC-May – 2019)**	5	2	Co1
8	Explain the signal description of 8086 microprocessor. (R13-2017-	5	2	Co1

	may)			
9	What is an interrupt? Explain the various types of interrupts in 8086 microprocessors. (R13-2017-may) (**GNITC- May – 2019)**	5	2	Co1
10	Explain 8086 string manipulation instructions. (R09-2015-may) (**GNITC-May – 2019)**	10	2	Co1
11	Explain the minimum mode pins of 8086 microprocessor in detail. **(JULY-2023)**	5	2	Co1
Unit - 2 Part – A (2 Marks)				
1	What is the difference between microprocessor and micro controller? (2016-oct/nov)	2	1	Co2
2	List out the addressing modes of 8051 microcontroller. (2016-oct/nov) (**GNITC-May – 2019)**	2	1	Co2
3	Explain the register set of 8051 microcontrollers. (2016-may) (**GNITC-May – 2019)**	2	2	Co2
4	List out the difference between microprocessor and microcontroller (2016-may)	2	1	Co2
5	Write TCON special function register used in 8051 microcontrollers. (2017-may) (**GNITC-May – 2019)**	2	1	Co2
6	Explain PUSH & POP instructions in 8051(oct-2016 & April-2018)	2	1	Co2
7	Explain the 8051instructions i) DJNZ ii) CJNE iii) RLC(April-2018)	2	2	Co1
8	what is the importance of jump instructions in ALP for 8051(april-2018)	2	1	Co2
9	List different instruction set groups of 8051(may-2016)	2	3	Co2
10	Define baud rate of 8051. (2016-oct/nov)	2	2	Co2
11	Mention the interrupt priority in 8051. (2016-oct/nov)	2	4	Co2

12	Draw the T0 and T1 registers of 8051 microcontrollers. (2016-may)	2	4	Co2
13	Explain the hardware interrupts of 8051 microcontroller with examples. (2016-may)	2	3	Co2
14	What are the different types of interrupts are used in 8051 microcontrollers. (2017-may)	2	3	Co2
15	Draw the timer/counter control logic diagram in 8051 microcontrollers. (2017-may)	2	1	Co2
16	how does affect of the SBUF SFR in serial communications of 8051? (April-2018)	2	2	Co2
17	Draw The IE And IP Registers Of 8051 Microcontroller (**GNITC-May – 2019)**	2	1	Co2
18	Draw the bit format of PSW register in 8051**(JULY-2023)**	2	1	Co2
19	Explain rotate and Swap instructions of 8051 microcontroller **(JULY-2023)**	2	2	Co2
	Unit - 2 **Part – B(5Marks)**			
1	Explain 8051 Architecture. (**GNITC-May – 2019)**	5	2	Co2
2	Explain 8051 Instruction set **(JULY-2023)**	5	2	Co2
3	Explain 8051 Timer/counter Operations	5	2	Co2
4	Explain 8051 serial communication	5	2	Co2
5	Explain interrupt structure of 8051	5	2	Co2
6	Explain the register organization of 8051(**GNITC-May – 2019)**	5	2	Co2
7	Draw the SCON & PCON register frames format of 8051 microcontroller and explain (**GNITC-May – 2019)**	5	2	Co2
8	Draw the IE and IP Registers Of 8051 Microcontroller (**GNITC-May – 2019)**	5	2	Co2
9	Interface external 8 K memory to 8051 microcontrollers. Draw the necessary diagram (**GNITC-May – 2019)**	5	2	Co2

10	Explain TCON, TMOD registers of 8051 microcontrollers.	5	2	Co2
Unit - 3 Part – A (2 Marks)				
1	Write the advantage and disadvantage of parallel communication over serial communication. (R13-2016-oct/nov) (**GNITC-May – 2019)**	2	2	Co3
2	List out the important features of the A/D converter. (R13-2016-oct/nov)	2	1	Co3
3	Explain serial data transfer scheme. (R13-2016-may)	2	4	Co3
4	Write short notes on I2C BUS. (R13-2016-may)	2	1	Co3
5	Write short notes on DAC. (R13-2017-may) (**GNITC-May – 2019)**	2	3	Co3
6	Write short notes on DAC. (R13-2017-may) (**GNITC-May – 2019)**	2	1	Co3
7	How does 8051 differences between the internal and external program memory **(JULY-2023)**	2	1	Co3
8	Write short notes on matrix keyboard interface of 8051**(JULY-2023)**	2	1	Co3
Unit – 3 Part – B (5 Marks)				
1	Explain I2C bus configuration (R13-2016-oct/nov) (R13-2016-oct/nov)	5	1	Co3
	Explain how to interface (a) ADC and (b) DAC to 8051. (R13-2016-oct/nov)	5	2	Co3
2	Explain how to interface LCD to 8051. (R13-2016-may)	5	2	Co3
3	Draw the interacting diagram of A/D convertor with 8051 and explain its operation. (R13-2016-may) (**GNITC-May – 2019)**	5	1	Co3
4	Explain the concept of keyboard and interfacing along with block diagram. (R13-2016-may) (**GNITC-May – 2019) (JULY-2023)**	5	**2**	Co3
5	Explain how to interface RAM/ROM to 8051 microcontrollers (R13-2016-may)	5	2	Co3
6	Describe the interfacing of D/A converter with a neat sketch. (R13-	5	2	Co3

	2017-may) (**GNITC-May – 2019)**			
7	Explain SPI bus configuration (R13-2017-may)	5	2	Co3
8	Explain RS 232C data cable (GNITC-May – 2019)	5	2	Co3
9	Write short notes on i) USB ii) UART (GNITC-May – 2019)	5	1	Co3
10	Explain the concept of methods of serial communication with examples. **(JULY-2023)**	5	2	
Unit – 4 Part – A (2 Marks)				
1	Difference between RISC and CISC processor **(JULY-2023)**.	2	1	Co4
2	List various advanced features of ARM processor.	2	1	Co4
3	List and explain various operating modes of ARM processor.	2	1	Co4
4	Define Interrupt vector table. **(JULY-2023)**	2	2	Co4
5	Give list of interrupt vector table.	2	2	Co4
6	Explain in short Instruction set of ARM processor	2	2	Co4
7	Define and Explain ARM assembly language program.	2	2	Co4
8	Give list of arithmetic instruction of ARM.	2	1	Co4
9	Draw the CPSR and flags (GNITC-MAY-2019)	2	2	Co4
Unit – 4 Part –B (5 Marks)				
1	Draw & explain ARM Architecture.	5	2	Co4
2	Explain ARM instruction set.	5	2	Co4
3	Explain exceptions & interrupt vector table	5	2	Co4
4	Explain Thumb instructions (GNITC-MAY-2019)	5	2	Co4
5	Explain about ARM 7 processor with neat Block Diagram (GNITC-MAY-2019	5	2	Co4
6	Explain about program status register in ARM Processor. (GNITC-MAY-2019)	5	2	Co4
7	Give distinguish features of ARM Processor **(JULY-2023)**	5	2	Co4
Unit – 5 Part –A(2 Marks)				
1	List and give details of different profiles of ARM cortex	2	1	Co5
2	Write short notes on cortex processor	2	1	Co5
3	Write about OMAP processor	2	2	Co5
4	Explain software instructions & program status register instruction	2	2	Co5
5	Explain how the constants are loaded in immediate mode in ARM	2	2	Co5
6	Explain about ARM addressing Modes	2	2	Co5

7	Write the applications of OMAP processor? (GNITC-MAY-2019)	2	1	Co5
8	What is wakeup interrupt controller? (GNITC-MAY-2019) **(JULY 2023)**	2	1	Co5
9	List the features of OMAP processor? (GNITC-MAY-2019) **(JULY-2023)**	2	2	Co5
10	Explain the Block diagram of OMAP processor. (GNITC-MAY-2019)			
Unit – 5 Part –B (5 Marks)				
1	Give the distinguishing features of ARM Cortex M3 and explain. **(JULY-2023)**	5	1	Co5
2	Explain CORTEX processor Architecture	5	3	Co5
3	Explain OMAP processor Architecture	5	3	Co5
4	What are the applications of cortex processor? (GNITC-MAY-2019)	5	4	Co5
5	What are major address ranges in cortex processor? Explain the block diagram of cortex processor. (GNITC-MAY-2019)	5	4	Co5
6	Describe the evolution and main trends of the microcontroller market until the appearance of ARM Cortex core micro controllers. What were the main microcontroller families and what new features they had?	5	4	Co5

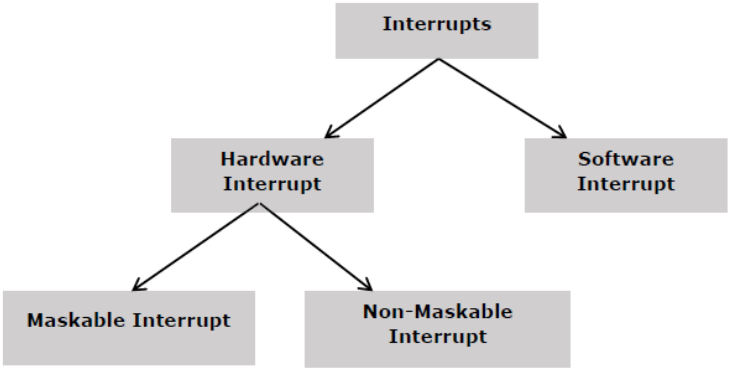
UNIT-I

PART-A answers

1. List different types of 8086 hardware interrupts. (R13-2016-oct/nov &April-2018)

Ans: Interrupt is the method of creating a temporary halt during program execution and allows peripheral devices to access the microprocessor. The microprocessor responds to that interrupt with an ISR (Interrupt Service Routine), which is a short program to instruct the microprocessor on how to handle the interrupt.

The following image shows the types of interrupts we have in a 8086 microprocessor −



Hardware Interrupts:

Hardware interrupt is caused by any peripheral device by sending a signal through a specified pin to the microprocessor**.**The 8086 has two hardware interrupt pins, i.e. NMI and INTR. NMI is a non-maskable interrupt and INTR is a maskable interrupt having lower priority. One more interrupt pin associated is INTA called interrupt acknowledge.

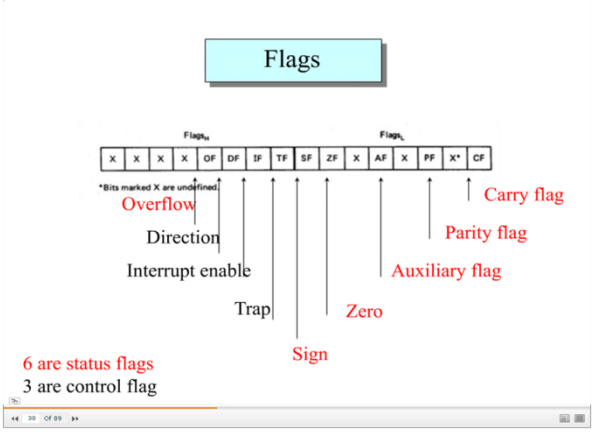
2. List out different segmentations presented in 8086 microprocessors. (R13-2016-may)

Ans: In 80x86 processors, unlike the 8085, has the memory divided into various sections called as segments. (Note that the following will be valid in 80286 and above for Real mode memory addressing only.)

1. The first is the code segment where you store the program.
2. Second is data segment where the data is stored.
3. Third is extra segment which is mostly used for string operations.
4. Last one is the stack segment which is used to push/pop (save and retrieve) your data or used to store addresses for RET when CALL is executed.

3. Draw the flag register of 8086 microprocessor and explain the function of each flag. (R13-2016-may) (GNITC- May – 2019)

Ans: Flag Register



It is a 16-bit register that behaves like a flip-flop, i.e. it changes its status according to the result stored in the accumulator. It has 9 flags and they are divided into 2 groups − Conditional Flags and Control Flags.

Conditional Flags:

It represents the result of the last arithmetic or logical instruction executed. Following is the list of conditional flags −

- Carry flag − This flag indicates an overflow condition for arithmetic operations.
- Auxiliary flag − When an operation is performed at ALU, it results in a carry/barrow from lower nibble (i.e. D0 – D3) to upper nibble (i.e. D4 – D7), then this flag is set, i.e. carry given by D3 bit to D4 is AF flag. The processor uses this flag to perform binary to BCD conversion.
- Parity flag − This flag is used to indicate the parity of the result, i.e. when the lower order 8-bits of the result contains even number of 1's, then the Parity Flag is set. For odd number of 1's, the Parity Flag is reset.
- Zero flag − This flag is set to 1 when the result of arithmetic or logical operation is zero else it is set to 0.
- Sign flag − This flag holds the sign of the result, i.e. when the result of the operation is negative, then the sign flag is set to 1 else set to 0.
- Overflow flag − This flag represents the result when the system capacity is exceeded.

Control Flags:

Control flags controls the operations of the execution unit. Following is the list of control flags −

- Trap flag − It is used for single step control and allows the user to execute one instruction at a time for debugging. If it is set, then the program can be run in a single step mode.

- Interrupt flag − It is an interrupt enable/disable flag, i.e. used to allow/prohibit the interruption of a program. It is set to 1 for interrupt enabled condition and set to 0 for interrupt disabled condition.
- Direction flag − It is used in string operation. As the name suggests when it is set then string bytes are accessed from the higher memory address to the lower memory address and vice-a-versa.
-

4. Name the fourteen register used in 8086 microprocessor. (R13-2017-may)

Ans: Registers of 8086 can be classified as general purpose registers(GPR s) and special function registers (SFR s)..

Or in specific to 8086--

1. General registers (AX, BX, CX, DX)
2. Index and pointer registers (DI, SI, BP, SP)
3. Flag register
4. Segment registers (CS, DS, SS, and ES)

5. List the advantages of memory segmentation.(oct-2016)

Ans: Advantages of memory segmentation:

1. Segmentation provides a powerful memory management mechanism.
2. It allows programmers to partition their programs into modules that operate independently of one another.
3. Segments allow two processes to easily share data.
4. It allows to extend the address ability of a processor i.e. segmentation allows the use of 16 bit registers to give an addressing capability of 1 MB. Without segmentation, it would require 20 bit registers.
5. Segmentation makes it possible to separate the memory areas for stack, code and data.
6. It is possible to increase the memory size of code data or stack segments beyond 64 KB by allotting more than one segment for each area.

6. What is the function of stack & stack register?

Ans: A stack is a useful feature that is included in the CPU of most computers. It is an ordered set of elements, only one of which can be accessed at a time. A stack is a storage device that follows the LIFO scheme (Last In First Out) to store information, i.e. the item that is stored last is the first item to be retrieved as shown in figure 1.1.

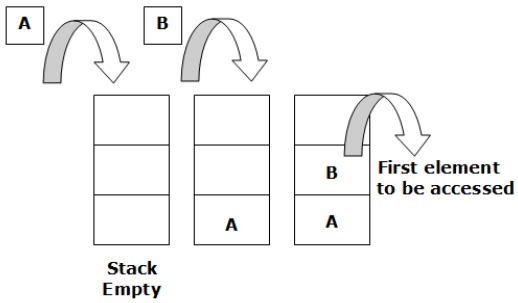


Figure 1.1: LIFO implementation of stack

Stack Pointer:

To perform any operation on the stack, the address of the top of the stack should be known. There is a special register that holds this address of stack and is called Stack Pointer Register (SP), as its value always points at the top item in the stack. The stack pointers may point to any address value starting from the origin of a stack till the limit of the stack as specified by the processor's limit register, However, the stack pointer cannot access the address beyond the origin of the stack and the (stack starting + limit) address. For example, if the starting address of stack is 1000 and its limit is 2000, then the stack pointer can point to address value starting from 1000 till (1000 + 2000) 3000.

7. What is the purpose of using macros? (R13-2017-may)

MACROS:
Macros provide several powerful mechanisms useful for the development of generic programs.
A Macro is a group of instructions with a name. When a macro is invoked, the associated set of instructions is inserted in place in to the source, replacing the macro name. This "macro expansion" is done by a Macro Preprocessor and it happens before assembly. Thus, the actual Assembler sees the "expanded" source!

Macros and Procedures:
Macros are similar to procedures in some respects, yet are quite different in many other respects.

Procedure:

- Only one copy exists in memory. Thus, memory consumed is less. "Called" when required;
- Execution time overhead is present because of the call and return instructions.

Macro:

- When a macro is "invoked", the corresponding text is "inserted" in to the source. Thus multiple copies exist in the memory leading to greater space requirements.

- However, there is no execution overhead because there are no additional call and return instructions. The code is in-place. These concepts are illustrated in the following figure:
  MACRO Definition:
  A macro has a name. The body of the macro is defined between a pair of directives, MACRO and ENDM. Two macros are defined in the example given below.

  Examples of Macro Definitions:
  Definition of a Macro named PUSHA2C
  PUSHA2C MACRO;
  PUSH AX;
  PUSH BX;
  PUSH CX;
  ENDM;

8. What are instruction formats? (may-2017)

Ans: An instruction format defines the layout of the bits of an instruction, in terms of its constituent's parts. An instruction format must include an opcode and, implicitly or explicitly, zero or more operands. Each explit operand is referenced using one of the addressing modes that is available for that machine. The format must, implicitly or explictly, indicate the addressing mode of each operand. For most instruction sets, more than one instruction format is used.

9. List the data transfer instruction set of 8086 microprocessors. (R13-2016-may)

Ans: Data Transfer Instructions

These instructions are used to transfer the data from the source operand to the destination operand. Following is the list of instructions under this group –

Instruction to transfer a word

- MOV − Used to copy the byte or word from the provided source to the provided destination.
- PPUSH − Used to put a word at the top of the stack.
- POP − Used to get a word from the top of the stack to the provided location.

- PUSHA − Used to put all the registers into the stack.
- POPA − Used to get words from the stack to all registers.
- XCHG − Used to exchange the data from two locations.
- XLAT − Used to translate a byte in AL using a table in the memory.

Instructions for input and output port transfer

- IN − Used to read a byte or word from the provided port to the accumulator.
- OUT − Used to send out a byte or word from the accumulator to the provided port.

Instructions to transfer the address

- LEA − Used to load the address of operand into the provided register.
- LDS − Used to load DS register and other provided register from the memory
- LES − Used to load ES register and other provided register from the memory.

Instructions to transfer flag registers

- LAHF − Used to load AH with the low byte of the flag register.
- SAHF − Used to store AH register to low byte of the flag register.
- PUSHF − Used to copy the flag register at the top of the stack.
- POPF − Used to copy a word at the top of the stack to the flag register.

10. List the logical instruction set of 8086 microprocessor. (R13-2018-April)

Ans: The processor instruction set provides the instructions AND, OR, XOR, TEST, and NOT Boolean logic, which tests, sets, and clears the bits according to the need of the program.

The format for these instructions −

Sr.No.	Instruction	Format
1	AND	AND operand1, operand2
2	OR	OR operand1, operand2
3	XOR	XOR operand1, operand2

4	TEST	TEST operand1, operand2
5	NOT	NOT operand1

11.Write a program to find the factorial of four using 8086 microprocessor. (R13-2017-may)

Ans:
```
DATA SEGMENT
A DB 4
DATA ENDS
CODE SEGMENT
ASSUME DS: DATA, CS: CODE
START:
MOV AX, DATA
MOV DS, AX
MOV AH, 00
MOV AL, A
L1:  DEC A
MUL A
MOV CL, A
CMP CL, 01
JNZ L1
MOV AH, 4CH
INT 21H
CODE ENDS
END START
```

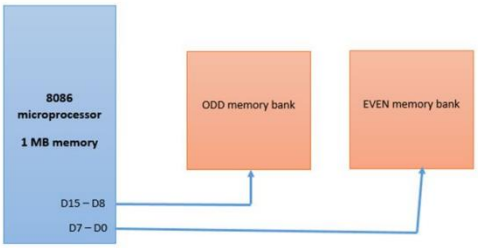
12. What is the data and address bus size in 8086? (GNITC-May – 2019)

Ans: All internal registers, as well as internal and external data buses, are 16 bits wide, which firmly established the "16-bit microprocessor" identity of the 8086. A 20-bit external address bus provides a **1 MB** physical address space

13. Explain memory organization of 8086? (GNITC- May – 2019)

Ans: There are 20 address lines in the 8086 microprocessors. This gives us 220 different memory locations. Hence the total size is 220 Bytes (as each memory location is Byte Addressable, i.e. one byte of data can be stored at every single location), which is equal to 1MB.

Even the memory is byte-addressable, yet the 8086 microprocessor an easily handle up to 16 bits of data at a time through its 16 data lines. So, to organize the memory efficiently, the entire memory in 8086 is divided into two memory banks: odd bank and the even bank.



The way in which data is read or written is decided by the value of BHE, and the last address bit, that is the A0 line. It is done in the following way:

BHE'	A0	Operation performed on memory
0	0	16 bits of data will be read or written into the memory
0	1	8 bits of data will be read/written into the odd memory bank
1	0	8 bits of data will be read/written into the even memory bank
1	1	No operation is performed

To read or write 8 bits of data, it would require only 1 CPU cycle, no matter the data is stored in any of the memory banks, but to read or write 16 bits of data, the BIU of the 8086 may require either 1 or 2 memory cycles depending upon whether the lower byte of word is located at even or odd memory address.

14. What is offset & physical address? Explain with an example (GNITC May – 2019)

Ans: The **offset address** in an 8086 is the logical **address** that the program "thinks about" when it **addresses** a location in memory. The Execution Unit (EU or CPU) is responsible for generating the **offset address**.

The 20-bit address is known as an absolute address, since it is a direct reference into the 1 MB memory space of the 8088 computers. The problem with the 8088 computer is that there are only 16-bit registers, so that something extra must be done to generate a 20-bit address. Part of the 8088 CPU is dedicated to generating 20-bit absolute addresses. The input to the address generator is two 16-bit numbers: one representing a segment and one representing an offset. The segment input will be from one of the segment registers: CS, DS, SS, ES. The other input will be from a base, index, or control register, or will be an immediate value. To generate the 20-bit address, the CPU shifts the segment 4 bits (1 hex digit) to the left and adds the offset to it.

A common combination for segment and offset is the CS and IP registers: together they indicate the address of the next instruction. As an example, suppose the CS register contains ABCDh and the IP register contains 0046h.

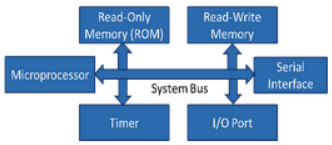
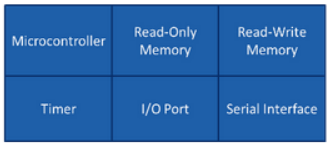
- Shift the CS register to the left by 1 hex digit: ABCD0h
- Add the IP register to the new CS value: ABCD0h + 0046h
- The absolute address is ABD16h.

UNIT-2

PART-A answers

1.What is the difference between microprocessor and micro controller?(R13-2016-oct/nov& April-2018)

Ans:

Microprocessor	Micro Controller
	
Microprocessor is heart of Computer system.	Micro Controller is a heart of embedded system.
It is just a processor. Memory and I/O components have to be connected externally	Micro controller has external processor along with internal memory and i/O components
Since memory and I/O has to be connected externally, the circuit becomes large.	Since memory and I/O are present internally, the circuit is small.
Cannot be used in compact systems and hence inefficient	Can be used in compact systems and hence it is an efficient technique
Cost of the entire system increases	Cost of the entire system is low
Due to external components, the entire power consumption is high. Hence it is not suitable to used with devices running on stored power like batteries.	Since external components are low, total power consumption is less and can be used with devices running on stored power like batteries.
Most of the microprocessors do not have power saving features.	Most of the micro controllers have power saving modes like idle mode and power saving mode. This helps to reduce power consumption even further.
Since memory and I/O components are all external, each instruction will need external operation, hence it is relatively slower.	Since components are internal, most of the operations are internal instruction, hence speed is fast.
Microprocessor have less number of registers, hence more operations are memory based.	Micro controller have more number of registers, hence the programs are easier to write.
Microprocessors are based on von Neumann model/architecture where program and data are stored in same memory module	Micro controllers are based on Harvard architecture where program memory and Data memory are separate
Mainly used in personal computers	Used mainly in washing machine, MP3 players

2. List out the addressing modes of 8086 microprocessor. (R13-2016-oct/nov)

Ans: The 8086 microprocessor accesses the data in different ways such as from different registers, from memory locations or from I/O ports are called its addressing modes. These addressing modes are categorized according to the accessing method. These are as follows.

1. Register Addressing Modes (Accessing data from registers)
2. Immediate Addressing Modes (Accessing immediate data and storing in the register as an operand)
3. Memory Addressing Modes (Accessing data from memory)
4. Direct Addressing Modes (Accessing direct data from I/O port)

Again some instruction are classified according to their behavior or condition, these are as follows.

5. Relative addressing modes (Related with some condition)
6. Implied or Implicit addressing mode (No operands)

3.Explain the register set of 8051 microcontroller.(R13-2016-may)

Ans: The 8051 microcontroller contains mainly two types of registers:

- General purpose registers (Byte addressable registers)
- Special function registers (Bit addressable registers)
- The 8051 consists of 256 bytes of RAM memory, which is divided into two ways, such as 128 bytes for general purpose and 128 bytes for special function registers (SFR) memory. The memory which is used for general purpose is called as RAM memory, and the memory used for SFR contains all the peripheral related registers like Accumulator, 'B' register, Timers or Counters, and interrupt related registers.

General Purpose Registers

General Purpose Memory :

The general purpose memory is called as the RAM memory of the 8051 microcontroller, which is divided into 3 areas such as banks, bit-addressable area, and scratch-pad area. The banks contain different general purpose registers such as R0-R7, and all such registers are byte-addressable registers that store or remove only 1-byte of data.

Banks and Registers

The B0, B1, B2, and B3 stand for banks and each bank contains eight general purpose registers ranging from 'R0' to 'R7'. All these registers are byte-addressable registers. Data transfer between general purpose registers to general purpose registers is not possible. These banks are selected by the Program Status Word (PSW) register.

PSW (Program Status Word) Register

The PSW register is a bit and byte-addressable register. This register reflects the status of the operation that is carried out in the controller. The PSW register determines bank selection by a RS1 and RS0, as shown below. The physical address of the PSW starts from D0h and the individual bits are accessed with D0h to D7h.

4. List out the difference between microprocessor and microcontroller. (R13-2016-may)

Same as 1st answer

5. Write about PSW used in 8051 microcontrollers. (R13-2017-may)

Ans: PSW (program status word) register:

The program status word (PSW) register is an 8-bit register. It is also referred to as the *flag register.* Although the PSW register is 8 bits wide, only *6* bits of it are used by the 8051. The two unused bits are user-definable flags. Four of the flags are called *conditional flags,* meaning that they indicate some conditions that result after an instruction is executed. These four are CY (carry), AC (auxiliary carry), P (parity), and OV (overflow).

the bits PSW.3 and PSW.4 are designated as RSO and RSI, respectively, and are used to change the bank registers. They are explained in the next section. The PSW.5 and PSW.l bits are general-purpose status flag bits and can be used by the programmer for any purpose. In other words, they are user definable. See Figure 2-4 for the bits of the PSW register.

CY	AC	F0	RS1	RS0	OV	–	P

CY	PSW.7	Carry flag.
AC	PSW.6	Auxiliary carry flag.
F0	PSW.5	Available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1.
RS0	PSW.3	Register Bank selector bit 0.
OV	PSW.2	Overflow flag.
--	PSW.1	User-definable bit.
P	PSW.0	Parity flag. Set/cleared by hardware each instuction cycle to indicate an odd/even number of 1 bits in the accumulator.

RS1	RS0	Register Bank	Address
0	0	0	00H - 07H
0	1	1	08H - 0FH
1	0	2	10H - 17H
1	1	3	18H - 1FH

6. Write TCON special function register used in 8051 microcontroller.(R13-2017-may)

Ans: TCON is an 8-bit register. Its bits are used for generating interrupts internal or external. The most important bits of the timer TR and TF are also in it. TR (timer run) and TF (timer overflow) bits which we use in almost all over timer applications are in it.

Microcontroller TCON register(Bit addressable)

TCON – Timer/Counter Control Register

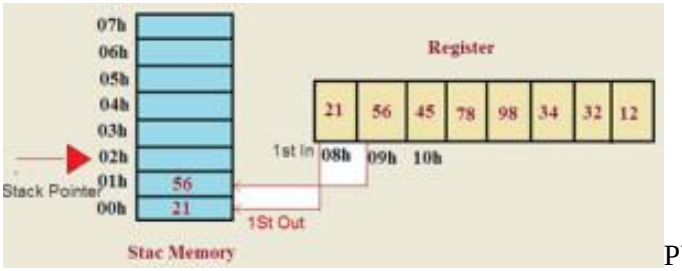
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

• TF1-TCON.7-Timer1 overflow flag
• TR1-TCON.6-Timer1 run control bit
• TF0-TCON.5-Timer0 overflow flag
• TR0-TCON.4-Timer0 run control bit
• IE1-TCON.3-External interrupt 1 edge flag
• IT1-TCON.2-Interrupt 1 type control bit
• IE0-TCON.1-External interrupt 0 edge flag
• IT0-TCON.0-Interrupt 0 type control bit

7. Explain PUSH & POP instructions in 8051(oct-2016 & April-2018)

Ans: PUSH operation

The 'PUSH' is used for taking the values from any register and storing in the starting address of the stack pointer, i.e., 00h by using 'PUSH' operation. And, for the next 'PUSH', it increments +1, and stores the value in the next address of the stack pointer, i.e., 01h.



PUSH operation of Stack

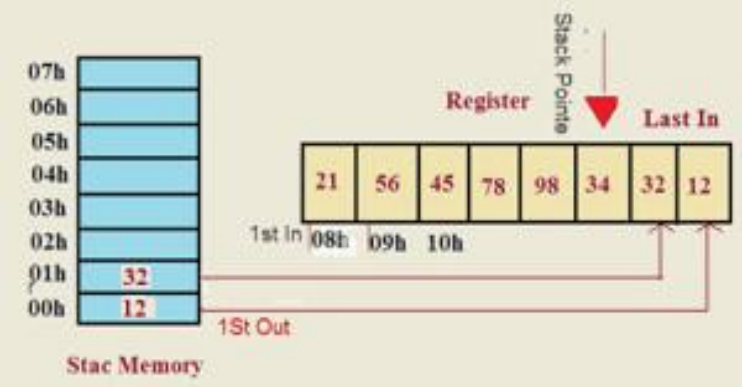
PUSH operation means (First in First out)

Example: WAP in assembly language for PUSH operation

```
0000h
MOV 08h, #21h
MOV 09h, #56h
PUSH 00h
PUSH 01h
END
```

POP Operation:

It is used for placing the values from the stack pointer's maximum address to any other register's address. If we use this 'POP' again, then it decrements by 1, and the value stored in any register is given as 'POP'.



POP Operation in Stack

8. explain the 8051instructions i) DJNZ ii) CJNE iii) RLC(April-2018)

Ans: DJNZ: The DJNZ instruction decrements the byte indicated by the first operand and, if the resulting value is not zero, branches to the address specified in the second operand.

CJNE: The CJNE instruction compares the first two operands and branches to the specified destination if their values are not equal. If the values are the same, execution continues with the next instruction.

RLC: The RLC instruction rotates the eight bits in the accumulator and the one bit in the carry flag left one bit position. Bit 7 of the accumulator is rotated into the carry flag while the original value of the carry flag is rotated into bit 0 of the accumulator. Bit 0 of the accumulator is rotated into bit 1, bit 1 into bit 2, and so on. No other flags are affected by this operation.

9. List different instruction set groups of 8051(may-2016)

Ans: Based on the operation they perform, all the instructions in the 8051 Microcontroller Instruction Set are divided into five groups. They are:

1.Data Transfer Instructions

2.Arithmetic Instructions

3.Logical Instructions

4.Boolean or Bit Manipulation Instructions

5.Program Branching Instructions

10. Define baud rate of 8051. (R13-2016-oct/nov)

Ans: Baud rate in 8051:

The 8051 transfers and receives data serially at many different baud rates. The baud rate in 8051 is completely programmable. This is done with help of timer 1.

8051 divides the crystal frequency by 12 to get machine cycle frequency. In case of XTAL = 11.0592 Mhz. so machine cycle here becomes 921.6 Khz. Now the 8051 UART circuitry divides the machine cycle frequency of 921.6 Khz by 32 once more before it is used by timer 1 to set the baud rate.

So 921.6 KHz divided by 32 gives 28,800 hz. This is the value of frequency upon which we will perform operation to get variable baud rate. When timer 1 is used to set baud rate it must be programmed in mode 2 8 bit auto reload.

Timer 1 TH1 register values for various baud rates

Baud rate	TH1(decimal)	TH1(hex)
9600	-3	FD
4800	-6	FA
2400	-12	F4
1200	-24	E8

As 28,800/3 = 9600 where -3 is loaded into TH1.

28800/12 = 2400 where -12 is loaded into TH1.

28800/24 = 1200 where -24 = E8 is loaded into TH1.

11. Mention the interrupt priority in 8051. (R13-2016-oct/nov)

Ans: IP (Interrupt Priority) Register

We can change the priority levels of the interrupts by changing the corresponding bit in the Interrupt Priority (IP) register as shown in the following figure.

A low priority interrupt can only be interrupted by the high priority interrupt, but not interrupted by another low priority interrupt.

If two interrupts of different priority levels are received simultaneously, the request of higher priority level is served.

If the requests of the same priority levels are received simultaneously, then the internal polling sequence determines which request is to be serviced.

-	-	PT2	PS	PT1	PX1	PT0	PX0
bit7	bit6	bit5	bit4	bit3	bit2	bit1	

-	IP.6	Reserved for future use.
-	IP.5	Reserved for future use.
PS	IP.4	It defines the serial port interrupt priority level.
PT1	IP.3	It defines the timer interrupt of 1 priority.
PX1	IP.2	It defines the external interrupt priority level.
PT0	IP.1	It defines the timer0 interrupt priority level.
PX0	IP.0	It defines the external interrupt of 0 priority level.

12. Draw the T0 and T1 registers of 8051 microcontroller. (R13-2016-may)

Ans: TMOD register :

As we know there are 2 timer registers in 8051. Timer 0 and timer 1. Both of these registers use the same register called TMOD to set various timer operation modes.

TMOD is an 8 bit register, in which lower 4 bits are for Timer 0 and upper 4 bits are for Timer 1.

See table below. MSB ---- LSB

GATE	C/T	M1	M0	GATE	C/T	M1	M0
TIMER 1				TIMER 0			

GATE	Gating control when set. The timer/counter is enabled only while the INTx pin is high and TRx control pin is set. When cleared, the timer is enabled whenever TRx control pin is set.
C/T	Timer or counter; 0 or clear for timer operation.(connected to input from internal system clock). 1 or set for counter operation(connected to input from Tx input pin).
M1	Mode bit 1
M0	Mode bit 0

M0 and M1 select the timer mode in TMOD. 4 modes as mode 0, mode 1, mode 2, mode 3. See table.

M1	M0	MODE	OPERATING MODE
0	0	MODE 0	13 bit timer mode 8-bit timer/counter THx with TLx as 5 bit prescaler
0	1	MODE 1	16 bit timer mode. 16 bit timer/counter THx and TLx are cascaded with no prescaler.
1	0	MODE 2	8 bit auto reload. 8 bit auto reload timer/counter THx holds a value that's to be reloaded in TLx each time it overflows.
1	1	MODE 3	Split timer mode

C/T (clock/timer) in TMOD:

This bit in TMOD register is used to know whether it is used as a delay generator or as an event counter.

C/T = 0, then it is used as a timer for time delay generation. The clock source for the time delay is the crystal frequency of 8051. Timer gets pulses from the crystal.

C/T = 1, then it is used as a counter and gets its pulses from outside the 8051. That is from pins T0 and T1 belonging to port 3. In case of timer 0, when C/T = 1 pin 3.4 provides the clock pulse and counter counts up for each clock pulse coming from that pin. Similarly for timer 1, when C/T = 1 pin 3.5 provides the clock pulse and counter counts up for each clock pulse coming from that pin.

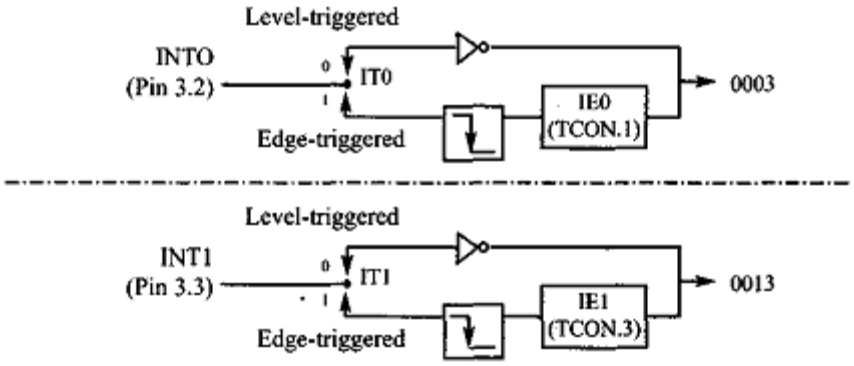
13. Explain the hardware interrupts of 8051 microcontroller with examples. (R13-2016-may)

Ans: The 8051 has two external hardware interrupts. Piri 12 (P3.2) and pin 13 (P3.3) of the 8051, designated as INTO and INT1, are used as external hardware interrupts. Upon activation of these pins, the 8051 gets interrupted in whatever it is doing and jumps to the vector table to perform the interrupt service routine

PROGRAMMING EXTERNAL HARDWARE INTERRUPTS:

The 8051 has two external hardware interrupts. Piri 12 (P3.2) and pin 13 (P3.3) of the 8051, designated as INTO and INT1, are used as external hardware interrupts. Upon activation of these pins, the 8051 gets interrupted in whatever it is doing and jumps to the vector table to perform the interrupt service

routine. In this section we study these two external hardware interrupts of the 8051 with some examples.



Activation of INTO and INT1

External interrupts INTO and INT1:

There are only two external hardware interrupts in the 8051: INTO and INT1. They are located on pins P3.2 and P3.3 of port 3, respectively. The interrupt vector table locations 0003H and 0013H are set aside for INTO and INT1, respectively. As mentioned in Section 11.1, they are enabled and disabled using the IE register. How are they activated? There are two types of activation for the external hardware interrupts: (1) level triggered, and (2) edge triggered. Let's look at each one. First, we see how the level-triggered interrupt works.

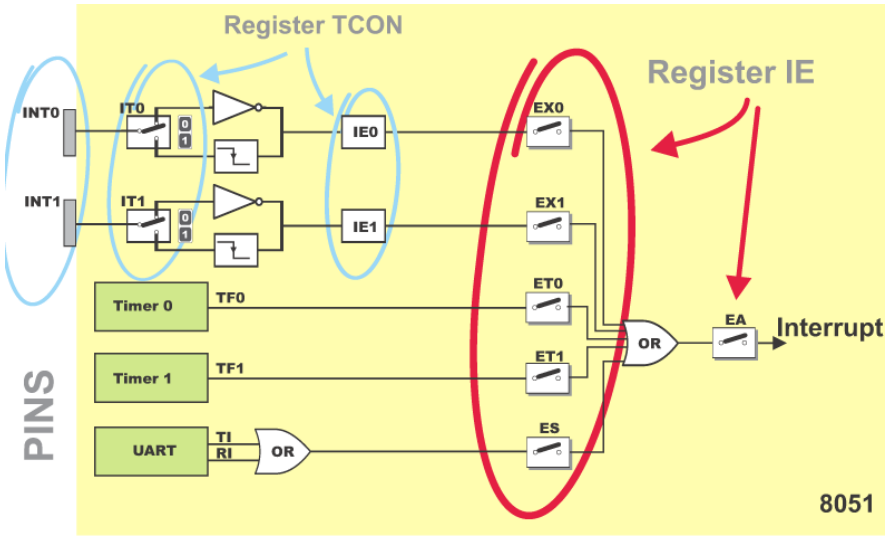
Level-triggered interrupt:

In the level-triggered mode, INTO and INT1 pins are normally high (just like all I/O port pins) and if a low-level signal is applied to them, it triggers the interrupt. Then the microcontroller stops whatever it is doing and jumps to the interrupt vector table to service that interrupt. This is called a *level-triggered* or *level-activated interrupt* and is the default mode upon reset of the 8051. The low-level signal at the INT pin must be removed before the execution of the last instruction of the interrupt service routine, RETI; otherwise, another interrupt will be generated. In other words, if the low-level interrupt signal is not removed before the ISR is finished it is interpreted as another interrupt and the 8051 jumps to the vector table to execute the ISR again.

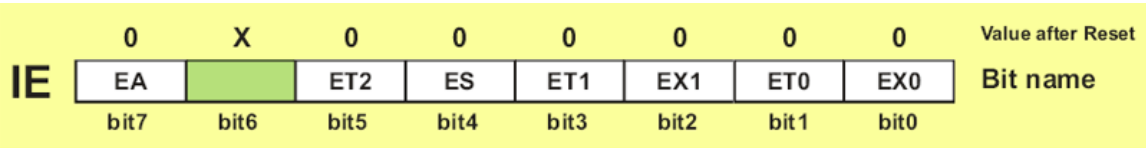
14. What are the different types of interrupts are used in 8051 microcontrollers. (R13-2017-may)

Ans: There are five interrupt sources for the 8051, which means that they can recognize 5 different events that can interrupt regular program execution. Each interrupt can be enabled or disabled by setting bits of the IE register. Likewise, the whole interrupt system can be disabled by clearing the EA bit of the same register. Refer to figure below.

Now, it is necessary to explain a few details referring to external interrupts- INT0 and INT1. If the IT0 and IT1 bits of the TCON register are set, an interrupt will be generated on high to low transition, i.e. on the falling pulse edge (only in that moment). If these bits are cleared, an interrupt will be continuously executed as far as the pins are held low.



IE Register (Interrupt Enable) :



- EA – global interrupt enable/disable:
  - 0 – disables all interrupt requests.
  - 1 – enables all individual interrupt requests.
- ES – enables or disables serial interrupt:
  - 0 – UART system cannot generate an interrupt.
  - 1 – UART system enables an interrupt.
- ET1 – bit enables or disables Timer 1 interrupt:
  - 0 – Timer 1 cannot generate an interrupt.
  - 1 – Timer 1 enables an interrupt.
- EX1 – bit enables or disables external 1 interrupt:
  - 0 – change of the pin INT0 logic state cannot generate an interrupt.
  - 1 – Enables an external interrupt on the pin INT0 state change.
- ET0 – bit enables or disables timer 0 interrupt:
  - 0 – Timer 0 cannot generate an interrupt.
  - 1 – Enables timer 0 interrupt.
- EX0 – bit enables or disables external 0 interrupt:
  - 0 – change of the INT1 pin logic state cannot generate an interrupt.

- 1 – Enables an external interrupt on the pin INT1 state change.

15. Draw the timer/counter control logic diagram in 8051 microcontroller. (R13-2017-may)

Ans: Timers / Counters

8051 has two 16-bit programmable UP timers/counters. They can be configured to operate either as timers or as event counters. The names of the two counters are T0 and T1 respectively. The timer content is available in four 8-bit special function registers, viz, TL0,TH0,TL1 and TH1 respectively.

In the "timer" function mode, the counter is incremented in every machine cycle. Thus, one can think of it as counting machine cycles. Hence the clock rate is 1/12 th of the oscillator frequency.

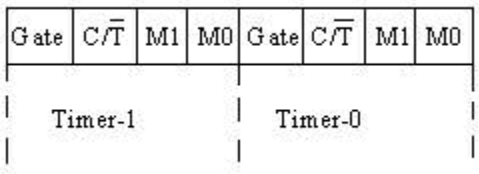
In the "counter" function mode, the register is incremented in response to a 1 to 0 transition at its corresponding external input pin (T0 or T1). It requires 2 machine cycles to detect a high to low transition. Hence maximum count rate is 1/24 th of oscillator frequency.

The operation of the timers/counters is controlled by two special function registers, TMOD and TCON respectively.

Timer Mode control (TMOD) Special Function Register:

TMOD register is not bit addressable.

TMOD
Address: 89 H



Various bits of TMOD are described as follows -

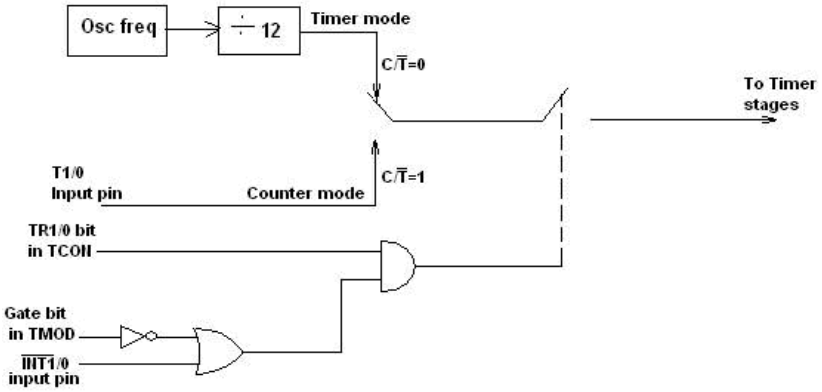
Gate: This is an OR Gate enabled bit which controls the effect of $\overline{INT1/0}$ on START/STOP of Timer. It is set to one ('1') by the program to enable the interrupt to start/stop the timer. If TR1/0 in TCON is set and signal on $\overline{INT1/0}$ pin is high then the timer starts counting using either internal clock (timer mode) or external pulses (counter mode).

$C/\overline{T}$: It is used for the selection of Counter/Timer mode.
Mode Select Bits:

M1	M0	Mode
0	0	Mode 0
0	1	Mode 1
1	0	Mode 2
1	1	Mode 3

M1 and M0 are mode select bits.

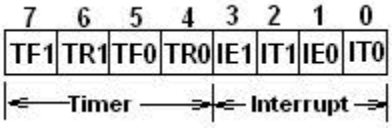
Timer/ Counter control logic:



Timer/Counter Control Logic

Timer control (TCON) Special function register:

TCON is bit addressable. The address of TCON is 88H. It is partly related to Timer and partly to interrupt.



TCON Register

16. How does effect of the SBUF SFR in serial communications of 8051?(April-2018)

Ans: The serial port of 8051 is full duplex, i.e., it can transmit and receive simultaneously. The register SBUF is used to hold the data. The special function register SBUF is physically two registers. One is, write-only and is used to hold data to be transmitted out of the 8051 via TXD. The other is, read-only and holds the received data from external sources via RXD. Both mutually exclusive registers have the same address 099H

17. What is the importance of jump instructions in ALP for 8051

Ans: In the 8051 there are two unconditional jumps: LJMP (long jump) and SJMP (shortjump). Each is discussed below. LJMP is an unconditional long jump. It is a 3-byteinstruction in which the first byte is the opcode, and the second and third bytes represent the 16-bit address of the target location.

UNIT-3

PART-A Answers

1. Write the advantage and disadvantage of parallel communication over serial communication. (R13-2016-oct/nov)
Ans:

Basis for Comparison	Serial Transmission	Parallel Transmission
Meaning	Data flows in bi-direction, bit by bit	Multiple lines are used to send data i.e. 8 bits or 1 byte at a time
Cost	Economical	Expensive
Bits transferred at 1 clock pulse	1 bit	8 bits or 1 byte
Speed	Slow	Fast
Applications	Used for long distance communication. Eg, Computer to computer	Short distance. Eg, computer to printer

The main advantages of parallel transmission over serial transmission are:

it is easier to program; And data is sent faster.

Although parallel transmission can transfer data faster, it requires more transmission channels than serial transmission. This means that data bits can be out of sync, depending on transfer distance and how fast each bit loads. A simple of example of where this can be seen is with a voice over IP (VOIP) call when distortion or interference is noticeable. It can also be seen when there is skipping or interference on a video stream.

2. List out the important features of the A/D converter. (R13-2016-oct/nov & April-2018)

Ans:
An Analog to Digital Converter (ADC) is a very useful feature that converts an analog voltage on a pin to a digital number. By converting from the analog world to the digital world, we can begin to use electronics to interface to the analog world around us.

A/D Converter features:
Digital Audio:
Digital audio workstations, sound recording, pulse-code modulation
Digital signal processing:
TV tuner cards, microcontrollers, digital storage oscilloscopes
Scientific instruments:
Digital imaging systems, radar systems, temperature sensors

3. Give the serial communication standards. (R13-2017-may & oct-2016 & April-2018)

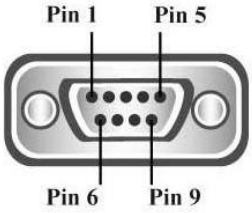
Ans:

In serial I/O, data can be transmitted as either current or voltage. When data is transmitted as voltage, the commonly used standard is known as RS-232C. This standard was developed by Electronic Industries Association (EIA), USA and adopted by IEEE. RS-232 standard proposes a maximum of 25 signals for the bus used for serial data transfer.

Serial data transmission standards including RS232, RS422, RS423, and RS485 were widely used for many data links, proving effective connectivity for the day. Although not nearly as widely used today, they can still be found in some areas.

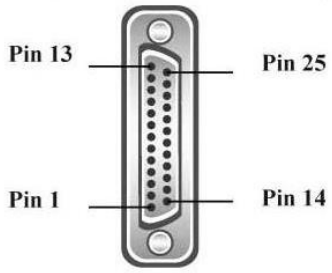
Pin 1	DCD
Pin 2	RXD
Pin 3	TXD
Pin 4	DTR
Pin 5	GND
Pin 6	DSR
Pin 7	RTS
Pin 8	CTS
Pin 9	RI

RS232 Pinout (9 Pin Male)



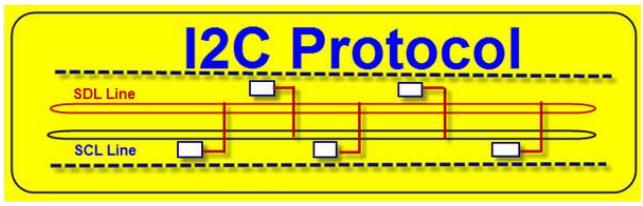
Pin 2	TXD
Pin 3	RXD
Pin 4	RTS
Pin 5	CTS
Pin 6	DSR
Pin 7	GND
Pin 8	DCD
Pin 20	DTR
Pin 22	RI

RS232 Pinout (25 Pin Male)

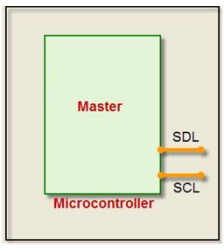


4. Write short notes on I2C BUS. (R13-2016-may)

Ans: Transmitting and receiving the information between two or more than two devices require a communication path called as a bus system. A I2C bus is a bidirectional two-wired serial bus which is used to transport the data between integrated circuits. The I2C stands for “Inter Integrated Circuit”. It was first introduced by the Philips semiconductors in 1982. The I2C bus consists of three data transfer speeds such as standard, fast-mode and high-speed-mode. The I2C bus supports 7-bit and 10-bit address space device and its operation differ with low voltages.



I2c Bus Protocol



I2C Signal Lines

The I2C is a serial bus protocol consisting of two signal lines such as SCL and SDL lines which are used to communicate with the devices. The SCL stands for a ‘serial clock line’ and this signal is

always driven by the ‘master device’. The SDL stands for the ‘serial data line’, and this signal is driven by either the master or the I2C peripherals. Both these SCL and SDL lines are in open-drain state when there is no transfer between I2C peripherals

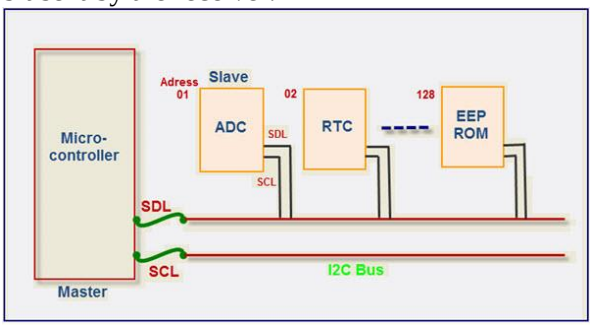
The open-drain is the concept for FET transistor wherein the drain terminal of the transistor is open state. The SDL and SCL pins of the master device are designed with the transistors in open state, so data transfer is possible only when these transistors are conducted. Hence, these lines or drain terminals are connected thorough pull-up resistors to VCC for conduction mode.

I2C Interfaces

Many slave devices are interfaced to the microcontroller with the help of the I2C bus through I2C level shifter IC for transferring the information between them. The I2C protocol used to connect a maximum of 128 devices that are all connected to communicate with the SCL and SDL lines of the master unit as well as the slave devices. It supports Multimaster communication, which means two masters are used to communicate the external devices.

I2C Data Transfer Rates

The I2C protocol operates three modes such as: fast mode, high-speed mode and standard mode wherein the standard mode data speed ranges 0Hz to 100Hz, and the fast mode data can transfer with 0Hz to 400 KHz speed and the high speed mode with 10 KHz to 100KHz. The 9-bit data is sent for each transfer wherein 8-bits are sent by the transmitter MSB to LSB, and the 9th bit is an acknowledgement bit sent by the receiver.



I2C Data Transfer Rates

I2C Communication:

The I2C bus protocol is most commonly used in master and slave communication wherein the master is called “microcontroller”, and the slave is called other devices such as ADC, EEPROM, DAC and similar devices in the embedded system. The number of slave devices is connected to the master device with the help of the I2C bus, wherein each slave consists of a unique address to communicate it. The following steps are used to communicate the master device to the slave:

Step1: First, the master device issues a start condition to inform all the slave devices so that they listen on the serial data line.

Step2: The master device sends the address of the target slave device which is compared with all the slave devices’ addresses as connected to the SCL and SDL lines. If anyone addresses matches, that device is selected, and the remaining all devices are disconnected from the SCL and SDL lines.

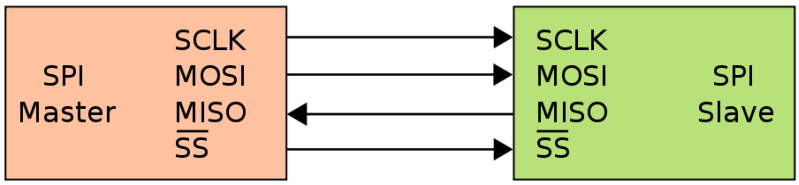
Step3: The slave device with a matched address received from the master, responds with an acknowledgement to the master thereafter communication is established between both the master and slave devices on the data bus.

Step4: Both the master and slave receive and transmit the data depending on whether the communication is read or write.

Step5: Then, the master can transmit 8-bit of data to the receiver which replies with a 1-bit acknowledgement.

5. Write short notes on SPI BUS.(R13-2017-may)
Ans:

SPI BUS:



The Serial Peripheral Interface (SPI) is a synchronous serial communication interface specification used for short distance communication, primarily in embedded systems. The interface was developed by Motorola in the mid 1980s and has become a *de facto* standard. Typical applications include Secure Digitalcards and liquid crystal displays.

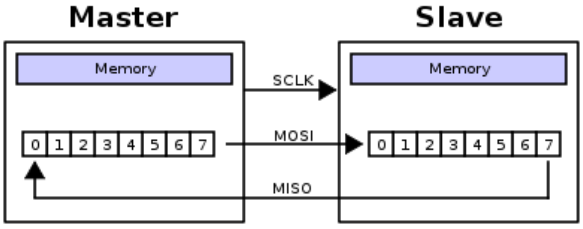
SPI devices communicate in full duplex mode using a master-slave architecture with a single master. The master device originates the frame for reading and writing. Multiple slave devices are supported through selection with individual slave select(SS) lines.

.

The SPI bus specifies four logic signals:
SCLK: Serial Clock (output from master)
MOSI: Master Output Slave Input, or Master Out Slave In (data output from master)
MISO: Master Input Slave Output, or Master In Slave Out (data output from slave)
SS: Slave Select (often active low, output from master)

Operation:

The SPI bus can operate with a single master device and with one or more slave devices.
If a single slave device is used, the SS pin *may* be fixed to logic low if the slave permits it. Some slaves require a falling edgeof the chip select signal to initiate an action. An example is the Maxim MAX1242 ADC, which starts conversion on a high→low transition. With multiple slave devices, an independent SS signal is required from the master for each slave device.
Most slave devices have tri-state outputs so their MISO signal becomes high impedance (*logically disconnected*) when the device is not selected. Devices without tri-state outputs cannot share SPI bus segments with other devices; only one such slave could talk to the master.
Data transmission



UNIT-4

PART-A ANSWERS

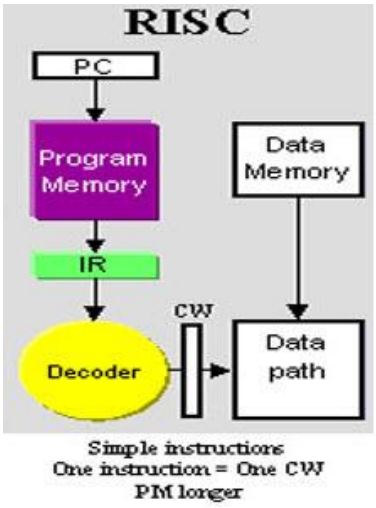
1. Difference between RISC and CISC processor.

Ans:

The architecture of the Central Processing Unit (CPU) operates the capacity to function from "Instruction Set Architecture" to where it was designed. The architectural design of the CPU is reduced instruction set computing (RISC) and Complex instruction set computing (CISC). CISC has the capacity to perform multi-step operations or addressing modes within one instruction set. It is the CPU design where one instruction works several low-level acts. For instance, memory storage, loading from memory, and an arithmetic operation. Reduced instruction set computing is a Central Processing Unit design strategy based on the vision that basic instruction set gives a great performance when combined with a microprocessor architecture which has the capacity to perform the instructions by using some microprocessor cycles per instruction. This article discusses the difference between the RISC and CISC architecture. The hardware part of the Intel is named as Complex Instruction Set Computer (CISC), and Apple hardware is Reduced Instruction Set Computer (RISC).

RISC Architecture:

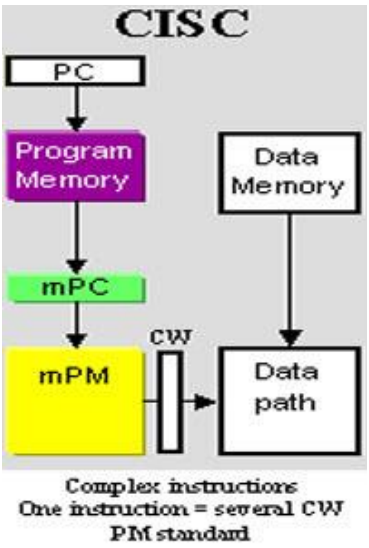
The term RISC stands for ''Reduced Instruction Set Computer''. It is a CPU design plan based on simple orders and acts fast.



RISC Architecture

CISC Architecture:

The term CISC stands for ''Complex Instruction Set Computer''. It is a CPU design plan based on single commands, which are skilled in executing multi-step operations.



CISC Architecture

2. List various advanced features of ARM processor.

Ans:

ARM is a family of instruction set architectures for computer processors based on a reduced instruction set computing (RISC) architecture developed by British company ARM Holdings. A RISC-based computer design approach means ARM processors require significantly fewer transistors than typical CISC x86 processors in most personal computers. This approach reduces costs heat and power use. These are desirable traits for light, portable, battery-powered devices including smart phones, laptops, tablet and notepad computers, and other embedded systems. A simpler design facilitates more efficient multi-core CPUs and higher core counts at lower cost, providing improved energy efficiency for servers.

ARM Holdings develops the instruction set and architecture for ARM-based products, but does not manufacture products. The company periodically releases updates to its cores. Current cores from ARM Holdings support a 32-bit address space and 32-bit arithmetic; the ARMv8-Aarchitecture, adds support for a 64-bit address space and 64-bit arithmetic. Instructions for ARM Holdings' cores have 32 bits wide fixed-length instructions, but later versions of the architecture support a variable-length instruction set that provides both 32 and 16 bits wide instructions for improved code density. Some cores can also provide hardware execution of Java byte codes

3. List and explain various operating modes of ARM processor.

Ans: The ARM7TDMI processor has seven modes of operation:

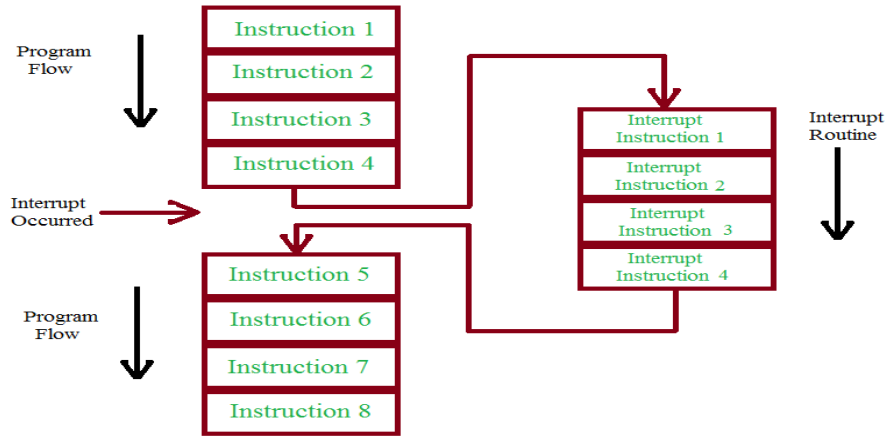
- User mode is the usual ARM program execution state, and is used for executing most application programs.
- Fast Interrupt (FIQ) mode supports a data transfer or channel process.

- Interrupt (IRQ) mode is used for general-purpose interrupt handling.
- Supervisor mode is a protected mode for the operating system.
- Abort mode is entered after a data or instruction Prefetch Abort.
- System mode is a privileged user mode for the operating system.
-

4. Define Interrupt vector table.

Ans:

The main purpose of any microcontroller is to accept input from input devices and accordingly drive the output. Hence, there will be several devices connected to a microcontroller at a time. Also, there are many internal components in a microcontroller like timers, counters etc. that require attention of the processor. Since all the devices can't obtain the attention of the processor at all times, the concept of "Interrupts" comes in to picture. An Interrupt, as the name suggests, interrupts the microcontroller from whatever it is doing and draws its attention to perform a special task. The following image depicts the procedure involved in Interrupts.



5. Give list of interrupt vector table.

Ans:

The following is the list and description of registers that are associated with Interrupts in LPC214x series MCUs. The registers mentioned here are few important of the total available VIC Registers and are also in best order to start learning about VIC.

- **Software Interrupt Register (VICSoftInt):**

  Software Interrupt Register is used to manually generate the interrupts using software i.e. code before the masking by external source. When a bit is set with 1 in the VICSoftInt register, the corresponding interrupt is triggered even without any external source

- **Software Interrupt Clear Register (VICSoftIntClear**):

  Software Interrupt Clear Register is used to clear the bits set by Software Interrupt Register. When a bit is set to 1 in this register, the corresponding bit in the Software Interrupt Register is cleared and hence releasing the forced interrupt.

- **Interrupt Enable Register (VICIntEnable**):

  Interrupt Enable Register is used to enable the interrupts that can later contribute to either FIQ or IRQ. When a bit is set to 1, the corresponding interrupt is enabled. As this is a read / write register, when this register is read, "1" indicates that the external interrupt request or software interrupts are enabled.

- **Interrupt Enable Clear Register (VICIntEnClear**):

  Interrupt Enable Clear Register is used to clear the bits set by the Interrupt Enable Clear Register i.e. it is used to disable the interrupts. When a bit is set with "1", the register allows the software to clear the corresponding bit in the Interrupt Enable Register and thus disabling the interrupt for that particular request.

- **Interrupt Select Register (VICIntSelect**):

  Interrupt Select Register is used to classify each of the 32 interrupts as either FIQ or IRQ. When a bit in this register is set to "0", then the corresponding interrupt (as shown in the above table) will be made as an IRQ. Similarly, when a bit is set to "1", the corresponding interrupt is made as FIQ.

- **IRQ Status Register (VICIRQStatus):**

  Interrupt Status Register is used to read out the status of the interrupts that enabled and declared as IRQ. Both Vectored and Non – Vectored IRQ are read out. When a bit is read as "1", then the corresponding Interrupt is enabled and defined as IRQ.

- **FIQ Status Register (VICFIQStatus**):

  This register is similar to IRQ Status Register (VICIRQStatus) except it reads the status of interrupts that are enabled and defined as FIQ.

- **Vector Control Registers (VICVectCntl0 – VICVectCntl15**):

  Vector Control Registers are used to assign slots to different interrupt sources that are classified as IRQ. There are 16 Vector Control Registers and each register controls one of the 16 Vectored IRQ slots. VICVectCntl0 (Slot 0) has the highest priority while VICVectCntl15 (Slot 15) has the least priority. The first 5 bits in the Vector Control Registers (Bit 0 – Bit 4) contains the number of the interrupt request. The 5^{th} bit (Bit 5) is used to enable the Vectored IRQ Slot. The following tables are be used to show the interrupt source and their corresponding Source Number in Decimal format.

6. Explain in short Instruction set of ARM processor

Ans: ARM provides by way of memory and registers, and the sort of instructions to manipulate them .All ARM instructions are 32 bits long. Here is a typical one:
10101011100101010010100111101011

Fortunately, we don't have to write ARM programs using such codes. Instead we use assembly language. We saw at the end of Chapter One a few typical ARM mnemonics. Usually, mnemonics are followed by one or more operands which are used to completely describe the instruction.

An example mnemonic is ADD, for 'add two registers'. This alone doesn't tell the assembler which registers to add and where to put the result. If the left and right hand side of the addition are R1 and R2 respectively, and the result is to go in R0, the operand part would be written R0,R1,R2. Thus the complete add instruction, in assembler format, would be:

ADD R0, R1, R2 ;R0 = R1 + R2

Most ARM mnemonics consist of three letters, e.g. SUB, MOV, STR, STM. Certain 'optional extras' may be added to slightly alter the affect of the instruction, leading to mnemonics such as ADCNES and SWINE. The mnemonics and operand formats for all of the ARM's instructions are described in detail in the sections below. At this stage, we don't explain how to create programs, assemble and run them. There are two main ways of assembling ARM programs - using the assembler built-in to BBC BASIC, or using a dedicated assembler. The former method is more convenient for testing short programs, the latter for developing large scale projects. Chapter Four covers the use of the BASIC assembler.

7. Define and Explain ARM assembly language program.

Ans:

Assembly language is just a thin syntax layer on top of the machine code which is composed of instructions that are encoded in binary representations (machine code), which is what our computer understands. So why don't we just write machine code instead? Well, that would be a pain in the ass. For this reason, we will write assembly, ARM assembly, which is much easier for humans to understand. Our computer can't run assembly code itself, because it needs machine code. The tool we will use to assemble the assembly code into machine code is a GNU Assembler from the GNU Binutils project named *as* which works with source files having the *.s extension. Therefore, Assembly language is the lowest level used by humans to program a computer. The operands of an instruction co

me after the mnemonic(s). Here is an example:

MOV R2, R1

8. Give list of arithmetic instruction of ARM.

Ans:
ADD – Add

- Rd := Rn + Operand2

ADC – Add with Carry

- Rd := Rn + Operand2 + Carry

SUB – Subtract

- Rd := Rn − Operand2

SBC – Subtract with Carry

- Rd := Rn − Operand2 − NOT(Carry)

RSB – Reverse Subtract

- Rd := Operand2 − Rn

RSC – Reverse Subtract with Carry

- Rd := Operand2 − Rn − NOT(Carry)

Examples of arithmetic instructions.

ADD r0, r1, r2

- R0 = R1 + R2

SUB r5, r3, #10

- R5 = R3 − 10

RSB r2, r5, #0xFF00

- R2 = 0xFF00 − R5

9. Draw the CPSR and flags (GNITC-MAY-2019)

Ans:

The Current Program Status **Register** is a 32-bit wide **register** used in the **ARM** architecture to record various pieces of information regarding the state of the program being executed by the processor and the state of the processor

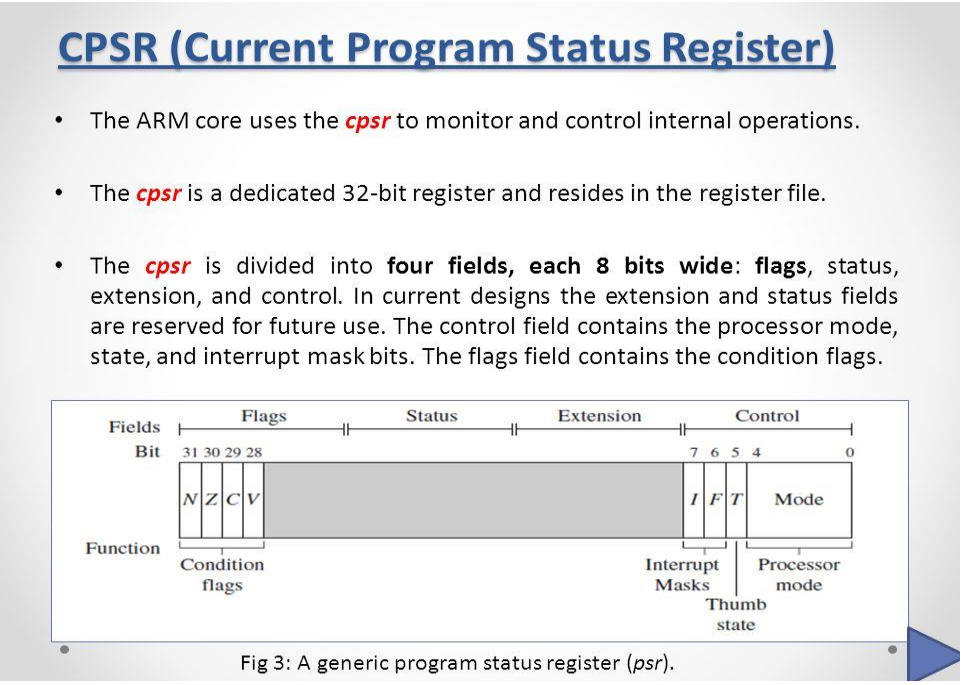


Fig 3: A generic program status register (*psr*).

UNIT-5
PART-A Answers

1. List and give details of different profiles of ARM cortex.

Ans: The ARM architecture profiles are:

1. Application profile

Application profiles implement a traditional ARM architecture with multiple modes and support a virtual memory system architecture based on an MMU. These profiles support both ARM and Thumb instruction sets.

2**. Real-time profile**

Real-time profiles implement a traditional ARM architecture with multiple modes and support a protected memory system architecture based on an MPU.

3. Microcontroller profile

Microcontroller profiles implement a programmers' model designed for fast interrupt processing, with hardware stacking of registers and support for writing interrupt handlers in high-level languages. The processor is designed for integration into an FPGA and is ideal for use in very low power applications.

2. Write short notes on cortex processor.

Ans:

The ARM Cortex-A9 MP Core is a 32-bit processor core licensed by ARM Holdings implementing the ARMv7-A architecture. It is a multicore processor providing up to 4 cache-coherent cores

Key features of the Cortex-A9 core are:

1.Out-of-order speculative issue superscalar execution 8-stage pipeline giving 2.50 DMIPS/MHz/core.

2.NEON SIMD instruction set extension performing up to 16 operations per instruction (optional).

3.High performance VFPv3 floating point unit doubling the performance of previous ARM FPUs (optional).

4.Thumb-2 instruction set encoding reduces the size of programs with little impact on performance.

5.TrustZone security extensions.

6.Jazelle DBX support for Java execution.

7Jazelle RCT for JIT compilation.

8.Program Trace Macrocell and CoreSight Design Kit for non-intrusive tracing of instruction execution.

9.L2 cache controller (0–4 MB).

10.Multi-core processing.

3. Write about OMAP processor.

Ans:

The OMAP (Open Multimedia Applications Platform) family, developed by Texas Instruments, is a series of image/video processors. They are proprietary system on chips (SoCs) for portable and mobile multimedia applications. OMAP devices generally include a general-purpose ARM architecture processor core plus one or more specialized co-processors. Earlier OMAP variants commonly featured a variant of the Texas Instruments TMS320 series digital signal processor. The platform was created after December 12, 2002, as STMicroelectronics and Texas Instruments jointly announced an initiative for Open Mobile Application Processor Interfaces (OMAPI) intended to be used with 2.5 and 3G mobile phones, that were going to be produced during 2003. (This was later merged into a larger initiative and renamed the MIPI Alliance.)

The OMAP was Texas Instruments' implementation of this standard. (The STMicroelectronics implementation was named Nomadic.) OMAP did enjoy some success in the smart phone and tablet market until 2011 when it lost ground to Qualcomm Snapdragon. On September 26, 2012, Texas Instruments announced they would wind down their operations in smart phone and tablet oriented chips and instead focus on embedded platforms. On November 14, 2012, Texas Instruments announced they would cut 1,700 jobs due to their shift from mobile to embedded platforms. The last OMAP5 chips were released in Q2 2013.

4 Explain about register indirect addressing mode in ARM.

Ans:

Register Indirect Addressing Mode :

Register indirect addressing means that the location of an operand is held in a register. It is also called indexed addressing or base addressing. Register indirect addressing mode requires three read operations to access an operand. It is very important because the content of the register containing the pointer to the operand can be modified at runtime. Therefore, the address is a variable that allows the access to the data structure like arrays.

- Read the instruction to find the pointer register
- Read the pointer register to find the operand address
- Read memory at the operand address to find the operand

Some examples of using register indirect addressing mode:

```
LDR     R2, [R0]  ; Load R2 with the word pointed by R0
```

```
        STR     R2, [R3]  ; Store the word in R2 in the location pointed by R3
```

Register Indirect Addressing with an Offset

ARM supports a memory-addressing mode where the effective address of an operand is computed by adding the content of a register and a literal offset coded into load/store instruction. For example,

```
        Instruction                 Effective Address
-------------------------------------------------------------------------------
        LDR R0, [R1, #20]  R1 + 20   ; loads R0 with the word pointed at by R1+20
-------------------------------------------------------------------------------
```

5. Explain about ARM addressing Modes

Ans:

There are different ways to specify the address of the operands for any given operations such as load, add or branch. The different ways of determining the address of the operands are called addressing modes. In this lab, we are going to explore different addressing modes of ARM processor and learn how all instructions can fit into a single word (32 bits).

Name	Alternative Name	ARM Examples
Register to register	Register direct	MOV R0, R1
Absolute	Direct	LDR R0, MEM
Literal	Immediate	MOV R0, #15 ADD R1, R2, #12
Indexed, base	Register indirect	LDR R0, [R1]
Pre-indexed, base with displacement	Register indirect with offset	LDR R0, [R1, #4]
Pre-indexed, autoindexing	Register indirect pre-incrementing	LDR R0, [R1, #4]!
Post-indexing, autoindexed	Register indirect post-increment	LDR R0, [R1], #4
Double Reg indirect	Register indirect Register indexed	LDR R0, [R1, R2]
Double Reg indirect with scaling	Register indirect indexed with scaling	LDR R0, [R1, r2, LSL #2]
Program counter relative		LDR R0, [PC, #offset]

6. Write the applications of OMAP processor? (GNITC-MAY-2019)

Ans:

The OMAP family consists of three product groups classified by performance and intended applications:

1) Integrated modem and applications processors
2) Basic multimedia applications processors
3) High-performance applications processors

7. What is wakeup interrupt controller? (GNITC-MAY-2019)

Ans:

The **Wakeup Interrupt Controller** (WIC) is a peripheral that can detect an **interrupt** and wake the processor from deep sleep mode. The WIC is enabled only when the system is in deep sleep mode. The WIC is not programmable, and does not have any registers or user interface. It operates entirely from hardware signals

Multiple Choice Questions

Unit-1

1. A microprocessor is a _____ chip integrating all the functions of a CPU of a computer.

A. multiple B. single C. double D. triple

ANSWER: B

2. Microprocessor is a/an _____ circuit that functions as the CPU of the compute

A. electronic B. mechanic C. integrating D. processing

ANSWER: A

3. Microprocessor is the _____ of the computer and it perform all the computational tasks

A. main B. heart C. important D. simple

ANSWER: B

4. The purpose of the microprocessor is to control _____

A. memory B. switches C. processing D. tasks

ANSWER: A

5. The first digital electronic computer was built in the year_____

A. 1950 B. 1960 C. 1940 D. 1930

ANSWER: C

6. In 1960's texas institute invented _____

A. integrated circuits B. microprocessor C. vacuum tubes D. transistors

ANSWER: A

7. The intel 8086 microprocessor is a _____ processor

A. 8 bit B. 16 bit C. 32 bit D. 4 bit

ANSWER: B

8. The microprocessor can read/write 16 bit data from or to _____

A. memory B. I /O device C. processor D. register

ANSWER: A

9. In 8086 microprocessor , the address bus is _____ bit wide

A. 12 bit B. 10 bit C. 16 bit D. 20 bit

ANSWER: D

10. The work of EU is _____

A. encoding B. decoding C. processing D. calculations

ANSWER: B

11. The 16 bit flag of 8086 microprocessor is responsible to indicate _____

A. the condition of result of ALU operation B. the condition of memory

C. the result of addition D. the result of subtraction

ANSWER: A

12. The CF is known as _____

A. carry flag B. condition flag C. common flag D. single flag

.ANSWER: A

13. The SF is called as _____

A. service flag B. sign flag C. single flag D. condition flag

ANSWER: B

14. The OF is called as _____

A. overflow flag B. overdue flag C. one flag D. over flag

ANSWER: A

15. The IF is called as _____

A. initial flag B. indicate flag C. interrupt flag D. inter flag

ANSWER: C

16. The register AX is formed by grouping _____

A. AH & AL B. BH & BL C. CH & CL D. DH & DL

ANSWER: A

17. The SP is indicated by _____

A. single pointer B. stack pointer C. source pointer D. destination pointer

ANSWER: B

18. The BP is indicated by _____

A. base pointer B. binary pointer C. bit pointer D. digital pointer

ANSWER: A

19. The SS is called as _____

A. single stack B. stack segment C. sequence stack .D. random stack

ANSWER: B

20. The index register are used to hold _____

A. memory register B. offset address C. segment memory D. offset memory

ANSWER: A

UNIT-2

1. 8051 micro controller has how many ports
   a) 3 b) 1 c) 2 d) 4

   Answer:d

2. Which of the registers 8051 support indirect addressing
   a) R6-R7 b) R0-R7 c) R0-R1 d) R0-R6
   Answer:d

3. Which of the register of 8051 is 16 bit
   a) A b) PSW c) DPTR d) SP

   Answer:b

4. Which of the opcode is for 8 bit displacement
   a) LMJP b) SJMP c) CALL d) AJMP

   Answer:b

5. 8051 has number of register banks
   a) 3 b) 1 c) 2 d) 4

   Answer:d

6. 8051 is of -----pin package
   a) 40 b) 50 c) 20 d) 30
   Answer:a

7. ALE of 8051 stands for
   a) Address latch enable b) Addition latch enable
   c) Address low enable d) Addition low enable
   Answer:a

8. Internal data memory of 8051 is of
   a) 256 B b) 64 B c) 216 B d) 250 B
   Answer:a

9. External data memory of 8051 is of
   a) 34 KB b) 64 KB c) 16 KB d) 23 KB
   Answer:b

10. Internal program memory of 8051 is of
    a) 4 KB b) 64 KB c) 16 KB d) 50 KB
    Answer:a

11. External program memory of 8051 is of
    a) 34 KB b) 64 KB c) 16 KB d) 23 KB
    Answer:b

12. Direct addressing mode is used for accessing
    a) Internal memory b) External memory c) RAM d) ROM
    Answer:a

13. 8051 has number of user defined flags
    a) 126 b) 124 c) 122 d) 128
    Answer:d

14. 8051 has the crystal oscillator with frequency of
    a) 12 MHz b) 10 MHz c) 11 MHz d) 13 MHz

Answer:d

15. Which port of 8051 has special functions
a) Port 3 b) Port 1 c) Port2 d) Port 4
Answer:d

16. Which of the following is an external interrupt?
a) INT0(active low) b) INT2(active low) c) Timer0 interrupt d) Timer1 interrupt

Answer:a
Explanation: INT0(active low) and INT1(active low) are two external interrupt inputs provided by 8051.

17. The interrupts, INT0(active low) and INT1(active low) are processed internally by flags
a) IE0 and IE1 b) IE0 and IF1 c) IF0 and IE1 d) IF0 and IF1

Answer:a
Explanation: The interrupts, INT0(active low) and INT1(active low) are processed internally by the flags IE0 and IE1.

18. The flags IE0 and IE1, are automatically cleared after the control is transferred to respective vector, if the interrupt is
a) level-sensitive b) edge-sensitive c) in serial port d) in parallel port

Answer: b
Explanation: If the interrupts are programmed as edge sensitive, the flags IE0 and IE1 are automatically cleared after the control is transferred to respective vector.

19. If the external interrupt sources control the flags IE0 and IE1, then the interrupt programmed is
a) level-sensitive b) edge-sensitive c) in serial port d) in parallel port

Answer: a
Explanation: If the interrupts are programmed as level sensitive, then the flags IE0 and IE1 are controlled by external interrupt sources themselves.

20. The pulses at T0 or T1 pin are counted in
a) timer mode b) counter mode c) idle mode d) power down mode

Answer: b
Explanation: In counter mode, the pulses are counted at T0 or T1 pin.

21. In timer mode, the oscillator clock is divided by a prescalar
a) (1/8) b) (1/4) c) (1/16) d) (1/32)

Answer: d
Explanation: In timer mode, the oscillator clock is divided by a prescalar (1/32) and then given to the timer.

22. The serial port interrupt is generated if
a) RI is set b) RI and TI are set c) either RI or TI is set d) RI and TI are reset

Answer: c
Explanation: The serial port interrupt is generated if atleast one of the two bits, RI and TI is set.

23. In serial port interrupt, after the control is transferred to the interrupt service routine, the flag that is cleared is
a) RI b) TI c) RI and TI d) none

Answer: d
Explanation: In serial port interrupt, after the control is transferred to the interrupt service routine, neither of the flags is cleared.

24. The atleast number of machine cycles for which the external interrupts that are programmed level-sensitive should remain high is
a) 1 b) 2 c) 3 d) 0

Answer: b
Explanation: The external interrupts, programmed level-sensitive should remain high for atleast 2 machine cycles.

25. If the external interrupts are programmed edge sensitive, then they should remain high for atleast
a) 0 machine cycle b) 2 machine cycles c) 1 machine cycle d) 3 machine cycles

Answer: c
Explanation: If the external interrupts are programmed edge sensitive, then they should remain high for atleast one machine cycle and low for atleast one machine cycle, for being sensed.

26. The timer generates an interrupt, if the count value reaches to
a) 00FFH b) FF00H c) 0FFFH d) FFFFH

Answer: d
Explanation: the timer is an up-counter and generates an interrupt when the count has reached FFFFH.

27. The external interrupt that has the lowest priority among the following is
a) TF0 b) TF1 c) IE1 d) NONE

Answer: c
Explanation: The order of given interrupts from high to low priority is TF0, IE1 and TF1.

28. Among the five interrupts generated by 8051, the lowest priority is given to the interrupt
a) IE0 b) TF1 c) TF0 d) RI

Answer: d
Explanation: the interrupt, RI=TI (serial port) is given the lowest priority among all the interrupts.

29. Among the five interrupts generated by 8051, the highest priority is given to the interrupt
a) IE0 b) TF1 c) TF0 d) IE1

Answer: a
Explanation: the interrupt, IE0(External INT0) is given the highest priority among all the interrupts.

30. All the interrupts are enabled using a special function register called
a) interrupt priority register b) interrupt register
c) interrupt function register d) interrupt enable register

Answer: d
Explanation: All the interrupts are enabled using a special function register called interrupt enable register (IE) and their priorities are programmed using another special function register called interrupt priority register(IP).

31. The number of bytes stored on the stack during one operation of PUSH or POP is
a) 1 b) 2 c) 3 d) 4

Answer: a
Explanation: As 8051 stack operations are 8-bit wide i.e. in an operation using PUSH or POP instruction, one byte of data is stored on a stack or retrieved from the stack. For implementing 16-bit operations, two 8-bit operations are cascaded.

32. The step involved in PUSH operation is
a) increment stack by 2 and store 8-bit content to address pointed to by SP
b) decrement stack by 1 and store 16-bit content to address pointed to by SP
c) increment stack by 1 and store 8-bit content to address pointed to by SP
d) store 8-bit content to address pointed to by SP and then increment stack by 1

Answer: c

33. The step involved in POP operation is
a) decrement stack by 2 and store 8-bit content to address pointed to by SP
b) store 16-bit content to address pointed to by SP and decrement stack by 1
c) decrement stack by 1 and store content of top of stack to address pointed to by SP
d) store content of top of stack to address pointed to by SP and then decrement stack by 1

Answer: d
Explanation: The POP instruction follows two steps..

34. The 8051 stack is
a) auto-decrement during PUSH operations b) auto-increment during POP operations
c) auto-decrement during POP operations d) auto-increment during PUSH operations

Answer: d
Explanation: The 8051 stack is opposite to that in 8085 or 8086 i.e. in 8085 it is auto-decrement while in 8051 it is auto-increment during PUSH operations.

UNIT-3

1. This set of Microprocessor Multiple Choice Questions & Answers (MCQs) focuses on “Serial Communication Unit”.

1. The serial communication is
a) cheaper communication
b) requires less number of conductors
c) slow process of communication
d) all of the mentioned

Answer: d
Explanation: The serial communication requires less number of conductors and thus it is cheaper. It is slow as the bits are transmitted one by one along with start, stop and parity bits.

2. The serial communication is used for
a) short distance communication
b) long distance communication
c) short and long distance communication
d) communication for a certain range of distance
Answer: b
Explanation: Serial communication is more popular for communication over longer distances as it requires less number of conductors.

3. The mcs 51 architecture supports
a) serial transmission and reception
b) simultaneous transmission and reception
c) transmission and reception of data using serial communication interface
d) all of the mentioned

Answer: d
Explanation: The mcs 51 architecture supports simultaneous transmission and reception of binary data byte by byte i.e. full duplex mode of communication. It supports serial transmission and reception of data using standard serial communication interface and baud rates.

4. The number of bits transmitted or received per second is defined as
a) transmission rate
b) reception rate
c) transceiver rate
d) baud rate
Answer: d
Explanation: Here, baud rate can be defined as the number of bits transmitted or received per second.

5. The task of converting the byte into serial form and transmitting it bit by bit along with start, stop and parity bits is carried out by
a) reception unit
b) serial communication unit
c) transmission unit
d) all of the mentioned

Answer: c
Explanation: the serial communication unit consists of transmission unit and reception unit. The task of converting the byte into serial form and transmitting it bit by bit along with start, stop and parity bits is carried out by transmission unit.

6. The transmission unit does not require assistance from processor if once a byte for transmission is written to
a) SCON register
b) SBUF register
c) SFR address
d) Any of the mentioned

Answer: b
Explanation: once a byte for transmission is written to the serial buffer(SBUF) register, the transmission unit does not require assistance from a processor.

7. The common unit shared by the receiver unit and transmission unit of serial communication unit is
a) SCON(Serial Port Control) Register
b) SBUF(Serial Buffer) register
c) 8-bit serial data interface
d) All of the mentioned

Answer: d
Explanation: The transmission unit and receiver unit both are controlled by using a common SCON(Serial Port Control) Register. Also both units share a common serial buffer(SBUF) register which is a common 8-bit serial data interface.

8. During serial reception, the buffer that receives serial bits and converts to a byte is
a) receive buffer 0
b) receive buffer 1
c) receive buffer 2
d) none

Answer: b
Explanation: During serial reception, the receive buffer 1 receives serial bits and converts to a byte, it then transfers the received parallel byte in receive buffer 2.

9. If SM0=1, SM1=0, then the transceiver selected is
a) 8-bit synchronous
b) 9-bit synchronous
c) 8-bit asynchronous
d) 9-bit asynchronous

Answer: d
Explanation: If SM0=1, SM1=0, then the 9-bit asynchronous transceiver is selected.

10.If the microcontroller is expected to communicate in a multiprocessor system, then the required condition is
a) SM0 is set
b) SM1 is set
c) SM2 is set
d) REN is set

11. SPI stands for

a.serial peripheral interface

b.serial port interrupt

c.serial port internet

d.serial peripheral internet.

Answer: a

12. I2C stands for

a) Internet circuit b) Inter integrated circuit c) Intra circuit d) Inter intermediate circuit

Answer: b

13. UART stands for

a)universal receiver transmitter b) universal asynchronous receiver

c) universal asynchronous transmitter d) universal asynchronous receiver& transmitter

Answer: d

14. RS-232C stands for

a)Recommended standard b)real standard c)receiver standard d) Recommended serial

Answer: a

15.USB stands for

a)universal support bus b)universal serial bus c)universal standard bus d)universal bus

Answer: b

UNIT-4

1. ARM stands for _____
a) Advanced Rate Machines
b) Advanced RISC Machines
c) Artificial Running Machines
d) Aviary Running Machines

Answer:b

The main importance of ARM micro-processors is providing operation with _____
a) Low cost and low power consumption
b) Higher degree of multi-tasking
c) Lower error or glitches
d) Efficient memory management

Answer:a

2. ARM processors where basically designed for _____
a) Main frame systems
b) Distributed systems
c) Mobile systems
d) Super computers
Answer:c

4. The ARM processors don't support Byte addressability.
a) True
b) False
Answer:b

5. The address space in ARM is _____
a) 2^{24}
b) 2^{64}
c) 2^{16}
d) 2^{32}
Answer:d

6. The address system supported by ARM systems is/are _____
a) Little Endian
b) Big Endian
c) X-Little Endian
d) Both Little & Big Endian
Answer:d

7. Memory can be accessed in ARM systems by _____ instructions.
i) Store
ii) MOVE
iii) Load
iv) arithmetic

v) logical
a) i,ii,iii
b) i,ii
c) i,iv,v
d) iii,iv,v
Answer:b

8. RISC stands for _____
a) Restricted Instruction Sequencing Computer
b) Restricted Instruction Sequential Compiler
c) Reduced Instruction Set Computer
d) Reduced Induction Set Computer
Answer:c

9. In the ARM, PC is implemented using ____
a) Caches
b) Heaps
c) General purpose register
d) Stack
Answer:c

10. The additional duplicate register used in ARM machines are called as _____
a) Copied-registers
b) Banked registers
c) EXtra registers
d) Extential registers
Answer:b

11. The banked registers are used for _____
a) Switching between supervisor and interrupt mode
b) Extended storing
c) Same as other general purpose registers
d) None of the mentioned
Answer:a

12. Each instruction in ARM machines is encoded into ____ Word.
a) 2 byte
b) 3 byte
c) 4 byte
d) 8 byte
Answer:c

13. All instructions in ARM are conditionally executed.
a) True
b) False
Answer:a

14. The addressing mode where the EA of the operand is the contents of Rn is _____
a) Pre-indexed mode
b) Pre-indexed with write back mode

c) Post-indexed mode
d) None of the mentioned
Answer:c

15. The effective address of the instruction written in Post-indexed mode, MOVE[Rn]+Rm I

a) EA = [Rn].

b) EA = [Rn + Rm].
c) EA = [Rn] + Rm
d) EA = [Rm] + Rn
Answer:a

UNIT-5

1. ____ symbol is used to signify write back mode.
a) #
b) ^
c) &
d) !
Answer:d

2. The instructions which are used to load or store multiple operands are called as _____
a) Banked instructions
b) Lump transfer instructions
c) Block transfer instructions
d) DMA instructions
Answer:c

3. The Instruction, LDM R10!, {R0,R1,R6,R7} _____
a) Loads the contents of R10 into R1, R0, R6 and R7
b) Creates a copy of the contents of R10 in the other registers except for the above mentioned ones
c) Loads the contents of the registers R1, R0, R6 and R7 to R10
d) Writes the contents of R10 into the above mentioned registers and clears R10
Answer:a

4. The instruction, MLA R0,R1,R2,R3 performs _____
a) R0<-[R1]+[R2]+[R3].
b) R3<-[R0]+[R1]+[R2].
c) R0<-[R1]*[R2]+[R3].
d) R3<-[R0]*[R1]+[R2].
Answer:c

5. The ability to shift or rotate in the same instruction along with other operation is performed with the help of _____
a) Switching circuit
b) Barrel switcher circuit
c) Integrated Switching circuit
d) Multiplexer circuit

Answer:b

6. _____ instruction is used to get the 1's complement of the operand.
a) COMP
b) BIC
c) ~CMP
d) MVN
Answer:d

7. The offset used in the conditional branching is ____ bit.
a) 24
b) 32
c) 16
d) 8
Answer:a

8. The BEQ instructions is used _____
a) To check the equality condition between the operands and then branch
b) To check if the Operand is greater than the condition value and then branch
c) To check if the flag Z is set to 1 and then causes branch
d) None of the mentioned
Answer:c

9. The condition to check whether the branch should happen or not is given by _____
a) The lower order 8 bits of the instruction
b) The higher order 4 bits of the instruction
c) The lower order 4 bits of the instruction
d) The higher order 8 bits of the instruction
Answer:b

10. Which of the two instructions sets the condition flag upon execution?
i) ADDS R0,R1,R2
ii) ADD R0,R1,R2
a) i
b) ii
c) Both i and ii
d) Insufficient data
Answer:a

11. ____ directive is used to indicate the beginning of the program instruction or data.
a) EQU
b) START
c) AREA
d) SPACE
Answer:c

12. _____ directive specifies the start of the execution.
a) START
b) ENTRY

c) MAIN
d) ORIGIN
Answer:b

13. _____ directives are used to initialize operands.
a) INT
b) DATAWORD
c) RESERVE
d) DCD
Answer:d

14. _____ directive is used to name the register used for execution of an instruction.
a) ASSIGN
b) RN
c) NAME
d) DECLARE
Answer:b

15. The pseudo instruction used to load an address into the register is _____
a) LOAD
b) ADR
c) ASSIGN
d) PSLOAD
Answer:b

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OBJECT ORIENTED PROGRAMMING THROUGH JAVA (210E0CS1A)- HANDBOOK

B.TECH. [III/ II]

Academic Year: 2023-2024

DEPARTMENT OF ELECTRONICS AND COMMUNICATIONS ENGINEERING

SCHOOL OF ENGINEERING AND TECHNLOGY

OBJECT ORIENTED PROGRAMMING THROUGH JAVA (210E0CS1A)-HANDBOOK

COURSE INFORMATION SHEET

PROGRAMME: Electronics and Communication Engineering	DEGREE: B. Tech.
COURSE: Object Oriented Programming Through Java	SEMESTER: II Sem CREDITS: 3
COURSE CODE: REGULATION: R21	COURSE TYPE: CORE
COURSE AREA/DOMAIN: Programming Language	CONTACT HOURS: 3 hours/week
CORRESPONDING LAB COURSE CODE (IF ANY): -	LAB COURSE NAME: -

PRE-REQUISITE:

1. A course on “Programming for Problem Solving”

COURSE OBJECTIVE:

The aim of this course is to comprehend object oriented programming concepts and apply them in problem solving

SYLLABUS:

UNIT – I

OOP concepts: Classes and objects, data abstraction, encapsulation, inheritance, benefits of inheritance, polymorphism, procedural and object oriented programming paradigm; Java programming: History of java, comments data types, variables, constants, scope and life time of variables, operators, operator hierarchy, expressions, type conversion and casting, enumerated types, control flow statements, jump statements, simple java stand alone programs, arrays, console input and output, formatting output, constructors, methods, parameter passing, static fields and methods, access control, this reference, overloading methods and constructors, recursion, garbage collection, exploring string class.

UNIT – II

Inheritance: Inheritance hierarchies, super and subclasses, member access rules, super keyword, preventing inheritance: final classes and methods, the object class and its methods; Polymorphism: Dynamic binding, method overriding, abstract classes and methods; Interface: Interfaces vs Abstract classes, defining an interface, implement interfaces, accessing implementations through interface references, extending interface; Packages: Defining, creating and accessing a package, understanding CLASSPATH, importing packages.

UNIT – III

Exception Handling: Benefits of exception handling, the classification of exceptions, exception hierarchy, checked and unchecked exceptions, usage of try, catch, throw, throws and finally, re-throwing exceptions, exception specification, built in exceptions, creating own exception sub classes. Multithreading: Differences between multiple processes and multiple threads, thread states, creating threads, interrupting threads, thread priorities, synchronizing threads, inter thread communication.

UNIT – IV

Files: Streams, byte streams, character stream, text input/output, binary input/output, random access file operations, file management using file class; Connecting to Database: Connecting to a database, querying a database and processing the results, updating data with JDBC.

UNIT – V

GUI programming with Java: The AWT class hierarchy, introduction to swing, swing Vs AWT, hierarchy for swing components, containers, JFrame, JApplet, JDialog, JPanel; Overview of some swing components: JButton, JLabel, JTextField, JTextArea, simple applications; Layout management: Layout manager types: Border, grid and flow; Applets: Inheritance hierarchy for applets, differences between applets and applications, life cycle of an applet, passing parameters to applets.

TEXT BOOKS:

1. Herbert Schildt, Dale Skrien, "Java Fundamentals: A Comprehensive Introduction", McGraw Hill, 1st Edition, 2013.

2. Herbert Schildt, "Java the Complete Reference", McGraw Hill, Osborne, 8th Edition, 2011.

3. T. Budd, "Understanding Object Oriented Programming with Java", Pearson Education, Updated Edition (New Java 2 Coverage), 1999.

REFERENCE BOOKS:

P.J. Deitel, H. M. Deitel, "Java: How to Program", Prentice Hall, 6th Edition, 2005.

P. Radha Krishna, "Object Oriented Programming through Java", Universities Press, CRC Press, 2007.

Bruce Eckel, "Thinking in Java", Prentice Hall, 4th Edition, 2006.

Sachin Malhotra, Saurabh Chaudhary, "Programming in Java", Oxford University Press, 2nd Edition, 2014.

COURSE OUTCOMES:

CO 1: Describe the concepts of OOP and basics of java programming

CO 2: Express the programming skills in problem solving

CO 3: Solve the exceptions and handle the exceptions in programming

CO 4: Extend the knowledge to Working with files and Connecting to the Database

CO 5: Extend their knowledge to GUI applications

MODEL LESSON PLAN / CONSOLIDATED UNIT WISE LESSON PLAN

Subject	Object Oriented Programming through JAVA
Faculty	Mrs.CH.Lavanya Kumari
Text Books (to be acquired by the Students)	
Book 1	Herbert Schildt, Dale Skrien, "Java Fundamentals: A Comprehensive Introduction", McGraw Hill, 1st Edition, 2013.
Book 2	Herbert Schildt, "Java the Complete Reference", McGraw Hill, Osborne, 8th Edition, 2011.
Reference Books	
Book 3	.J. Deitel, H. M. Deitel, "Java: How to Program", Prentice Hall, 6th Edition, 2005.

Unit	Topic	Chapters			No of Classes
		Book 1	Book 2	Book 3	
I	Object oriented Programming Concepts	Chap-1, 2,3,4,5,6,7	Chap-1,2	Chap 1	15
II	Inheritance	Chap-8,9	Chap 3,4	Chap 2,3	12
III	Exception handling, Multithreading	Chap-10,12	Chap 4,5	Chap 4,5	10
IV	Files	Chap-11	Chap 7,8	Chap 6,7	9
V	GUI programming with Java	Chap-17,18	Chap 9,10	Chap 8,9	9
Total Classes					55
Tutorial Classes					06
Classes for Beyond Syllabus-03, Remedial Classes-04, Descriptive Tests-02					09
Total Number of Classes					70

MICRO LESSON PLAN

Sl. No	Name of the Topic	No. of Classes required	Cumulative number of periods	Teaching AID
	UNIT – I			
1	OOP concepts: Classes and objects, data abstraction	1	1	PPT/Chalk & Talk
2	encapsulation, inheritance, benefits of inheritance, polymorphism,	1	2	PPT/Chalk & Talk
3	procedural and object oriented programming paradigm;	1	3	PPT/Chalk & Talk
4	Java programming	1	4	
5	Tutorial Class	1	5	PPT/Chalk & Talk
6	History of Java, Java buzzwords, data types, variables,constants	2	6	PPT/Chalk & Talk
7	scope and life time of variables,	1	7	PPT/Chalk & Talk
8	operators,operator hierarchy	1	8	
9	expressions, type conversion and casting,enumerated types, control flow statements, jump statements	1	9	PPT/Chalk & Talk
10	Tutorial Class	1	10	PPT/Chalk & Talk
11	simple java program, arrays,console input and output,	1	11	PPT/Chalk & Talk
12	formatting output,constructors, methods,	1	12	
13	Parameter passing ,static fields and methods access, control,	2	13	PPT/Chalk & Talk
14	This reference, overloading methods and constructors	1	14	PPT/Chalk & Talk
15	recursion,garbage collection ,	1	15	PPT/Chalk & Talk
16	exploring string class.	1	16	
17	Descriptive Test	1	17	Practice

18	Remedial/NPTEL	1	18	Practice
UNIT – II				
19	Inheritance: Inheritance hierarchies, super and subclasses	1	19	PPT/Chalk & Talk
20	Member access rules, super keyword	1	20	PPT/Chalk & Talk
21	preventing inheritance: final classes and methods,	1	21	PPT/Chalk & Talk
22	the object class and its methods	1	22	
23	Tutorial Class	1	23	Practice
24	Polymorphism: Dynamic binding, method overriding,	1	24	PPT/Chalk & Talk
25	abstract classes and methods	1	25	
26	Interface: Interfaces vs Abstract classes,	1	26	PPT/Chalk & Talk
27	defining an interface,	1	27	PPT/Chalk & Talk
28	implement interfaces,	1	28	PPT/Chalk & Talk
29	accessing implementations through interface references, extending interface;	1	29	PPT/Chalk & Talk
30	Packages: Defining, creating and accessing a package,	1	30	PPT/Chalk & Talk
31	Understanding CLASSPATH, importing packages	2	31	PPT/Chalk & Talk
32	Remedial/NPTEL	1	32	Practice
33	Special Descriptive test-1	1	33	Test
UNIT – III				
34	Exception handling and Multithreading-- benefits of exception handling, the classification of exceptions	1	34	PPT/Chalk & Talk
35	exception hierarchy, checked and unchecked exceptions,	1	35	PPT/Chalk & Talk
36	Tutorial Class	1	36	Practice
37	usage of try, catch, throw, throws and finally,	1	37	PPT/Chalk & Talk
38	re-throwing exceptions, exception specification,	1	38	

39	built in exceptions, creating own exception sub classes	1	39	PPT/Chalk & Talk
40	Multithreading: Differences between multiple processes and multiple threads,	1	40	PPT/Chalk & Talk
41	thread states, creating threads,	2	41	PPT/Chalk & Talk
42	interrupting threads,	1	42	
43	thread priorities, synchronizing threads,	1	43	PPT/Chalk & Talk
44	inter thread communication	2	44	PPT/Chalk & Talk
45	Remedial/NPTEL	1	45	Practice
46	Classes for Beyond Syllabus	1	46	Guest Lecture
UNIT – IV				
47	Files: Streams,	1	47	PPT/Chalk & Talk
48	Byte Streams	1	48	PPT/Chalk & Talk
49	character streams	1	49	PPT/Chalk & Talk
50	Tutorial Class	1	50	Practice
51	text input/output, binary input/output	1	51	PPT/Chalk & Talk
52	random access file operations,	1	52	PPT/Chalk & Talk
53	file management using file class;	1	53	PPT/Chalk & Talk
54	Connecting to Database: Connecting to a database, querying a database	1	55	PPT/Chalk & Talk
55	processing the results,	1	56	PPT/Chalk & Talk
56	updating data with JDBC	1	57	PPT/Chalk & Talk
57	Remedial/NPTEL	1	58	Practice
UNIT V				
58	The AWT class hierarchy, introduction to swing, swing Vs AWT	1	59	PPT/Chalk & Talk
59	hierarchy for swing components, containers, JFrame, JApplet, JDialog, Jpanel	1	60	PPT/Chalk & Talk
60	Overview of some swing components: JButton, JLabel, JTextField, JTextArea, simple applications	1	61	PPT/Chalk & Talk
61	Tutorial Class	1	62	Practice

62	Layout management: Layout manager types: Border	1	63	PPT/Chalk & Talk
63	grid and flow	1	64	PPT/Chalk & Talk
64	Applets: Inheritance hierarchy for applets	1	65	PPT/Chalk & Talk
65	differences between applets and applications	1	66	PPT/Chalk & Talk
66	life cycle of an applet	1	67	PPT/Chalk & Talk
67	passing parameters to applets.	1	68	PPT/Chalk & Talk
68	Topics Beyond Syllabus	1	69	Guest Lecture
69	Tutorial class	1	70	Practice

Total Classes	55
Tutorial Classes	06
Topics for Beyond Syllabus	03
Descriptive Tests	02
Remedial classes/NPTEL	04
Total Number of Classes	70

ASSIGNMENT QUESTIONS

PART-A QUESTIONS

Unit / Question	BTL	Course Outcome
Unit-I		
1. What is the size of char data type? Why does it differ from C language? (JNTUH Dec-17,R13)	L1	CO1
2. Define Data abstraction. (JNTUH Dec-17,R13)	L1	CO1
3.What are the features of Java Language? (JNTUH May-17R15)	L1	CO1
4. List the types of operators used in Java. (JNTUH May-17R15)	L1	CO1
5. What is Static Inner class? (JNTUH May-17R15)	L1	CO1
6. Distinguish between break and continue. (JNTUH May-16R13)	L1	CO1
7. What is type casting? (JNTUH May-16R13)	L1	CO1
8. List String manipulation functions of Java String class. (JNTUHMay-15R13)	L1	CO1
9. Define Polymorphism. (JNTUH Nov-16R13)	L1	CO1
10. Why Java is known as Platform independent? (JNTUH Nov-16R13)	L1	CO1
Unit-II		
1. What is package? (JNTUH Dec-17R13)	L1	CO2
2. What is the use of Super keyword? (JNTUH May-16R13)	L1	CO2
3. Distinguish between abstract class and concrete class. (JNTUH May-16 R13, Dec-18R15)	L1	CO2
4. What is Java package? What is CLASSPATH? (JNTUH May-17R15, May-18R16)	L1	CO2
5. Differentiate between interface and Abstract class. (JNTUH May-15R13, JNTUH Jun-14R15, Dec-18R15)	L1	CO2
6. What are the uses of final keyword in java? (JNTUH May-15R13, Dec-18R15)	L1	CO2
7. What is Runtime Polymorphism? (JNTUH Jun-14)	L1	CO2
8.What is the significance of the CLASSPATH environment variable in creating/using a package? (JNTUH Dec-17R16)	L1	CO2
9.What is abstract class?Give example. (JNTUH May-18R16)	L1	CO2
10.Write about hierarchical and multiple inheritance using interfaces.(GNITC Oct 2020 R18)	L1	CO2
Unit-III		
1.Differentiate between error and exception. (JNTUH Dec-17R16)	L1	CO3
2.Explain how multiple catch statements work. (JNTUH May-17R15,Dec-18R15)	L1	CO3
3.What are the advantages of multithreading? (JNTUH May-16R13)	L1	CO3
4. What are the types of Exceptions? (JNTUH May-16R13)	L1	CO3
5.List any six built-in exceptions in java. (JNTUH May-15R13)	L1	CO3
6.What are checked and unchecked Exceptions? (JNTUHMay-16R13)	L1	CO3
7.What is Synchronization and why it is important? (JNTUH Dec-17R16)	L1	CO3
8.How do we start and stop a thread? (JNTUH May-18R16)	L1	CO3
9.Write the complete life cycle of thread. (JNTUH May-18R16)	L1	CO3
10.How do we set Priorities for threads? (JNTUH May-18R16)	L1	CO3
Unit-IV		
1.Compare byte streams with Character Stream. (JNTUH Dec-18 R15)	L1	CO4
2. List file access operations. (JNTUH Dec-18 R15)	L1	CO4
3.What are the methods available in Character Stream? (JNTUH Dec-17 R16)	L1	CO4
4.What types of streams does java define? (JNTUH Dec-18 R15)	L1	CO4
5.What streams are used to read and write binary data?(JNTUH Dec-18 R15)	L1	CO4
6.Write the syntax to create a random file. (JNTUH April/May-2018 R15)	L1	CO4
7.What class is used to read characters from a file? Write the syntax.	L1	CO4

(JNTUHMay-18 R15)		
8.What method is used to list the files in a directory?(JNTUH Dec-18 R15)	L1	CO4
9.Write a program to compare two files? (JNTUH Dec-18 R15)	L1	CO4
10.What is the use of FileInputStream and FileOutputStream? (JNTUH Dec-18 R15)	L1	CO4
Unit-V		
1. What is the use of Layout Manager? (JNTUH May-17 R13, Dec-17 R13)	L1	CO5
2. Give the hierarchy for swing components. (JNTUH Dec-17R13)	L1	CO5
3. What are the containers available in Swings? (JNTUH May-15,R13)	L1	CO5
4.Difference between Applet and Application. (JNTU May-16,May-15,R13)	L1	CO5
5. What are the limitations of AWT? (JNTUH May-18R16)	L1	CO5
6.Why do applet class need to be declared as public? (JNTUH May-18R16)	L1	CO5
7.What is Swing in Java? How it is differs from Applet? (JNTUH Dec-18R16)	L1	CO5
8.How do Java applets differ from Application programs? (JNTUH Dec-18R16)	L1	CO5
9.List the types of containers. (JNTUH Dec-18R16)	L1	CO5
10.Write a simple program for swing.(JNTUH May-18R16)	L1	CO5

PART-B QUESTIONS

Unit / Question	BTL	Course Outcome
Unit-I		
1.Describe the structure of a typical Java program with an example. (JNTUH Dec-18R16)	L2	CO1
2.Write the significance of Java Virtual Machine. (JNTUH Dec-18R16)	L2	CO1
3.How do we implement polymorphism in Java? (JNTUH Dec-18R16)	L2	CO1
4. What is a Array? How to declare Array in Java? Give Examples. (JNTUH Dec-18R16)	L2	CO1
5.What is inheritance and how does it help to create new classes quickly? (JNTUH May-18R16)	L2	CO1
6.Describe different levels of access protection available in Java. (JNTUH May-18R16)	L2	CO1
7.List and explain the primitive data types available in Java. (JNTUH May-18R16)	L2	CO1
8.What is polymorphism? Explain different types of polymorphisms with example. (JNTUH May-18R16)	L2	CO1
9. What is meant by byte code? Briefly explain how Java is platform independent. (JNTUH Dec-17R16)	L2	CO1
10.Explain the significance of public,protected and private access specifiers in inheritance. (JNTUH Dec-17R16)	L2	CO1
Unit-II		
1. What is package? How do you create a package with suitable examples? (JNTUH Dec-17 R16)	L2	CO2
2.Give an example where interface can be used to support multiple inheritance(JNTUH Dec-17R16, May-18 R16)	L2	CO2
3.What is the accessibility of a public method or field inside a non public class or interface? Explain. (JNTUH Dec-17R16)	L2	CO2
4. What is an interface? What are the similarities between interface and classes? (JNTUH May-18R16)	L2	CO2
5.How can you extend one interface by the other interface? Discuss. (JNTUH May-18R16)	L2	CO2
6.Discuss about CLASSPATH environment variables. (JNTUH May-18R16)	L2	CO2
7.How to design and implement interface in Java? Give Example. (JNTUH May-18R16)	L2	CO2
8.What are the three uses of final keyword? Explain with example. (JNTUH May-17 R13)	L2	CO2
9.Make a comparison between the Classes and Interfaces. (JNTUH Nov-16R13)	L2	CO2
10. How can you extend one interface by the other interface? Discuss.(GNITC Oct-2020 R18)	L2	CO2
Unit-III		
1. Write a program to use multiple catch blocks in a try block. (JNTUH Dec-17R13, Dec-18R15)	L2	CO3
2.What is an Exception? How is an Exception handled in Java? (JNTUH Dec-18R16)	L2	CO3
3.Differentiate between multiprocessing and multithreading. (JNTUH Dec-18R16)	L2	CO3
4.What are the advantages of using Exception handling mechanism in a program? (JNTUH May-18R16)	L2	CO3
5.Write a java program that demonstrates how certain exception types are not allowed to be thrown. (JNTUH May-18R16)	L2	CO3
6.Explain about multiple threaded programs in Java? (JNTUH May-18R16)	L2	CO3
7.Write a program to create four threads using Runnable interface. (JNTUH May-	L2	CO3

18R16)		
8.Differentiate between checked and unchecked exceptions with examples. (JNTUH Dec-17R16)	L2	CO3
9.What are the different ways to handle exceptions? Explain. (JNTUH May-18R16)	L2	CO3
10.Explain about thread life cycle. (JNTUH May-18R16)	L2	CO3
Unit-IV		
1. What are the methods available in the Character Stream? (JNTUH Dec-18R16)	L2	CO4
2.Distinguish between Byte Stream and Character Stream Classes. (JNTUH Dec-18R16)	L2	CO4
3.Explain the types of drivers used in JDBC. (JNTUH May-16R13)	L2	CO4
4. What is JDBC? Explain the role & responsibility of JDBC API. (GNITC Dec-19)	L2	CO4
5. What is Driver Manager Class? Explain the types of JDBC Driver with suitable diagram. (GNITC Dec-19)	L2	CO4
6. What is Thin Driver? Which driver is fast among the four JDBC drivers? Justify. (GNITC Dec-19)	L2	CO4
7. What is statement? Explain the types of statement in JDBC. ? (JNTUHDec-18 R16)	L2	CO4
8.How to read and write files in java? Explain with example? JNTUH May-16R13)	L2	CO4
9.Write about character streams (JNTUHDec-17 R16)	L2	CO4
10.Write aboutbinary verses text files? (JNTUH Dec-18R16)	L2	CO4
Unit-V		
1. Explain about parameter passing to applets. (JNTUH Mar-17R13)	L2	CO5
2.What is the difference between init() and start() methods in an Applet? When will each be executed?(JNTUH Dec-18R16)	L2	CO5
3.Write about the difference between applet and application(JNTUH Dec-18R16, May-18R16)	L2	CO5
4.Explain various layout managers in Java. (JNTUH Dec-18R16, May-18R16)	L2	CO5
5.What is an Applet? Explain the life cycle of Applet with neat sketch. (JNTUH May-18R16)	L2	CO5
6.Write a program that create a frame window that responds to key strokes. (JNTUH May-18R16)	L2	CO5
7.Discuss about different applet display methods in brief. (JNTUH Dec-17R16)	L2	CO5
8.Explain the various components of Swings. (JNTUH Dec-17R16)	L2	CO5
9.Explain move or drag component placed in Swing Container. (JNTUH Dec-17R16	L2	CO5
10. Write a Swing Program using checkboxes and radio buttons. (JNTUH Dec-15 R07)	L2	CO5

OBJECTIVE TYPE QUESTIONS

UNIT I

1. Which of these operators is used to allocate memory for an object?
A. malloc

B. alloc

C. new

D. give

2. What is the return type of a method that does not returns any value?
A. int

B. float

C. void

D. double

3. Which of the following is a method having same name as that of it's class?
A. finalize

B. delete

C. class

D. constructor

4. Which keyword is used by method to refer to the object that invoked it?
A. import

B. catch

C. abstract

D. this

5. Which function is used to perform some action when the object is to be destroyed?
A. finalize()

B. delete()

C. main()

D. None of the mentioned

6. Which of these can be overloaded?
A. Methods

B. Constructors

C. All of the mentioned

D. None of the mentioned

7. Which of these is used to access member of class before object of that class is created?
A. public

B. private

C. static

D. protected

8. Which of these cannot be declared static?
A. class

B. object

C. variable

D. method

9. Which of these method of String class is used to obtain character at specified index?
A. char()

B. Charat()

C. charat()

D. charAt()

10. Which of these keyword must be used to inherit a class?
A. super

B. this

C. extent

D. extends

11. What is the process of defining a method in subclass having same name & type signature as a method in its superclass?
A. Method overloading

B. Method overriding
C. Method hiding

D. None of the mentioned

12. Which of these keywords can be used to prevent Method overriding?
A. static

B. constant

C. protected

D. final

13. Which of these class is superclass of every class in Java?
A. String class

B. Object class

C. Abstract class

D. ArrayList class

14. Which of these keywords can be used to prevent inheritance of a class?
A. super

B. constant

C. Class

D. final

15. Which of these class is superclass of String and StringBuffer class?
A. java.util

B. java.lang

C. ArrayList

D. None of the mentioned

16. Which of these method of class String is used to obtain length of String object?
A. get()

B. Sizeof()

C. lengthof()

D. length()

17. Which of these cannot be declared static?
A. class

B. object

C. variable

D. method

18. Which of these is a process of converting a simple data type into a class?
A. type wrapping

B. type conversion

C. type casting

D. None of the Mentioned.

19. Which of these keywords is used to define packages in Java?

A. pkg

B. Pkg

C. package

D. Package

20. Which of these keywords is used to define interfaces in Java?
A. interface

B. Interface

C. intf

D. Intf

21. What is the extension of compiled java classes?

a) .txt
b) .js
c) .class
d) .java

22. Which of these are selection statements in Java?

a) break
b) continue
c) for()
d) if()

23.Which of these is not a bitwise operator?

a)&
b)&=
c)|=
d) <=

24. Which of these can be returned by the operator &?

a)Integer
b)Boolean
c)Character
d) Integer or Boolean

25. Literal can be of which of these data types?

a) integer
b) float
c) boolean
d) all of the mentioned

UNIT II

1. Java does not support multiple inheritance, but some of the abilities of multiple inheritance are available by

A. Implementing interfaces.

B. Creating aliases.

C. Importing classes.

D. Using public rather than protected or private modifiers.

2. In order to determine the type that a polymorphic variable refers to, the decision is made by the

A. Operating system when the program is loaded into memory.

B. Java run-time environment at run time.

C. Compiler at compile time.

D. Programmer at the time the program is written.

3. The relationship between a parent class and a child class is referred to as a(n) _____ relationship.

A. is-a

B. was-a

C. has-a

D. instance-of

4. _____ is the process by which object of one class acquires the properties of object of another class

A. Encapsulation

B. Data hiding

C. Inheritance

D. None of the above

5. The concept of inheritance provides the idea of _____

A. taking more than one form

B. reusability

C. data hiding

D. None of the above

6. The derived class is known as _____

A. superclass

B. subclass

C. parentclass

D. None of the above

7. The class from which the subclass derives the properties is called as _____

A. superclass

B. subclass

C. baseclass

D. None of the above

8. The property or the ability to take more than one form is called as _____

A. encapsulation

B. polymorphism

C. inheritance

D. None of the above

9. Polymorphism is extensively used in implementing _____

A. encapsulation

B. polymorphism

C. inheritance

D. None of the above

10. Java achieves dynamic polymorphism using

A. encapsulation

B. data hiding

C. method overriding

D. inheritance

11. Which of these keywords is used to define interfaces in Java?

A. interface

B. Interface

C. intf

D. Intf

12. Which of these can be used to fully abstract a class from its implementation?

A. Objects

B. Packages

C. Interfaces

D. None of the Mentioned.

13. Which of these access specifiers can be used for an interface?

A. Public

B. Protected

C. private

D. All of the mentioned

14. Which of these keywords is used by a class to use an interface defined previously?

A. import

B. Import

C. implements

D. Implements

15. Which of the following is correct way of implementing an interface salary by class manager?

A. class manager extends salary {}

B. class manager implements salary {}

C. class manager imports salary {}

D. None of the mentioned.

16. Which of the following is incorrect statement about packages?

A. Interfaces specify what class must do but not how it does.

B. Interfaces are specified public if they are to be accessed by any code in the program.

C. All variables in interface are implicitly final and static.

D. All variables are static and methods are public if interface is defined pubic.

17. Which of the following package stores all the standard java classes?

A. lang

B. java

C. util

D. java.packages

18. Which of these interfaces declares core method that all collections will have?

A. Set

B. EventListner

C. Comparator

D. Collection

19. Which of this interface handle sequences?

A. Set

B. List

C. Comparator

D. Collection

20. Which of this interface is not a part of Java's collection framework?

A. List

B. Set

C. SortedMap

D. SortedList

UNIT III

1. When does Exceptions in Java arises in code sequence?
A. Run Time

B. Compilation Time

C. Can Occur Any Time

D. None of the mentioned

2. Which of these keywords is not a part of exception handling?
A. try

B. finally

C. thrown

D. catch

3. Which of these keywords must be used to monitor for exceptions?
A. try

B. finally

C. throw

D. catch

4. Which of these keywords must be used to handle the exception thrown by try block in some rational manner?
A. try

B. finally

C. throw

D. catch

5. Which of these keywords is used to manually throw an exception?
A. try

B. finally

C. throw

D. catch

6. In Java, exceptions are divided into two categories, namely checked and unchecked exceptions.

A. True

B. False

7. The subclass exception should precede the base class exception when used within the catch clause.

A. True

B. False

8. What are checked exceptions

A. checked by java compiler

B. checked by java virtual machine

C. above two

D. none of the above

9. Is it possible to re-throw exceptions

A. True

B. False

10. What are unchecked exceptions

A. checked by java compiler

B. checked by java virtual machine

C. above two

D. none of the above

11. exception is available in util package

A. True

B. False

12. The statements following the throw keyword in a program are not executed.

A. True

B. False

13. Finally block will get invoke whether the exception is thrown or not

A. True

B. False

14. If you throw an exception in your code, then you must declare it using the throws keyword in your method declaration.

A. True

B. False

15. Question: Match each situation in the first list with an item in the second list. a)int[] A; A[0] = 0; b)The JVM starts running your program, but the JVM can't find the Java platform classes. (The Java platform classes reside in classes.zip or rt.jar.) c)A program is reading a stream and reaches the end of stream marker. d)Before closing the stream and after reaching the end of stream marker, a program tries to read the stream again. 1__error 2__checked exception 3__compile error 4__no exception

A. a-2,b-1,c-3,d-4

B. a-4,b-3,b-2,c-1

C. a-3,b-1,c-4,d-2

D. a-1,b-2.c-3.d-4

16. Creating an exception object and handling it to the run time system is called

A. exception handler

B. catch the exception

C. pass the exception

D. throwing an exception

17. Pick runtime exception?

A. class cast exception

B. File not found exception

C. Nullpointer exception

D. security exception

18. Checked exceptions include all subtypes of Exception, including classes that extend RuntimeException.

A. True

B. False

19. Exceptions can be caught or rethrown to a calling method.

A. True

B. False

20. Which one of the following statement is correct?

A. The ‘try’ block should be followed by a ‘catch’ block.

B. The ‘try’ block should be followed by a ‘finally’ block.

C. The ‘try’ block should be followed by either a ‘catch’ block or a ‘finally’ block.

D. The ‘try’ block should be followed by at least two ‘catch’ blocks. The ‘try’ block should be followed by at least two ‘catch’ blocks.

UNIT IV

1. Which of these classes contains the methods used to write in a file?
A. FileStream

B. FileInputStream
C. BUfferedOutputStream

D. FileBufferStream

2. Which of these exceptions is thrown in cases when the file specified for writing it not found?
A. IOException

B. FileException
C. FileNotFoundException

D. FileInputException

3. Which of these methods are used to read in from file?
A. get()

B. read()

C. scan()

D. readFileInput()

4. Which of these values is returned by read() method is end of file (EOF) is encountered?
A. 0

B. 1

C. -1

D. Null

5. Which of these exception is thrown by close() and read() methods?
A. IOException

B. FileException
C. FileNotFoundException

D. FileInputOutputException

6. Which of these methods is used to write () into a file?
A. put()

B. putFile()

C. write()

D. writeFile()

7. The JDBC-ODBC Bridge supports multiple concurrent open statements per connection?

A. yes

B. No

8. A Java program cannot directly communicate with an ODBC driver because .....

A. ODBC written in C language
B. ODBC written in C# language
C. ODBC written in C++ language
D. ODBC written in Basic language

9. Which of this class is used to read from a file?

A. InputStream

B. BufferedInputStream

C. FileInputStream

D. BufferedFileInputStream

10. _____method returns the length of this file.

A. len()

B. lengthof()

C. length()

D. lengthofFile()

11. Which of this class is used to read characters and strings in Java from console?

A. BufferedReader

B. StringReader

C. BufferedStreamReader

D. InputStreamReader

12. Which of this class is implemented by FilterInputStream class?

A. InputStream

B. InputOutputStream

C. BufferedInputStream

D. SequenceInputStream

13. Which of these classes are used by character streams input operations?

A. InputStream

B. Reader

C. ReadStream

D. InputOutputStream

14. _____method closes this random access file stream

A. closeat()

B. close()

C. closed()

D. exitall()

15. Which of this class is implemented by FilterOuputStream class?

A. OuputStream

B. InputOutputStream

C. BufferedInputStream

D. SequenceInputStream

16. _____method sets the file-pointer offset, measured from the beginning of this file, at which the next read or write occurs.

A. getfp()

B. seek()

C. setfp()

D. offset()

17. Which of these class is used for reading and writing to random access file

A. RandomAccessFile

B. InputOutputStream

C. BufferedInputStream

D. SequenceInputStream

18. _____method creates the directory named by this abstract pathname

A. listDir()

B.createDir()

C. mkdir()

D. dir()

19. _____method returns an array of abstract pathnames denoting the files in the directory denoted by this abstract pathname.

A. list()

B. seek()

C. listFiles()

D. listdir()

20. Which of these method(s) is/are used for writing bytes to an outputstream?

A. put()

B. print() and write()

C. printf()

D. write() and read()

UNIT V

1. Which of these methods is a part of Abstract Window Toolkit (AWT) ?
A. display()

B. print()

C. drawString()

D. transient()

2. Which of these functions is called to display the output of an applet?
A. display()

B. print()

C. displayApplet()

D. PrintApplet()

3. Which of these methods can be used to output a sting in an applet?
A. display()

B. print()

C. drawString()

D. transient()

4. What does AWT stands for?
A. All Window Tools

B. All Writing Tools
C. Abstract Window Toolkit

D. Abstract Writing Toolkit

5. What is the most number of states a CheckBox can have?

A. 0

B. 1

C. 2

D. 3

6. What is the standard prefix for the name of a CheckBox?

A. chb

B. chk

C. ckb

D. ckx

7. A CheckBox can also appear as a(n):

A. button

B. RadioButton

C. ScrollBar

D. Both a and b

8. What is the standard prefix for the name of a RadioButton?

A. rad

B. rab

C. rdo

D. rdb

9. How many RadioButtons in a Group Box can be selected at the same time?

A. 0

B. 1

C. 2

D. 3

10. Which of these methods is a part of Abstract Window Toolkit (AWT)?
A. display()

B. paint()

C. drawString()

D. transient()

11. Which of these modifiers can be used for a variable so that it can be accessed from any thread or parts of a program?
A. transient

B. volatile

C. global

D. No modifier is needed

12. Which of these package is used for text formatting in Java programming language?
A. java.text

B. java.awt

C. java.awt.text

D. java.io

13. Where are the following four methods commonly used?
A. public void add(Component c)

B. public void setSize(int width,int height)
C. public void setLayout(LayoutManager m)

D. public void setVisible(boolean)

14. Which is the container that doesn't contain title bar and MenuBars but it can have other components like button, textfield etc?

A. Window

B. Frame

C. Panel

D. Container

15. In Graphics class which method is used to draws a rectangle with the specified width and height?
A. public void drawRect(int x, int y, int width, int height)

B. public abstract void fillRect(int x, int y, int width, int height)

C. public abstract void drawLine(int x1, int y1, int x2, int y2)

D. public abstract void drawOval(int x, int y, int width, int height)

16. Which of these operators can be used to get run time information about an object?

A. getInfo

B. Info

C. instanceof

D. getinfoof

17. Name the class used to represent a GUI application window, which is optionally resizable and can have a title bar, an icon, and menus.

A. Window

B. Panel

C. Dialog

D. Frame

18. Which is a component in AWT that can contain another component like buttons, text fields, labels etc.?

A. Window

B. Container

C. Panel

D. Frame

19. What are the different types of controls in AWT?

A. Labels

B. Pushbuttons

C. Checkboxes

D. Choice lists

20. Which class provides many methods for graphics programming?

A. java.awt

B. java.Graphics

C. java.awt.Graphics

D. None of the above

KEY:

UNIT-I	UNIT-II	UNIT-III	UNIT-IV	UNIT-V
1.C	1.A	1.B	1.B	1.C
2.C	2.B	2.C	2.C	2.A
3.D	3.A	3.C	3.B	3.C
4.D	4.C	4.B	4.C	4.C
5.A	5.B	5.D	5.C	5.B
6.C	6.B	6.B	6.B	6.C
7.C	7.A	7.A	7.B	7.B
8.B	8.B	8.A	8.B	8.A
9.D	9.C	9.A	9.C	9.C
10.D	10.C	10.B	10.C	10.B
11.B	11.A	11.A	11.A	11.B
12.D	12.C	12.B	12.A	12.B
13.B	13.A	13.A	13.B	13.D
14.D	14.C	14.B	14.B	14.B
15.B	15.B	15.C	15.A	15.B
16.D	16.D	16.B	16.B	16.C
17.B	17.B	17.B	17.A	17.B
18.A	18.D	18.B	18.C	18.B
19.C	19.B	19.A	19.C	19.C
20.A	20.D	20.C	20.B	20.B