Indian Institute of Technology Bombay
Department of Electrical Engineering
EE-224: Digital Design

Assignment 2

Submission Deadline: April 19 (Friday)

Description of design:

Design a signed 8-bit (8 bit inputs and 16-bit output) quarter precision floating multiplier. Use Structural VHDL for the design. You are also required to write testbench to verify your design.

Representation of numbers in quarter precision floating point format

S: 1 bit sign bit

E: 3 bit exponent

F: 4 bit significant (fraction)

Format: sign exponent significant [SEF]