

## Indian Institute of Technology Bombay Department of Electrical Engineering

EE-224: Dígital Design

## **Assignment 1:**

Submission Deadline: April 15 (Monday)

Description of design:

Design a signed 8-bit (8 bit inputs and 16-bit output) booth encoded multiplier. Use Structural VHDL for the design. You are also required to write test bench to verify your design.