Charitha Pieris
BSCP|CS|62|114

Computer Systems

Week 3 Assessment Tasks
SIT111 - Task 3.3D

This is a piece of HDL (Hardware Description Language) code for a chip ALU (Arithmetic Logic Unit), which operates on two 16-bit inputs, x and y, to execute mathematical and logical operations. The following control signals can be used to modify the inputs:

- zx: if 1, the x input is set to zero
- nx: if 1, the x input is negated
- zy: if 1, the y input is set to zero
- ny: if 1, the y input is negated
- f: if 1, the output is the sum of x and y; if 0, the output is the bitwise AND of x and y
- no: if 1, the output is negated

A 16-bit result, a flag indicating whether the result is zero (zr), and a flag indicating if the result is negative (ng) make up the chip's output.

A number of sub-components are used in the implementation of the chip, including the Mux16 (multiplexer), Not16 (16-bit NOT gate), Add16 (16-bit adder), And16 (16-bit AND gate), Or8Way (8-input OR gate), and And (AND gate with one input locked to a constant true value). The PARTS portion of the code explains how these supporting elements are linked together to create the ALU capability.