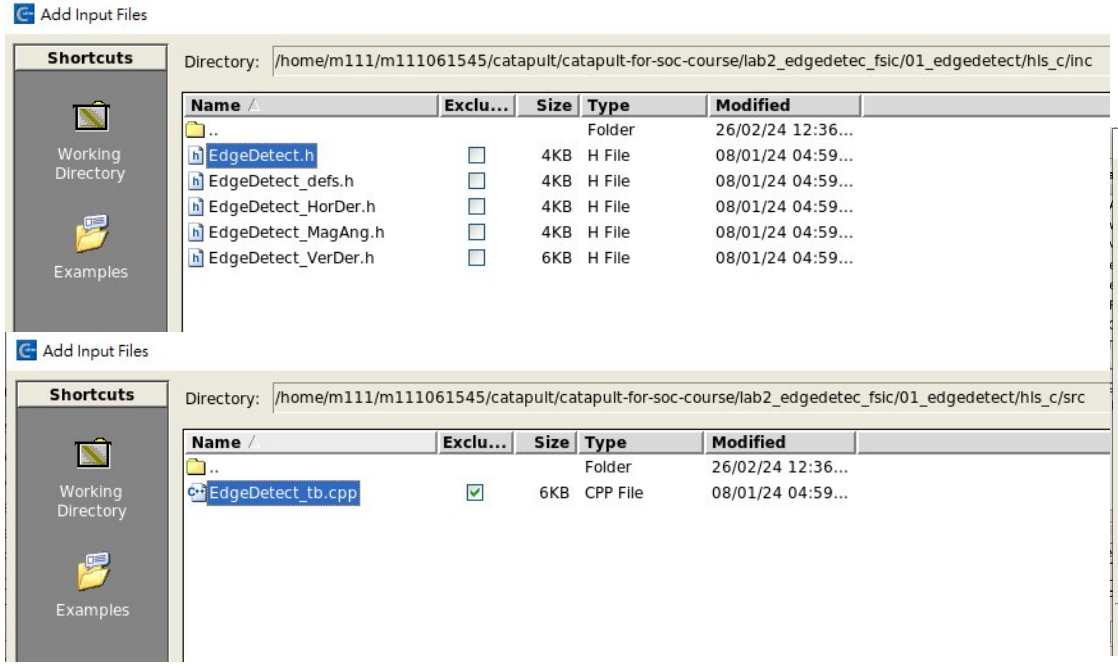
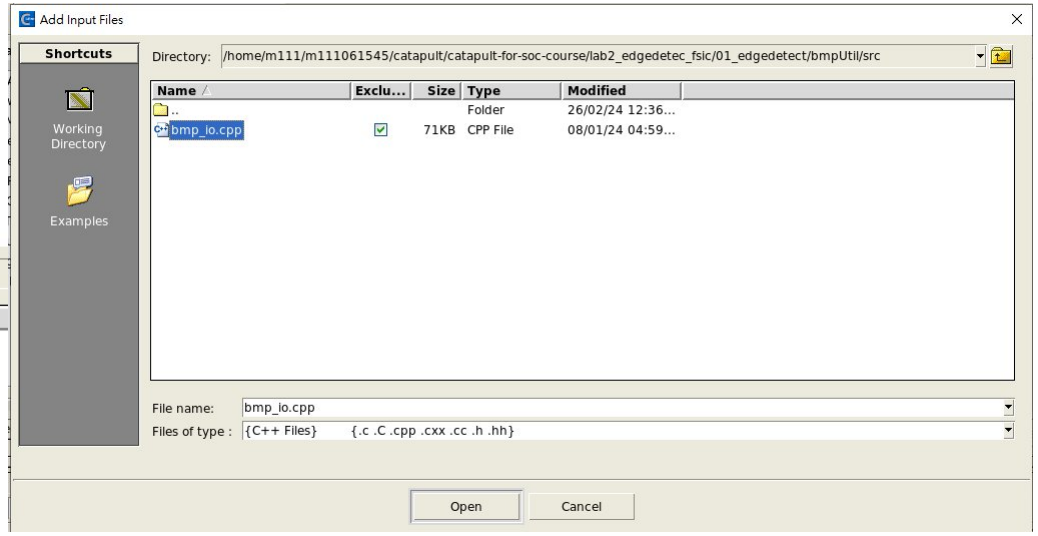
Catapult FPGA (Edge Detect) workflow

TA:陳揚哲

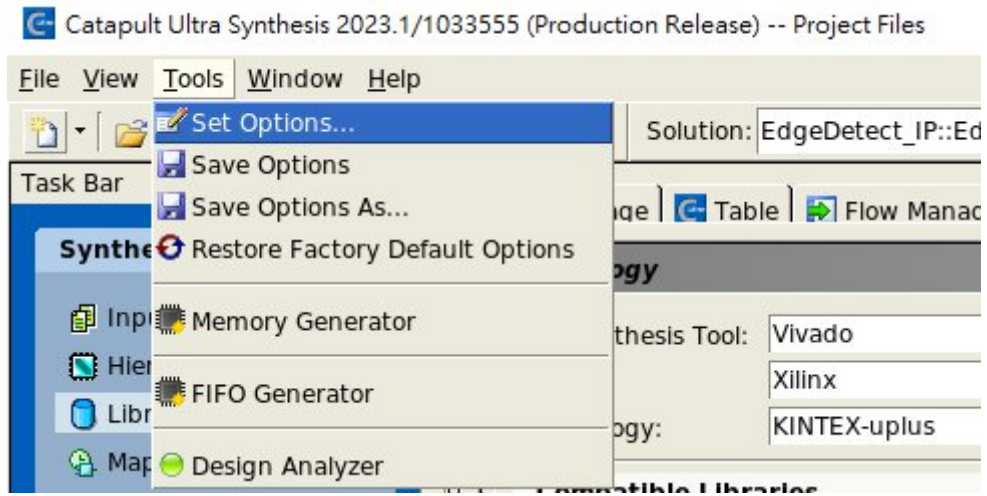
Add input file

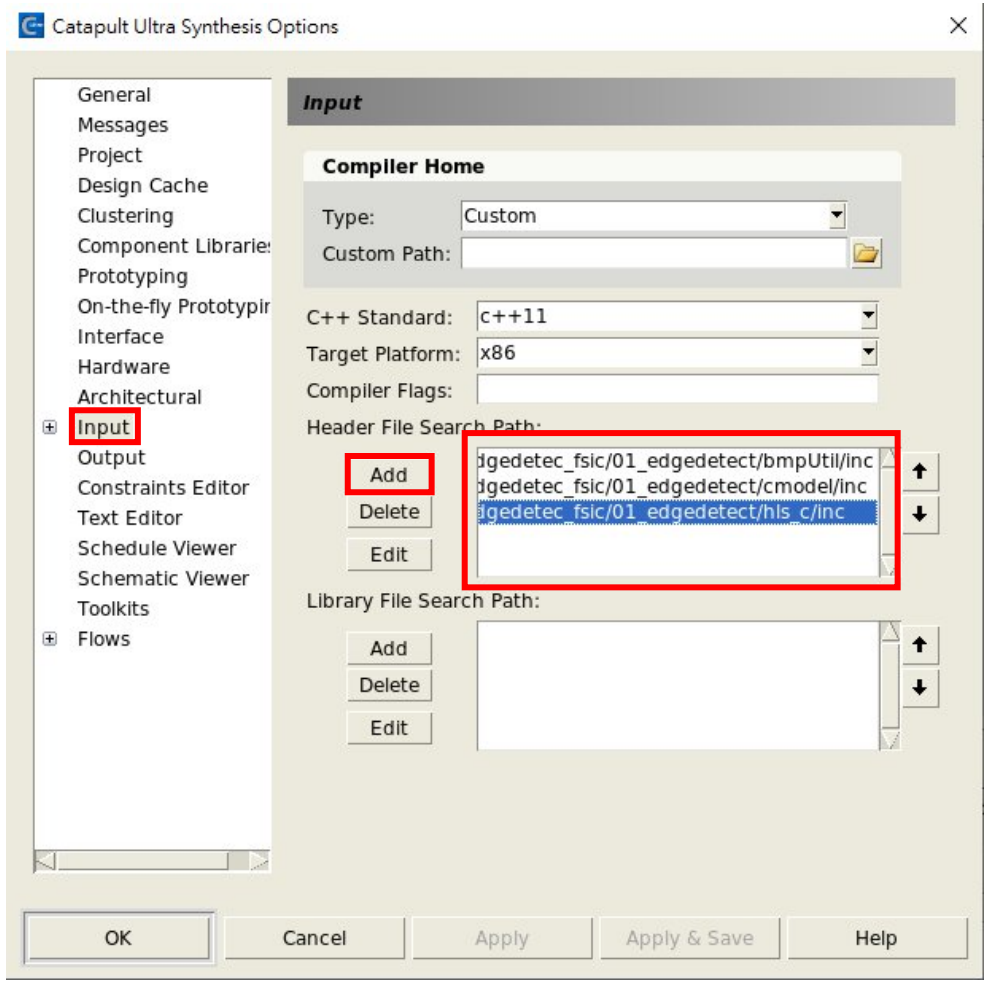
- Add EdgeDetect.h(hls_c/inc), EdgeDetect_tb.cpp(hls_c/src), and bmp_io.cpp(bmpUtil/src)
  - Note: these file should be set as excluded





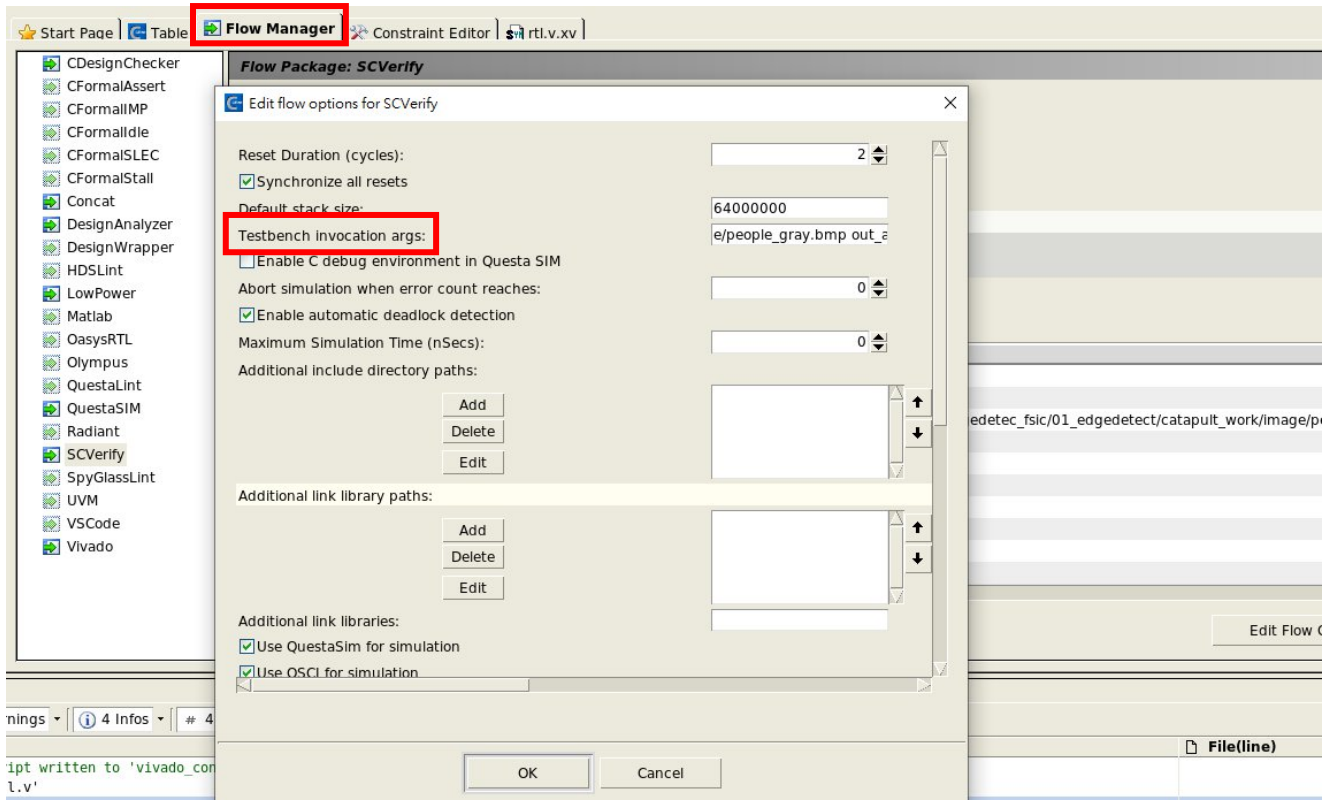
Add include path





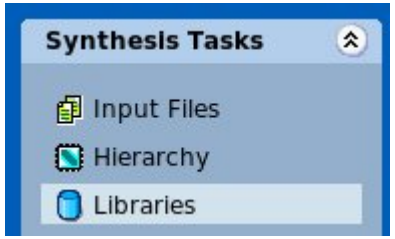
Add testbench invocation args

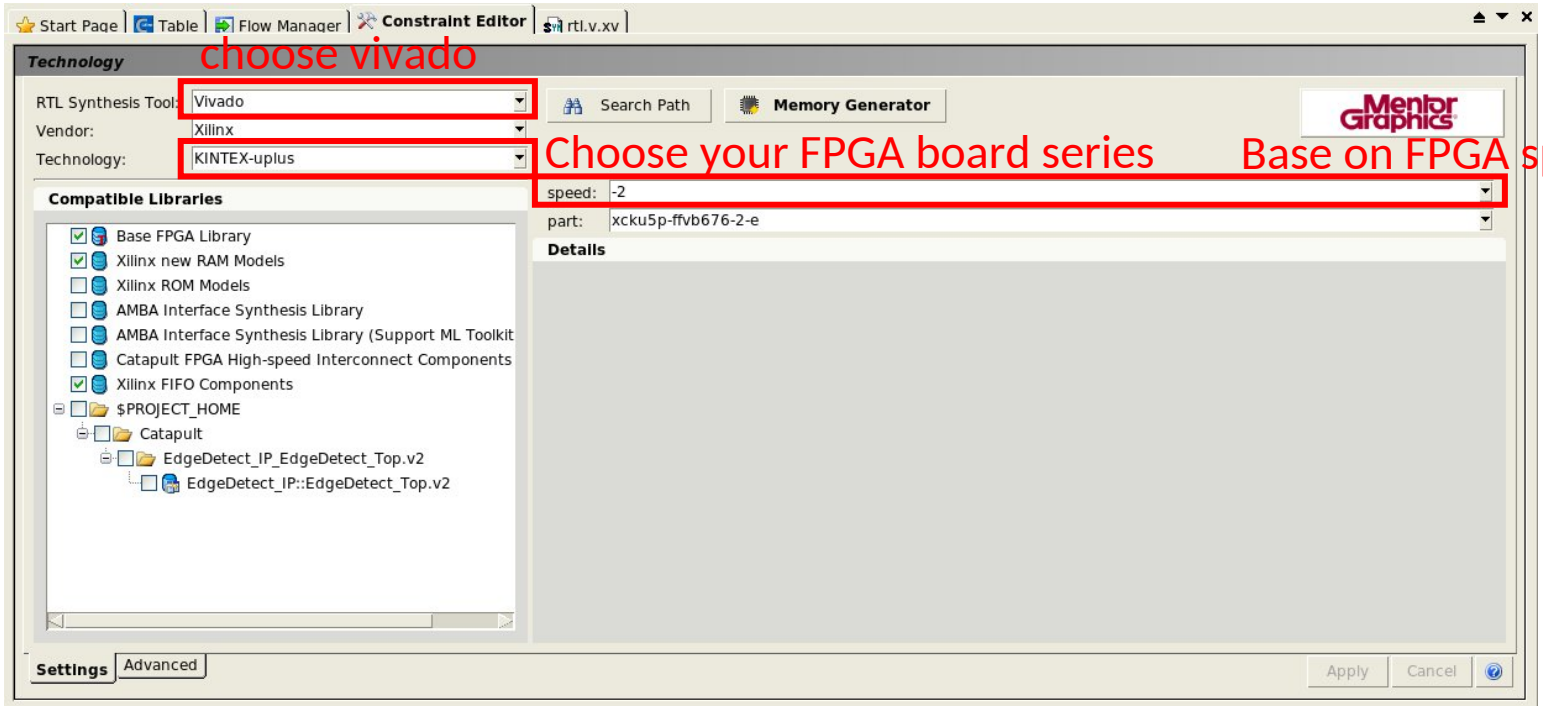
- **Add the directory (~/image/people_gray.bmp out_algorithm.bmp out_hw.bmp)**



Choose library (FPGA board)

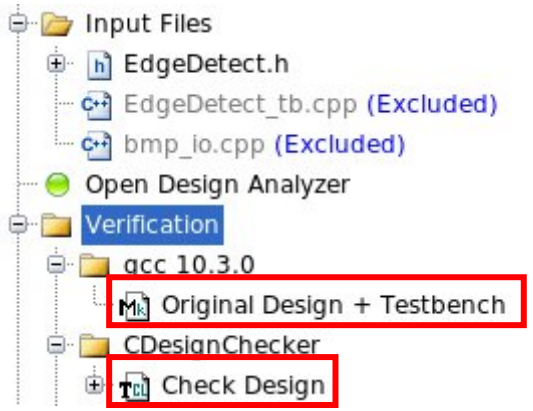
- You can choose your own FPGA board for catapult project
- Here I use KCU116 board for example
- Check Xilinx new RAM Model, Xilinx FIFO Components





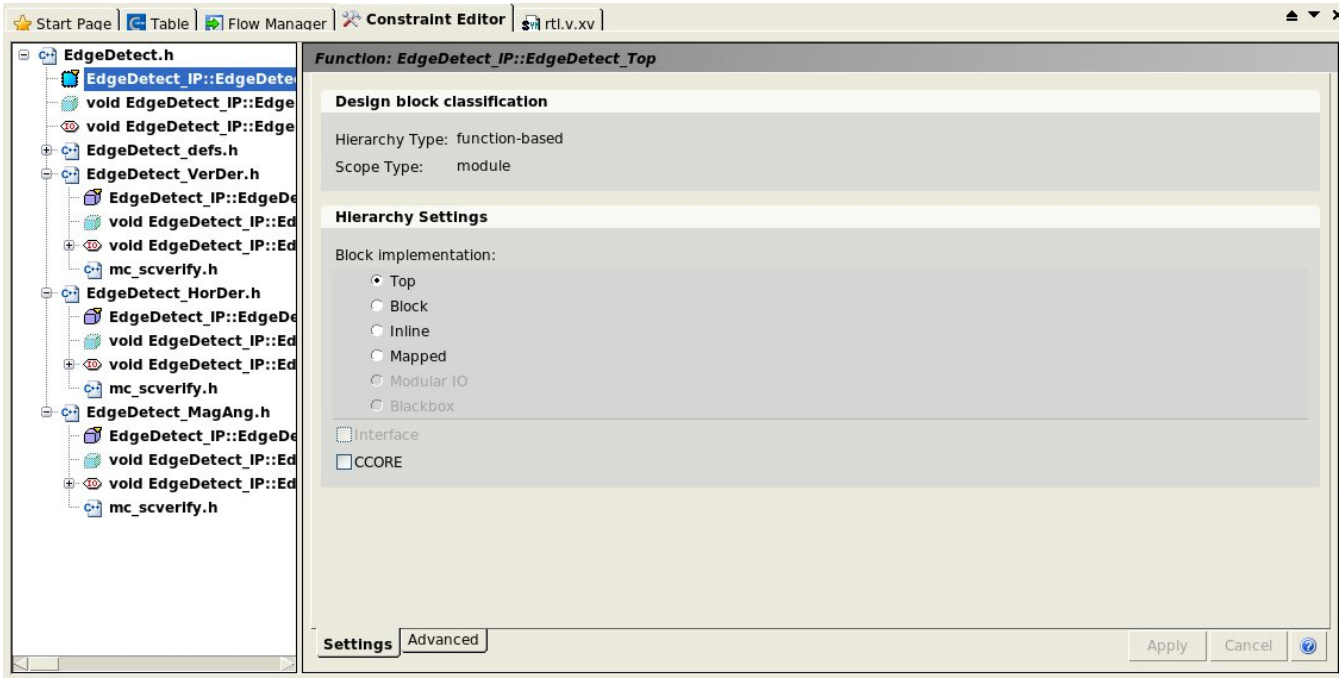
GCC and CDesignChecker

- Double click **Original Design + Testbench** and **Check Design**



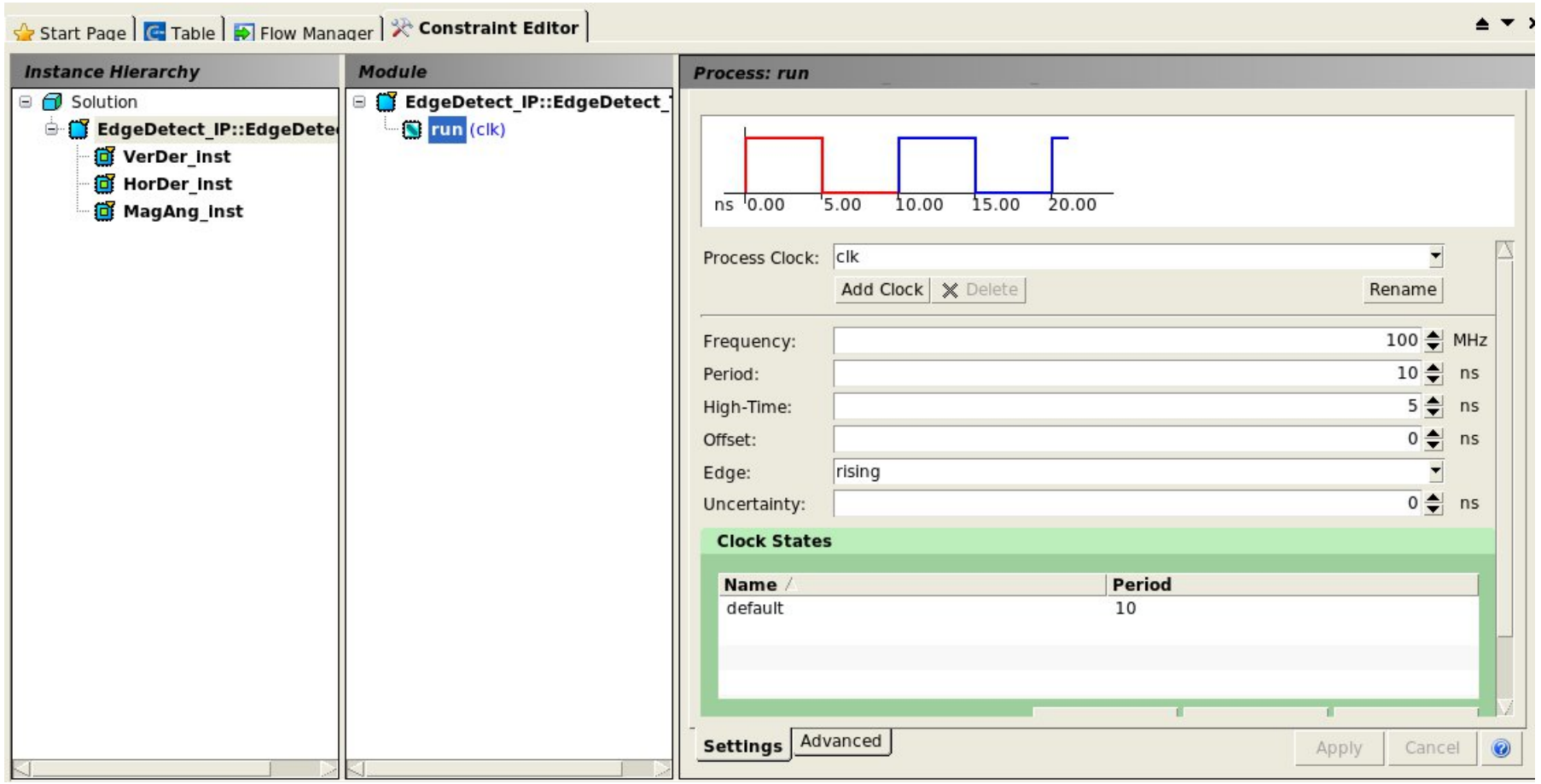
Top-down Process

- Here use Top-down process for example
  - Choose top module as top in block implementation
- Suggest bottom-up process. (Step_by_step_lab2_EdgeDetect.pdf)
  - ***_Ver -> *_Hor-> *_Mag -> *_Top**



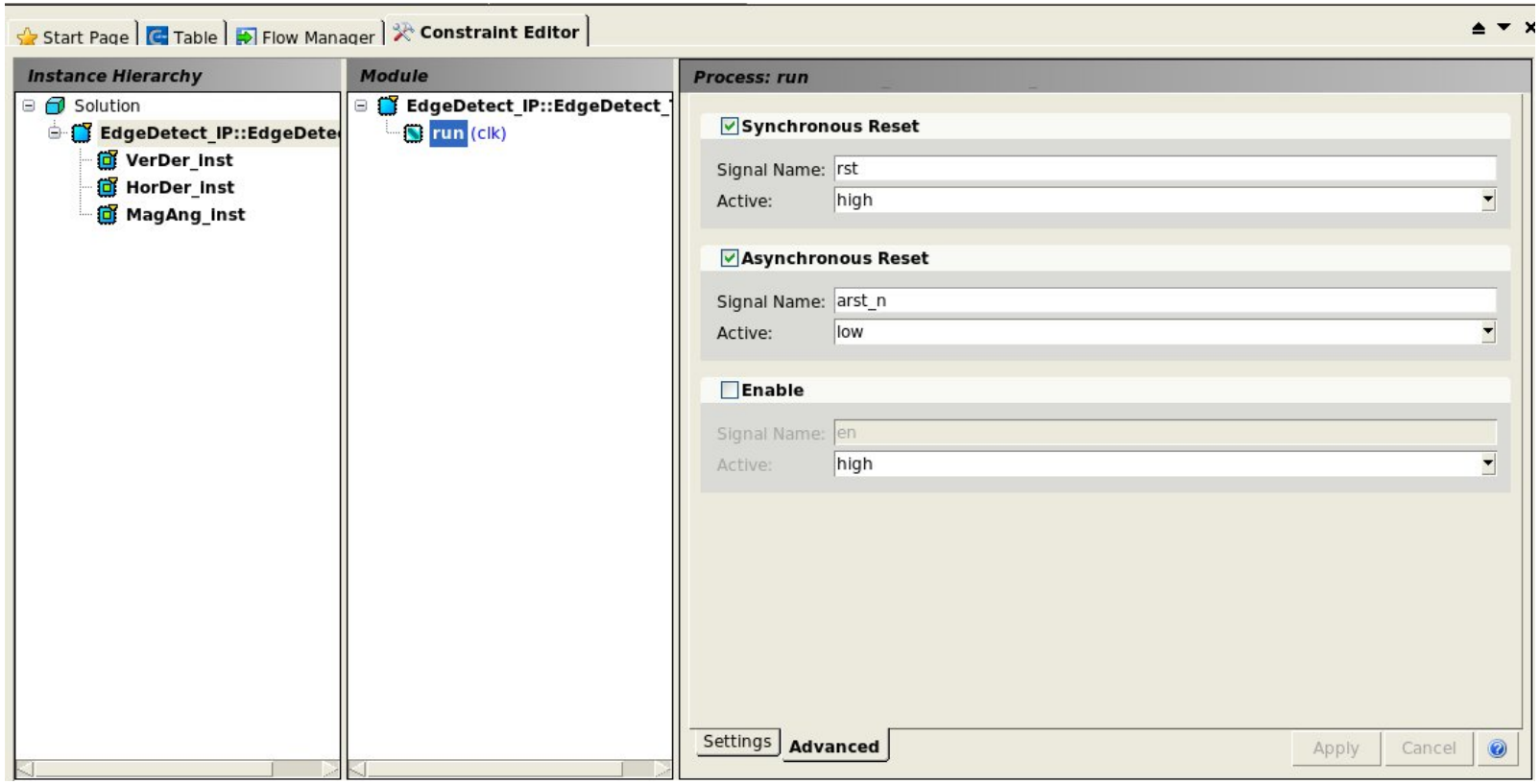
Mapping

- Set clock as 100 MHz

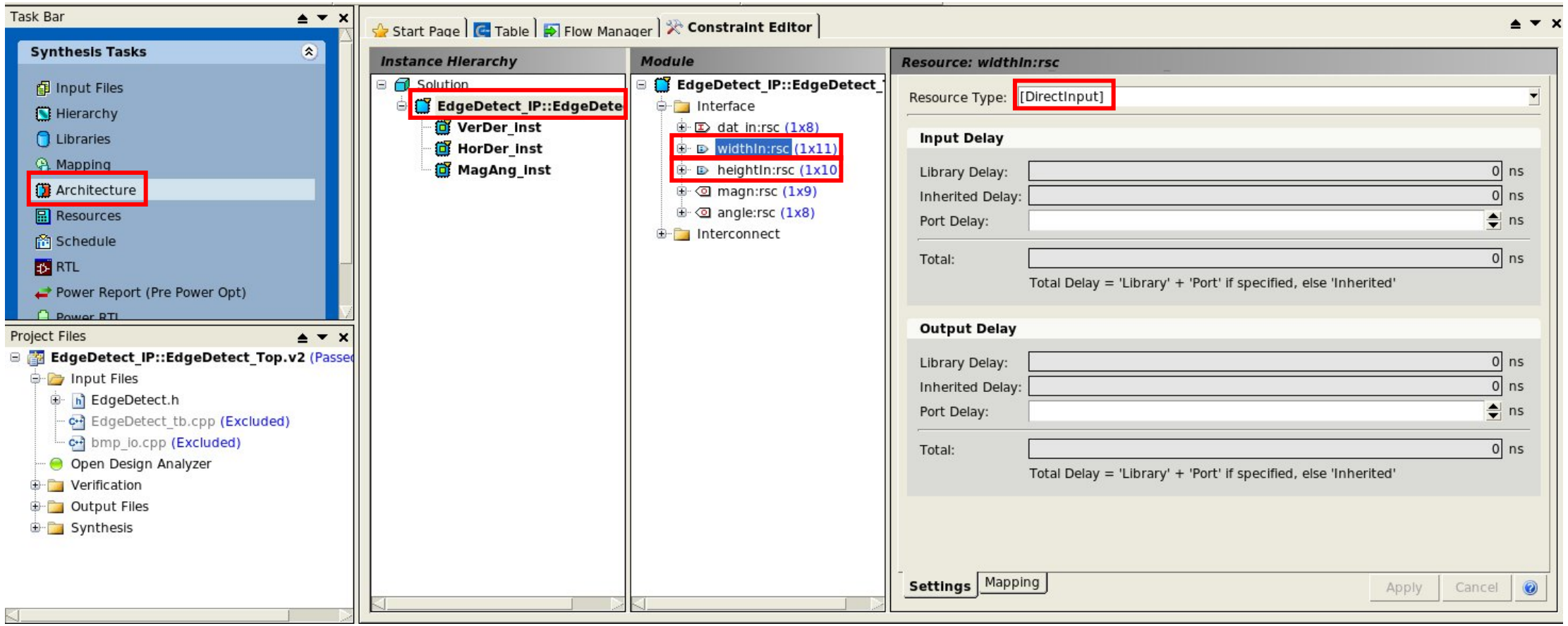


Mapping

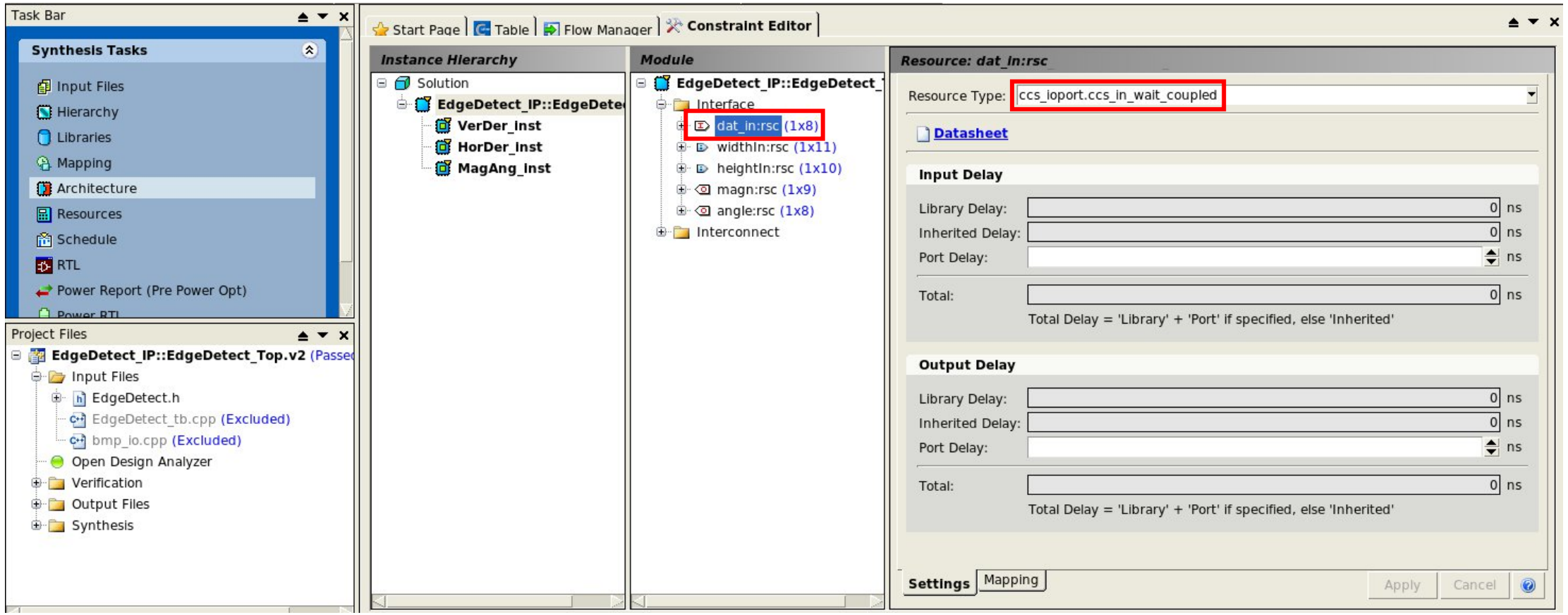
- Check Asynchronous Reset



Architecture

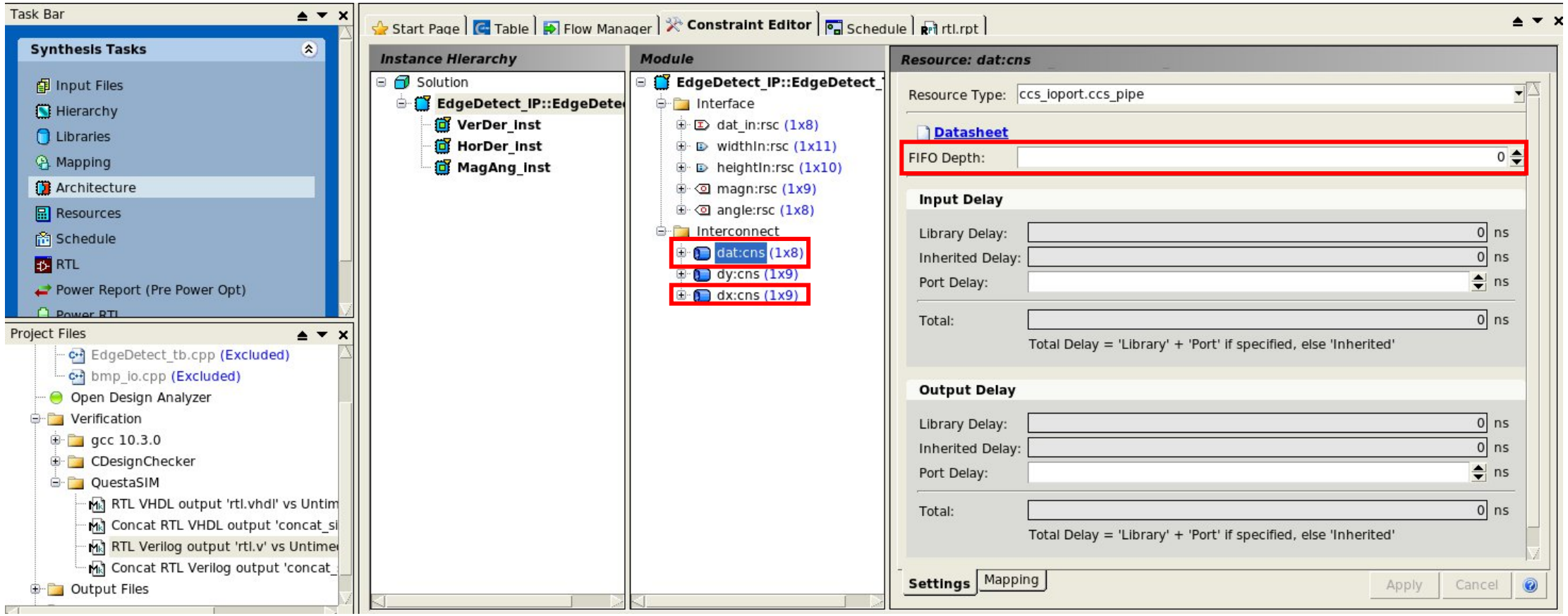


Architecture

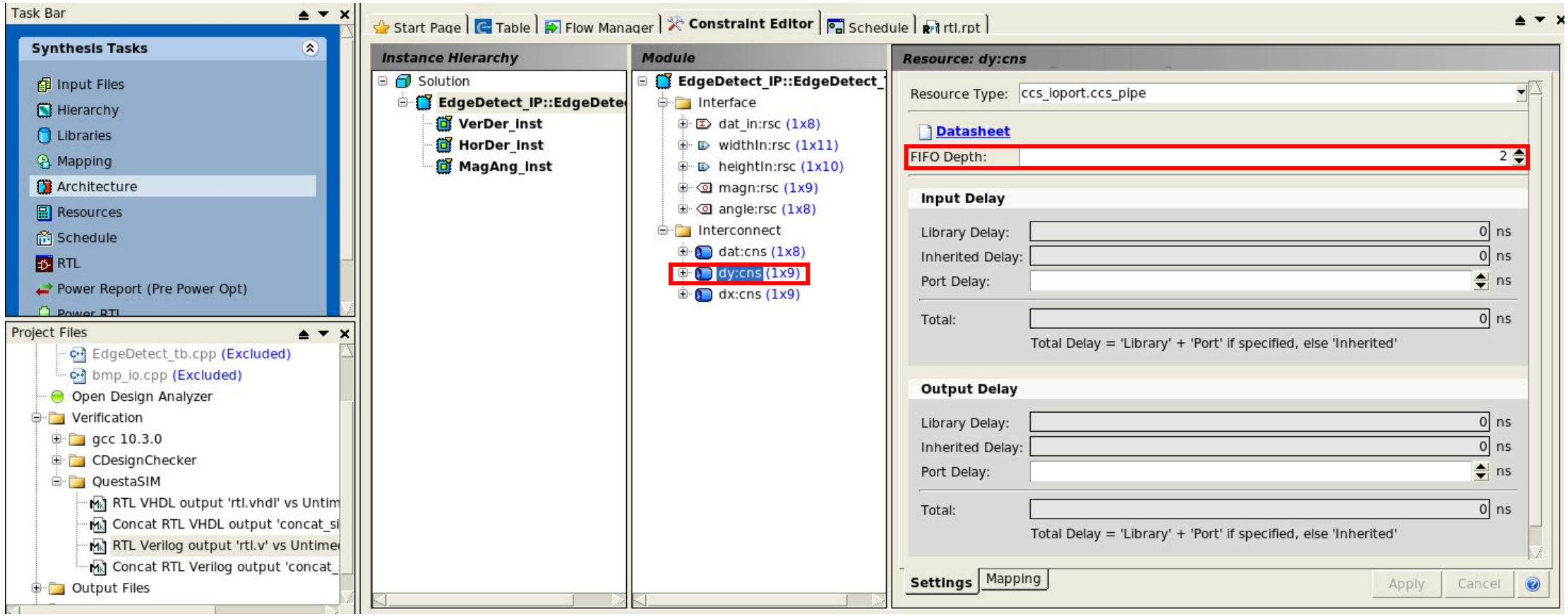


Architecture

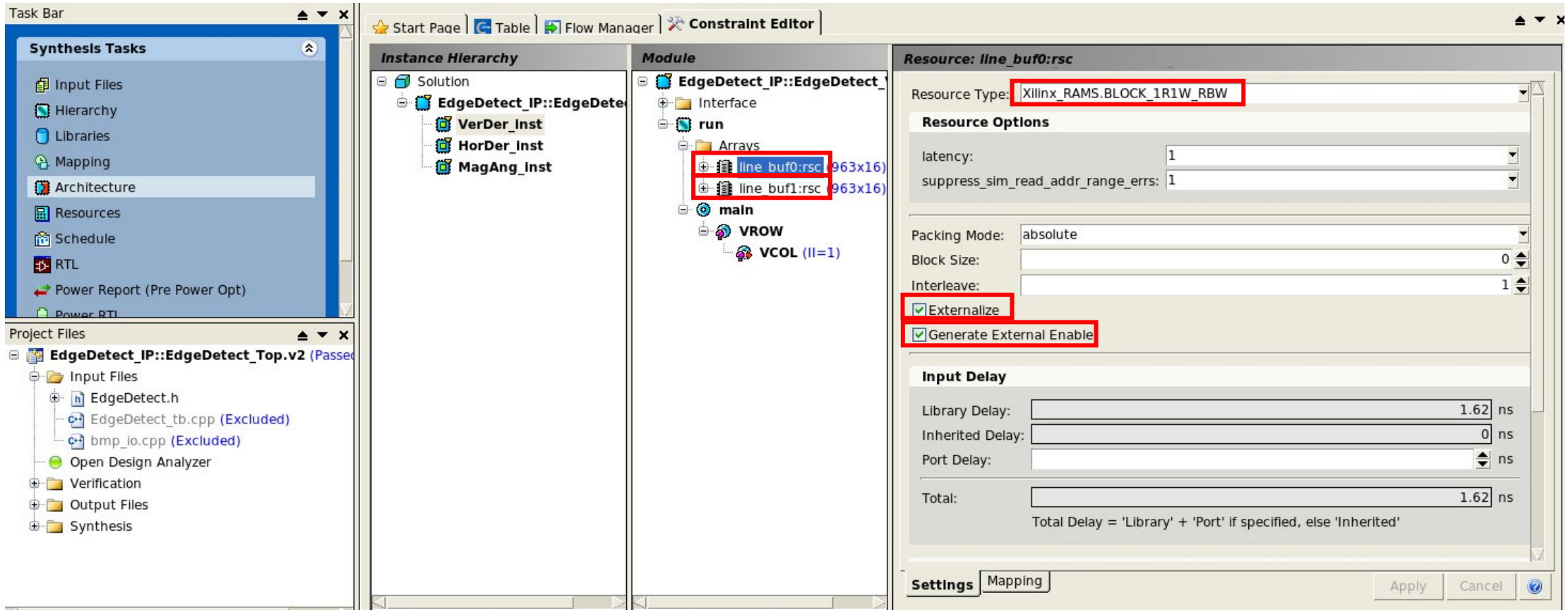
- Set FIFO depth base on your design delay(By bottom-up step)



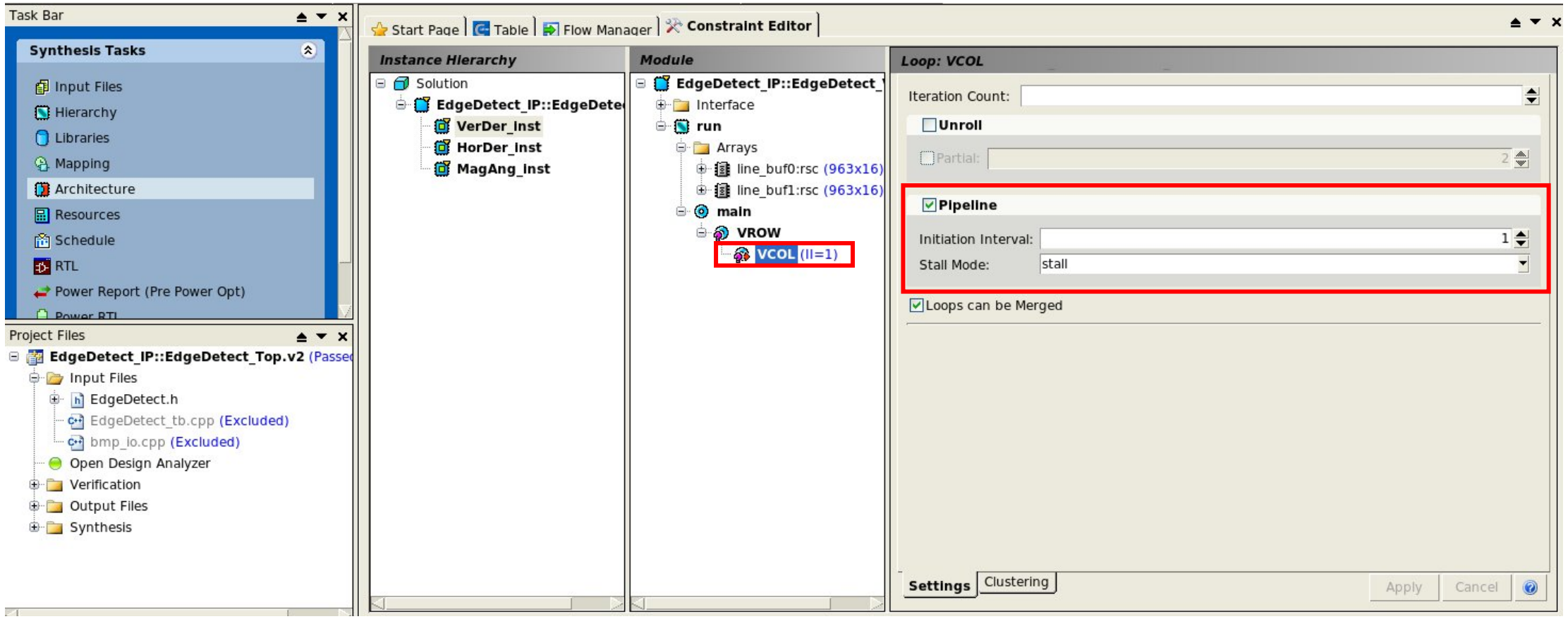
Architecture



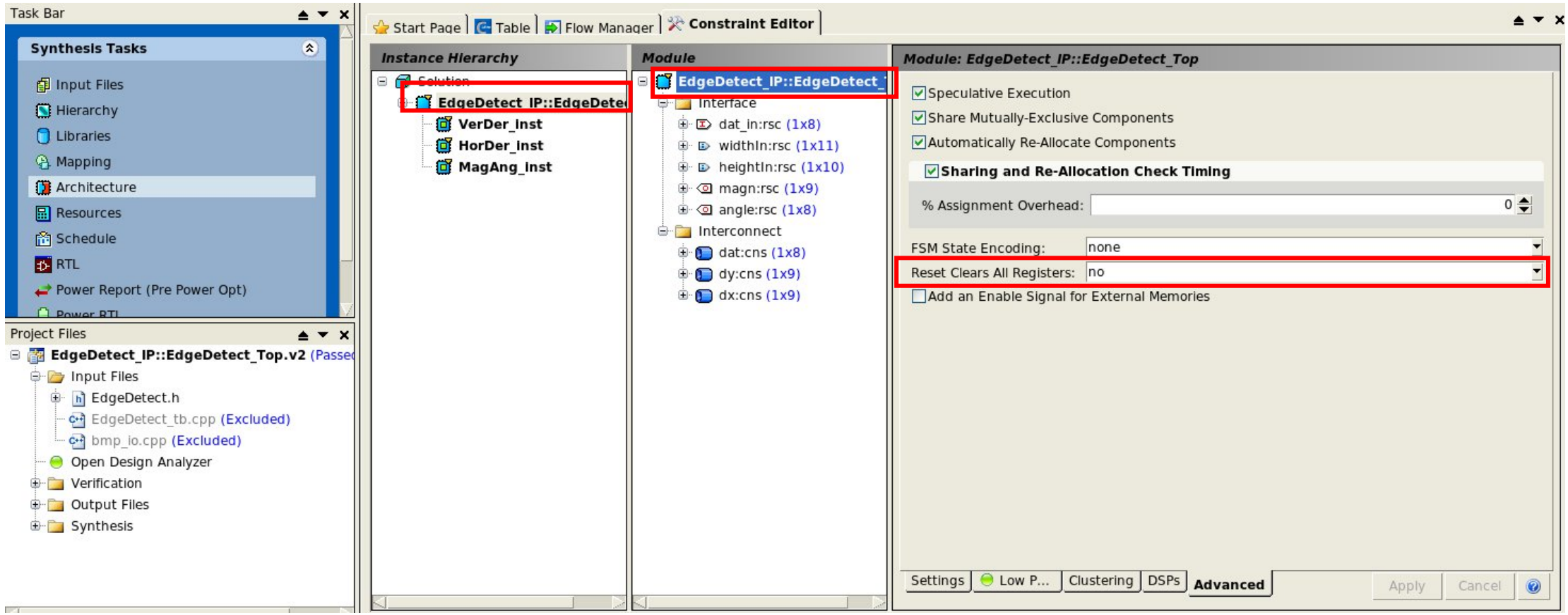
Architecture



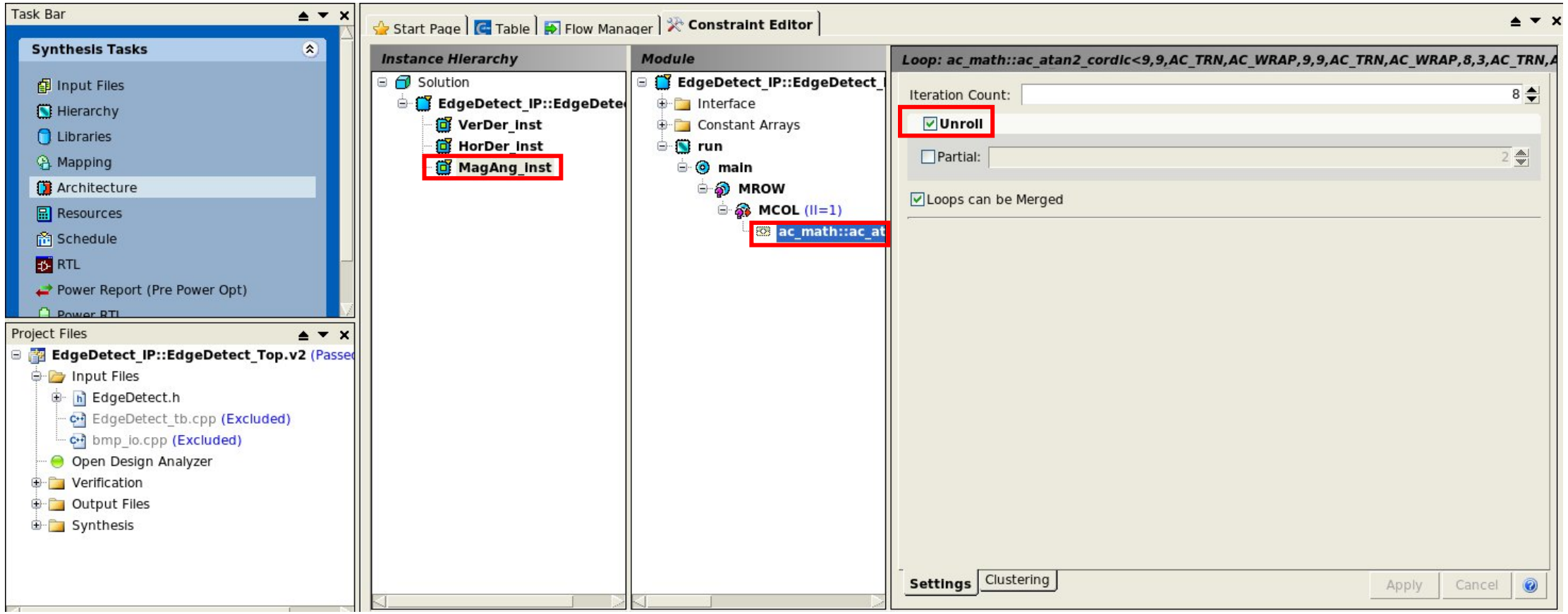
Architecture



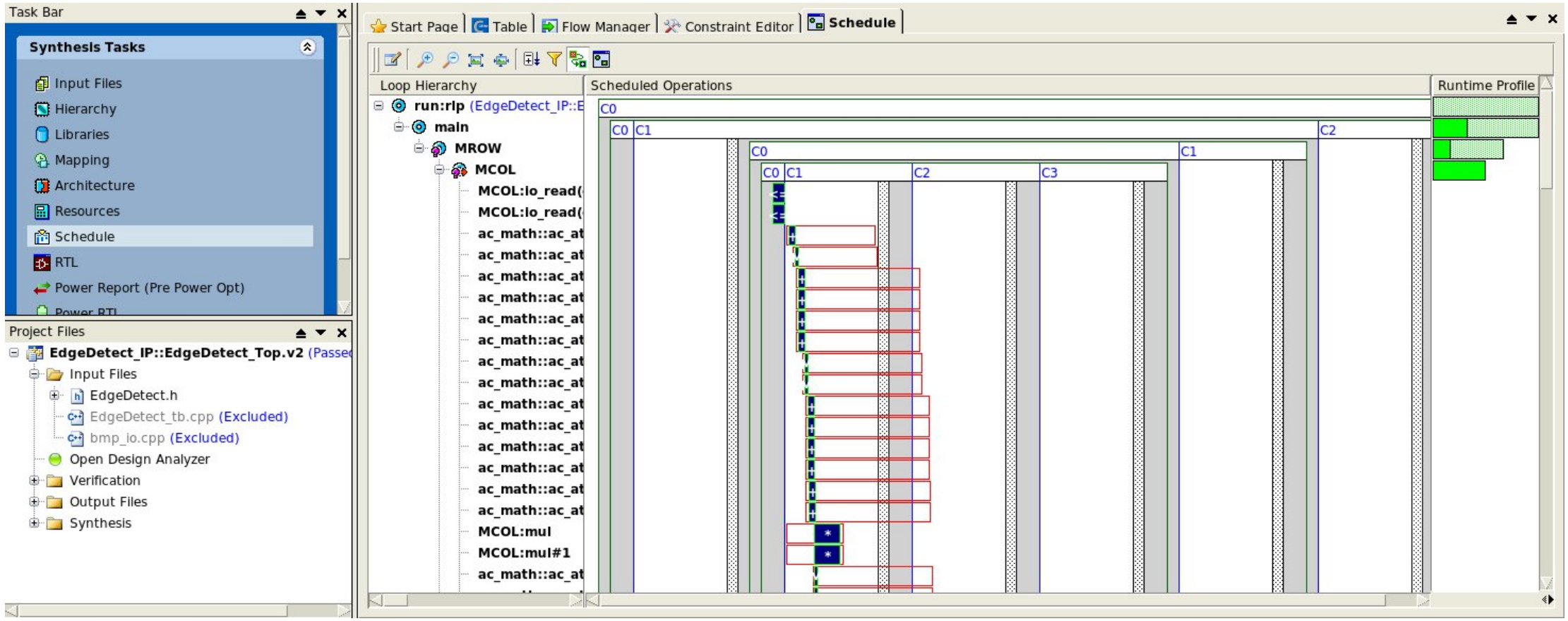
Architecture



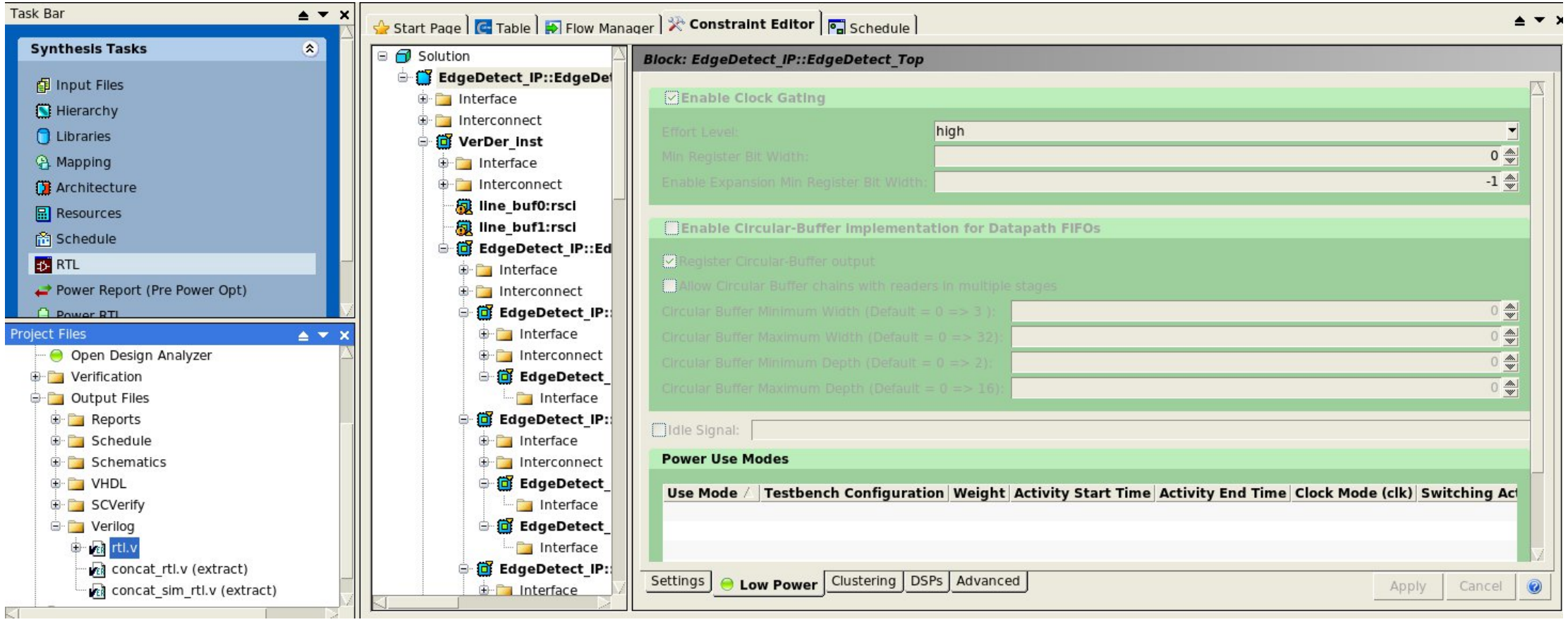
Architecture



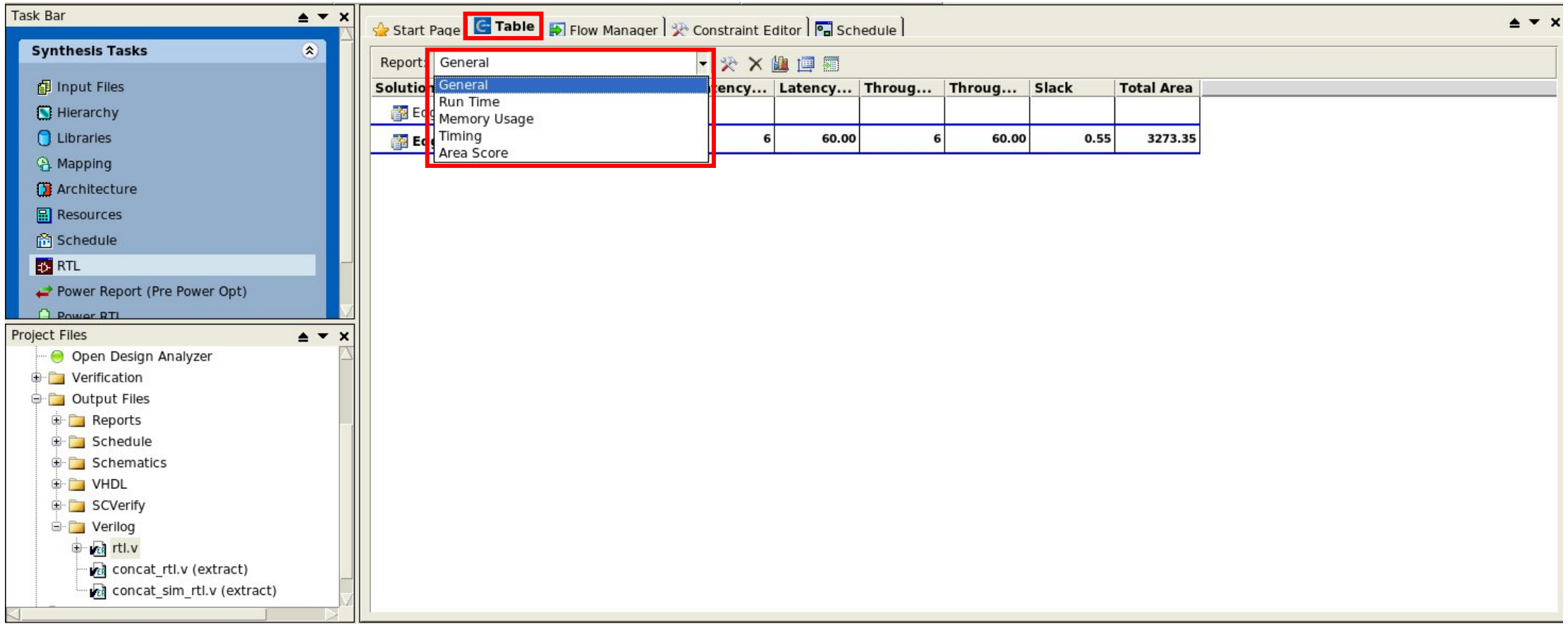
Schedule


Task Bar
Synthesis Tasks
Input Files
Hierarchy
Libraries
Mapping
Architecture
Resources
Schedule
RTL
Power Report (Pre Power Opt)
Project Files
EdgeDetect_IP::EdgeDetect_Top.v2 (Passe
Input Files
EdgeDetect.h
EdgeDetect_tb.cpp (Excluded)
bmp_io.cpp (Excluded)
Open Design Analyzer
Verification
Output Files
Synthesis
Start Page
Table
Flow Manager
Constraint Editor
Schedule
Loop Hierarchy
Scheduled Operations
Runtime Profile
run:rlp (EdgeDetect_IP::E
main
MROW
MCOL
MCOL:lo_read(
MCOL:lo_read(
ac_math::ac_at
MCOL:mul
MCOL:mul#1
C0
C1
C2
C3

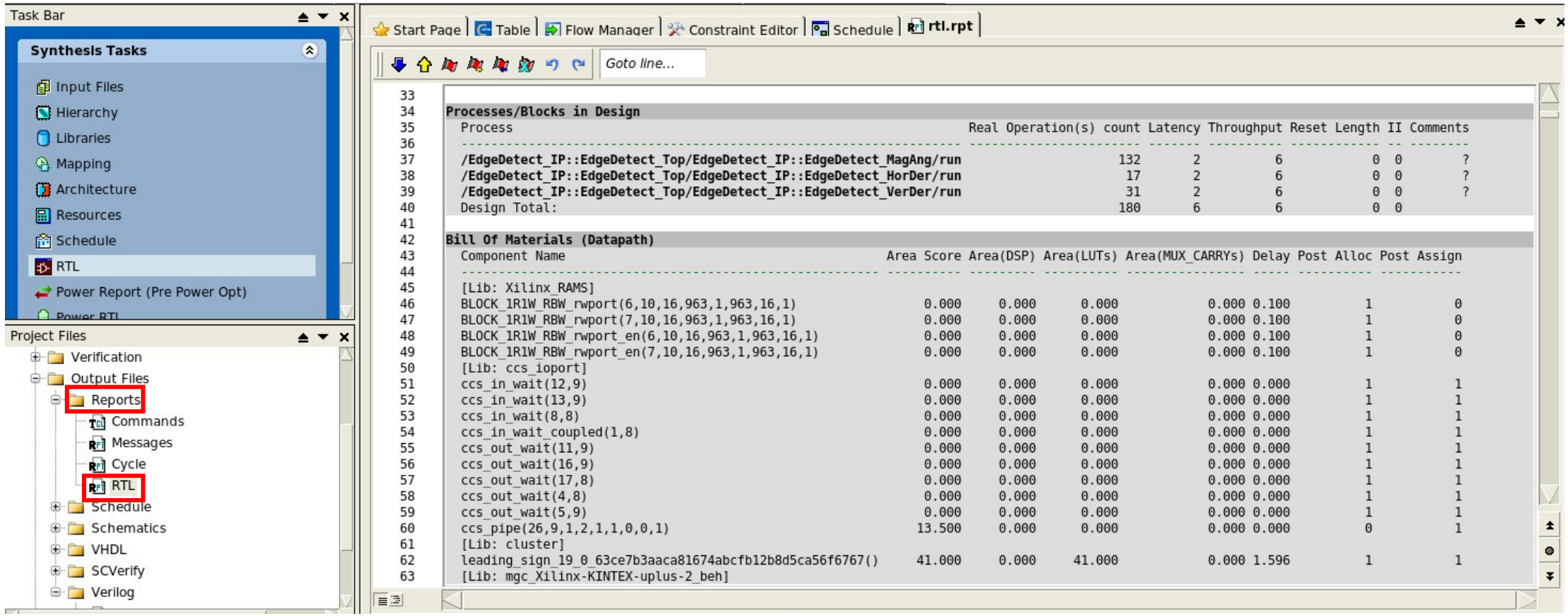
Generate RTL



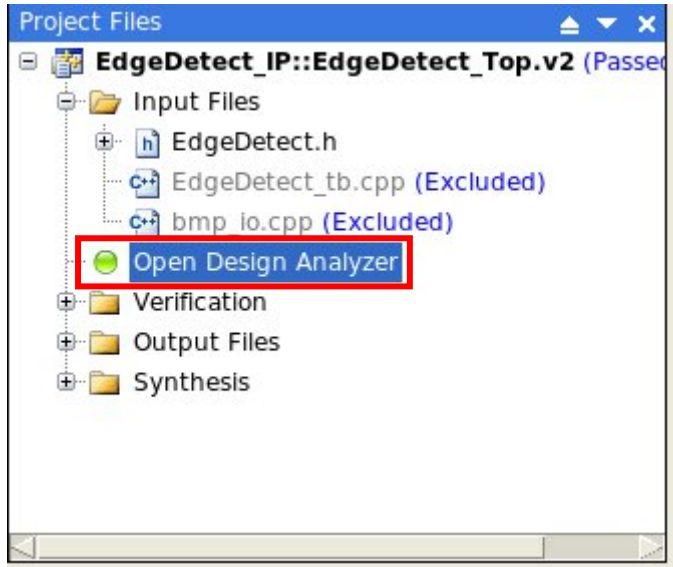
Synthesis report

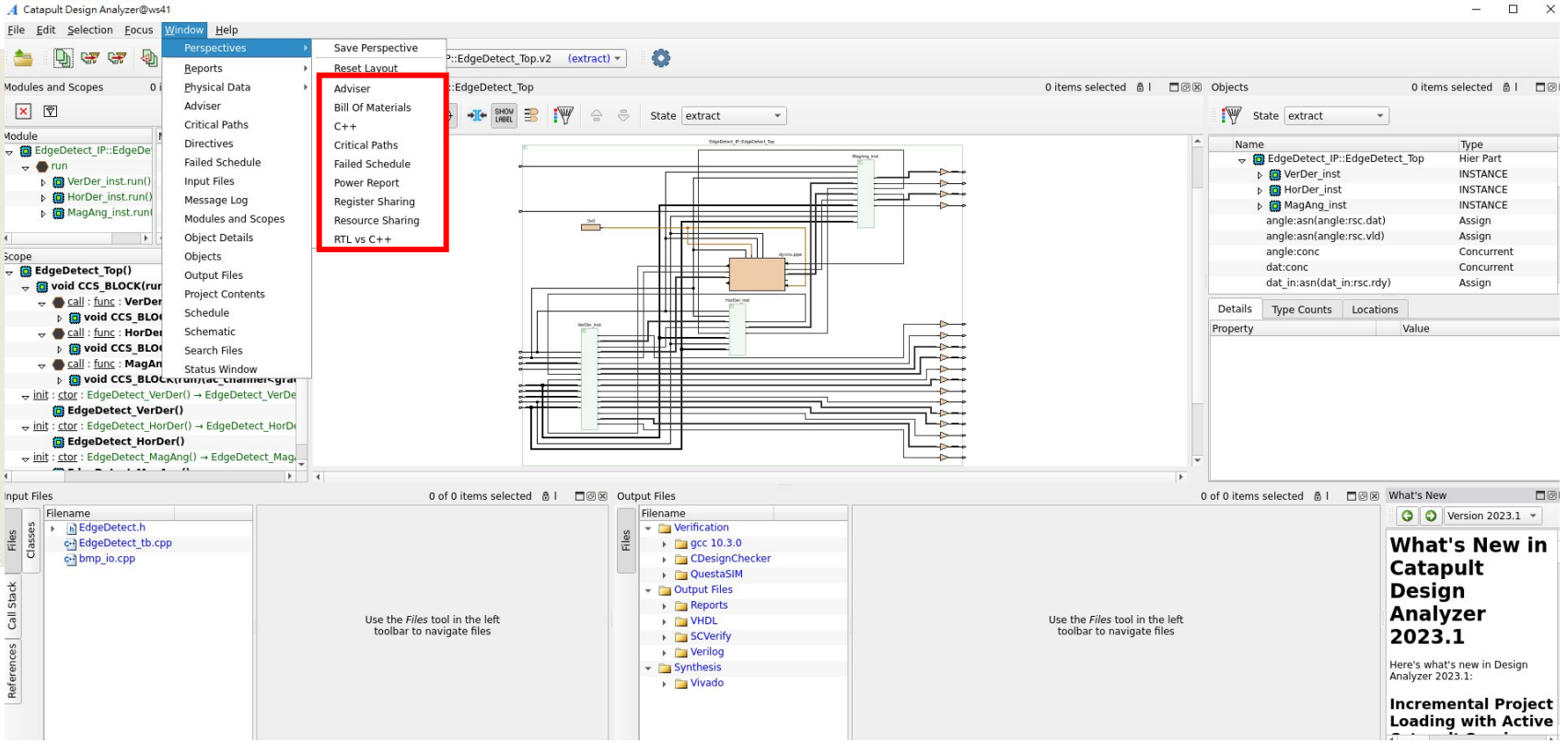


Synthesis report

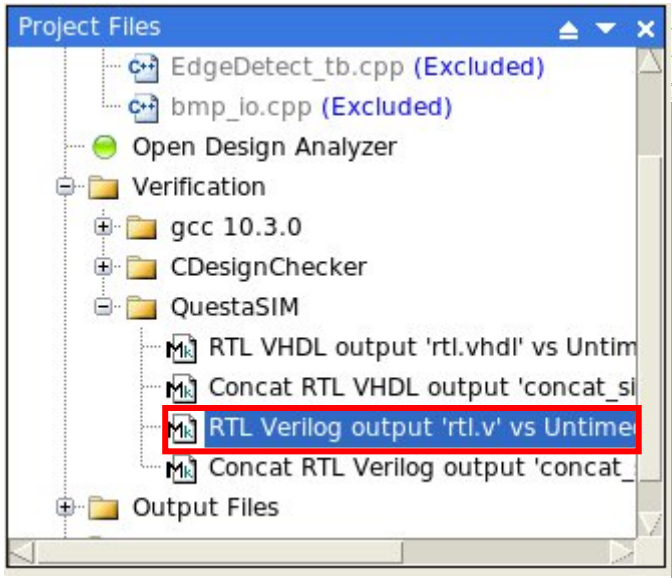


Design Analyzer

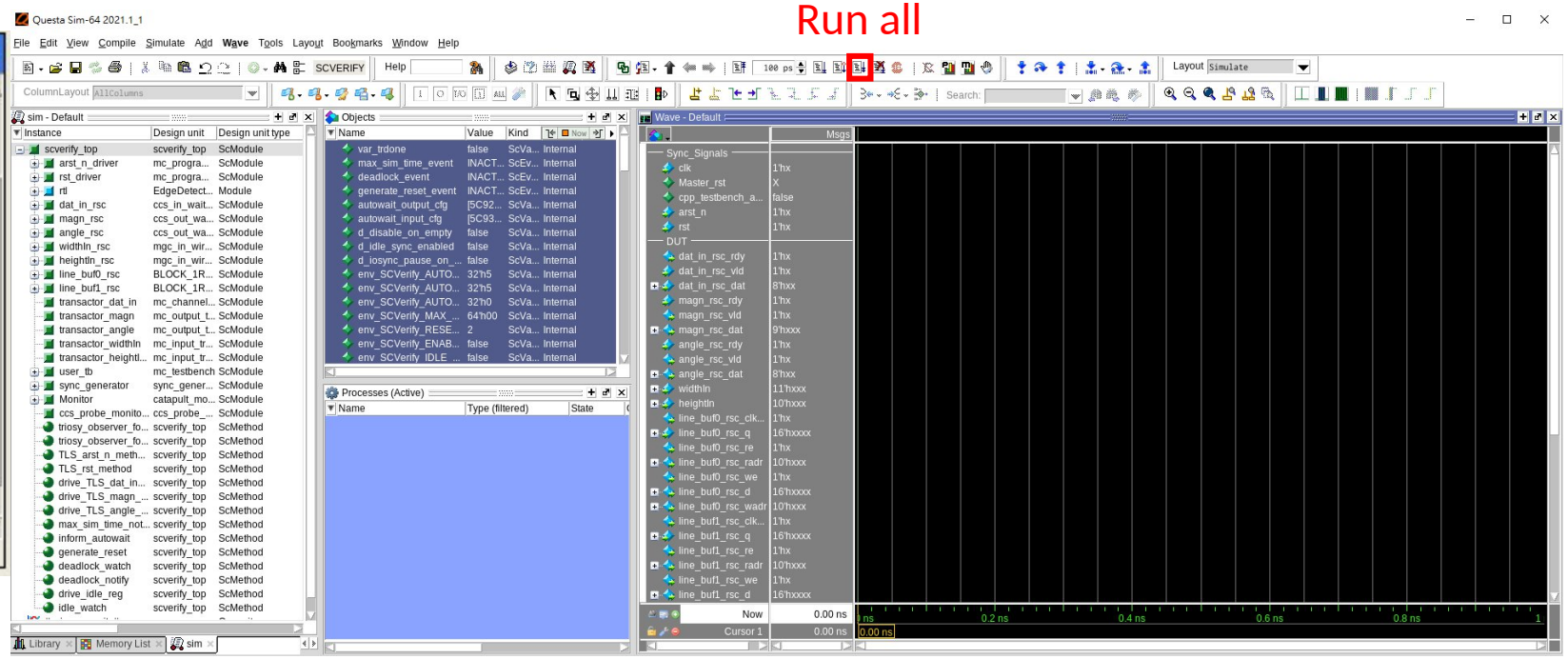




RTL Verification (Cont.)

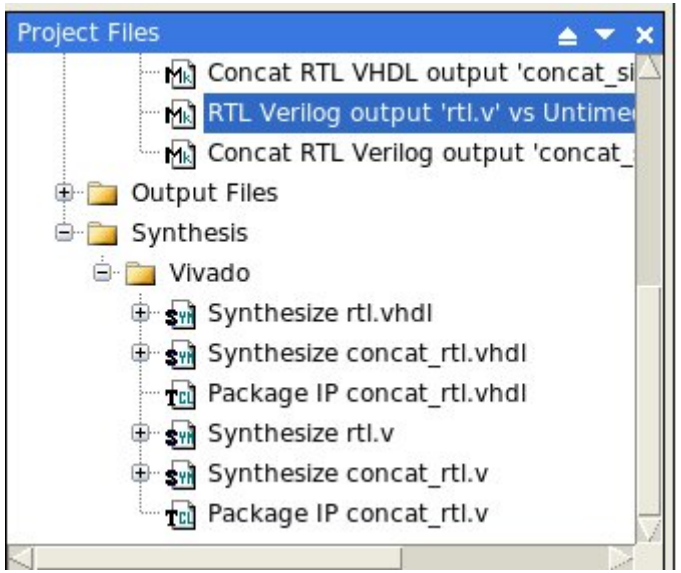


Run all



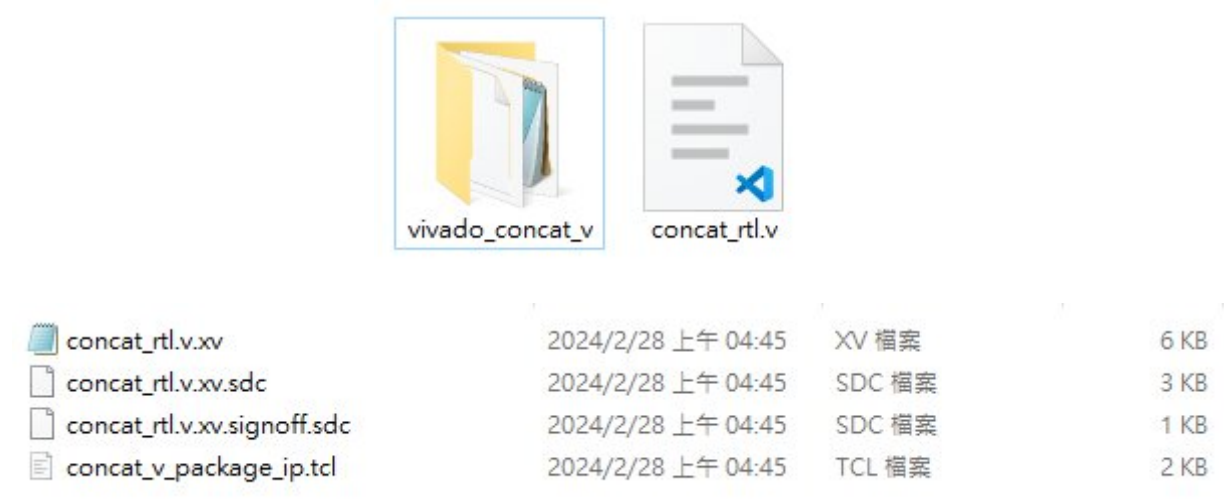
Synthesis workflow (Catapult GUI)

- If your environment have Vivado project, set up Vivado directory and double click Synthesize concat_rtl.v
- If not, follow the synthesis workflow



Synthesis workflow (Vivado)

- Download the file of concat_rtl.v and the folder of vivado_concat_v
- File under vivado_concat_v folder



Change all of the directory in xv file

```
## HLS SP synthesis script
## Generated for stage extract
## Vivado mode is Non-project

# Version check
set vv [version -short]
if { [regexp {(\d+)\.(\d+).*} $vv all major minor] } {
  if { ($major < 2020) || ($major == 2020 && $minor < 2) } {
    puts "Vivado version (v${vv}) is not compatible with version used for the Catapult library (v2020.2)."
  }
}
# Reporting settings
puts "-- Requested 4 fractional digits for design 'EdgeDetect_IP_EdgeDetect_Top' timing"
puts "-- Requested 4 fractional digits for design 'EdgeDetect_IP_EdgeDetect_Top' capacitance"
puts "-- Characterization mode: p2p "

puts "-- Synthesis Timing report: '/home/ubuntu/catapult_test/vivado_concat_v/timing_summary_synth.rpt' "
puts "-- Synthesis Utilization report: '/home/ubuntu/catapult_test/vivado_concat_v/utilization_synth.rpt' "
if { ([info exists env(Xilinx_RUN_PNR)] && $env(Xilinx_RUN_PNR) ) ||
     ([info exists env(Xilinx_BITGEN)] && $env(Xilinx_BITGEN) ) } {
puts "-- Routed Timing report: '/home/ubuntu/catapult_test/vivado_concat_v/timing_summary_routed.rpt' "
puts "-- Routed Utilization report: '/home/ubuntu/catapult_test/vivado_concat_v/utilization_placed.rpt' "
}

```

Change all of the directory in xv file

```
25 # Environment variable settings
26 global env
27 ## set CATAPULT_HOME "/usr/cadtool/mentor/Catapult/2023.1/Mgc_home"
28 ## Set the variable for file path prefixing
29 set RTL_TOOL_SCRIPT_DIR /home/ubuntu/catapult_test/vivado_concat_v
30 set RTL_TOOL_SCRIPT_DIR [file dirname [file normalize [info script] ] ]
31 puts "-- RTL_TOOL_SCRIPT_DIR is set to '$RTL_TOOL_SCRIPT_DIR' "
32 # Vivado Non-Project mode script starts here
33 puts "============================================"
34 puts "Catapult driving Vivado in Non-Project mode"
35 puts "============================================"
36 set outputDir /home/ubuntu/catapult_test/vivado_concat_v
37 set outputDir $RTL_TOOL_SCRIPT_DIR
38 #file mkdir $outputDir
39 #
40 # STEP#1: setup design sources and constraints
41 #
42 create_project -force tcl_concat_v
43    read_verilog /home/ubuntu/catapult_test/concat_rtl.v
44 # set up XPM libraries for XPM-related IP like the Catapult Xilinx_FIFO
45 set_property XPM_LIBRARIES {XPM_CDC XPM_MEMORY XPM_FIFO} [current_project]
46 read_xdc /home/ubuntu/catapult_test/vivado_concat_v/concat_rtl.v.xv.sdc
47 set_property part xcku5p-ffvb676-2-e [current_project]
48 #
49 # STEP#2: run synthesis, report utilization and timing estimates, write checkpoint design
50 #
51 synth_design   -cascade_dsp auto  -top EdgeDetect_IP_EdgeDetect_Top -part xcku5p-ffvb676-2-e -mode out_of_context  -include_dirs ""
52 write_checkpoint -force $outputDir/post_synth
53 set viv_report_dir /home/ubuntu/catapult_test/vivado_concat_v
54 report_utilization -file $viv_report_dir/utilization_synth.rpt
55 report_timing_summary -path_type summary -file $viv_report_dir/timing_summary_synth.rpt
56 report_timing -nworst 1 -from [all_inputs] -to [all_outputs] -file $viv_report_dir/timing_summary_synth.rpt -append
57 if { [llength [all_clocks] ] > 0 } {
58    report_timing -nworst 1 -from [all_inputs] -to [all_clocks] -file $viv_report_dir/timing_summary_synth.rpt -append
59    report_timing -nworst 1 -from [all_clocks] -to [all_clocks] -file $viv_report_dir/timing_summary_synth.rpt -append
60    report_timing -nworst 1 -from [all_clocks] -to [all_outputs] -file $viv_report_dir/timing_summary_synth.rpt -append
61 }
```

Synthesis by GUI

- Open Vivado
- Create a project with any board
- Execute xv file, (or the command in xv file), in tcl console
- It will generate the design of the board you choose in catapult

Synthesis by Command Shell (Linux)

- Create file named run_vivado.
- Specify the directory of xv file and source it by vivado command.
- Then execute run_vivado.


```
echo "start vivado project"


# ----- remove vivado project log files -----#
rm -rf ./NA
rm -rf ./.Xil
rm -f timing_report.log
rm -f vivado*.jou
rm -f vivado*.log


# ----- Re-build vivado project -----#

vivado -source concat_rtl.v.xv -mode tcl
```

```
ubuntu@ubuntu2004: ~/catapult_test/vivado_concat_v
mount: /home/ubuntu/tools: /dev/sdb1 already mounted on /home/ubuntu/tools.
mount: /tools: /dev/sdb1 already mounted on /home/ubuntu/tools.
ubuntu@ubuntu2004:~/catapult_test/vivado_concat_v$ ./run_vivado
start vivado project

****** Vivado v2022.1 (64-bit)
  **** SW Build 3526262 on Mon Apr 18 15:47:01 MDT 2022
  **** IP Build 3524634 on Mon Apr 18 20:55:01 MDT 2022
    ** Copyright 1986-2022 Xilinx, Inc. All Rights Reserved.
```

For implement and bitstream (opt.)

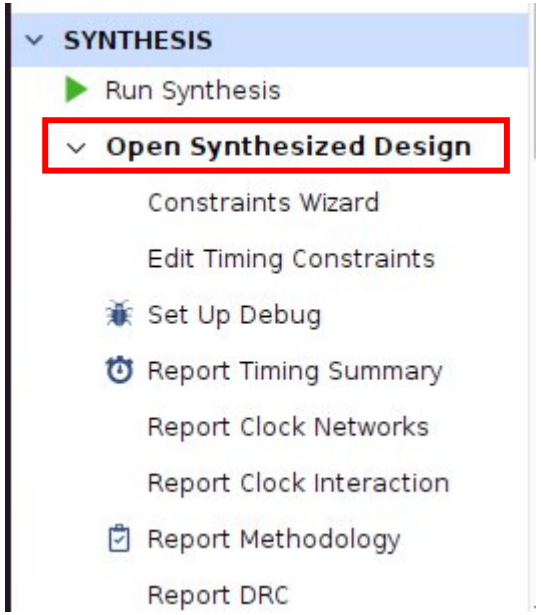
- For implement and generate bitstream, you need specify the constraints.
- You can specify the constraints on your own, or assigned by vivado
- Note: If you change the design board, you need to make sure the timing is satisfied.

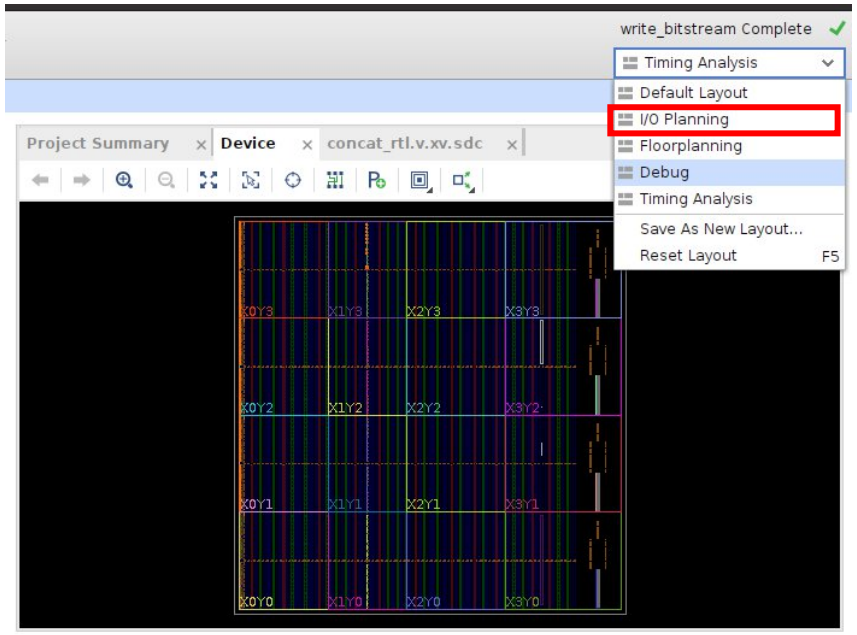
Set up constraints

- Set up the arst_n constraints

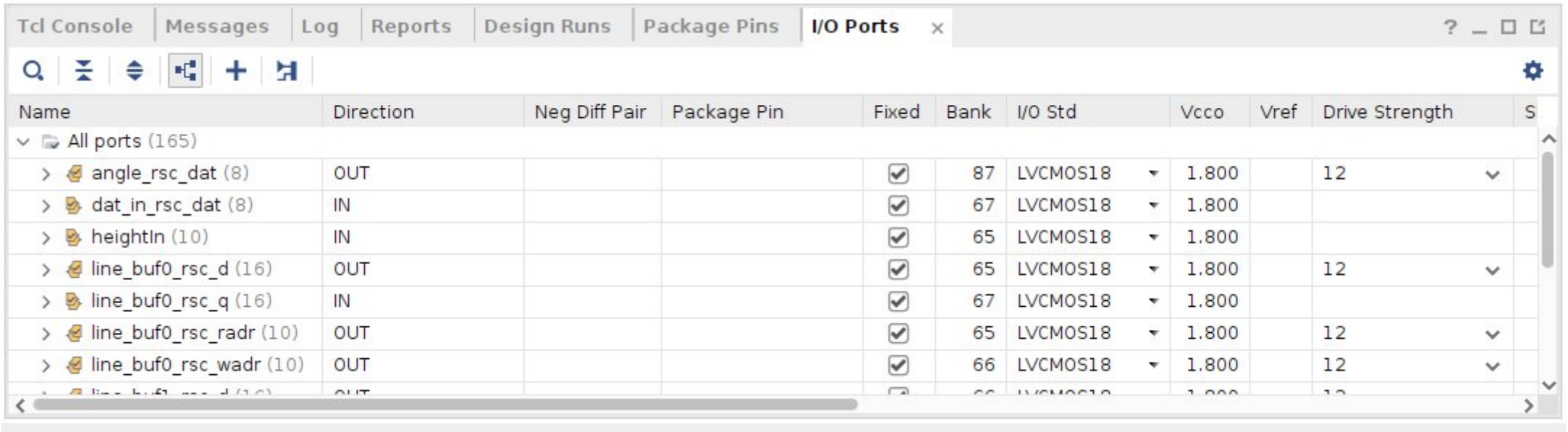
```
set_input_delay -clock [get_clocks clk] -min -add_delay 0.000 [get_ports arst_n]
set_input_delay -clock [get_clocks clk] -max -add_delay 0.000 [get_ports arst_n]
```

- Open synthesis design, and choose I/O planning for set up constraints





Check Fixed and set I/O standard



Name	Direction	Neg Diff Pair	Package Pin	Fixed	Bank	I/O Std	Vcco	Vref	Drive Strength	S
All ports (165)										
angle_rsc_dat (8)	OUT			☑	87	LVCMOS18	1.800		12	
dat_in_rsc_dat (8)	IN			☑	67	LVCMOS18	1.800			
heightIn (10)	IN			☑	65	LVCMOS18	1.800			
line_buf0_rsc_d (16)	OUT			☑	65	LVCMOS18	1.800		12	
line_buf0_rsc_q (16)	IN			☑	67	LVCMOS18	1.800			
line_buf0_rsc_radr (10)	OUT			☑	65	LVCMOS18	1.800		12	
line_buf0_rsc_wadr (10)	OUT			☑	66	LVCMOS18	1.800		12	

Generate bitstream

- Click generate bitstream, it will generate the bitstream file under the directory of ***project_name***.runs/impl_1/***design.bit***