ASOC Lab3 Snps-flow

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Lab Synthesis:

1. Report contents must include the description of command in scripts (tcl file)
   make all:會執行 setup、compile_for_timing。
   setup:會檢查 LOG 是否存在，如果 LOG 不存在，會使用命令 mkdir 建立。
   compile_for_timing:會先執行 set up，然後在 dc_shell 執行 compile_for_timing.tcl 並複製結果至 compile_for_timing.log。
   compile_for_timing.tcl:會執行 common.tcl，common.tcl 會設定。
   然後執行一些在 common.tcl 裡設定完成的檔案類型，如 Constraints、Warning，在執行 set_dont_use.tcl。
   最後 check_design、使用 compile 設定選項，將 timing、qor、area、power 寫成 report。
2. The screenshot of every stage in design flow

```
  Optimization Complete
  ---------------------
1
## reporting and output
report_timing > ../../reports/timing_${DESIGN_NAME}_timing_reports.log
report_qor > ../../reports/timing_${DESIGN_NAME}_qor_reports.log
report_area -hierarchy  > ../../reports/timing_${DESIGN_NAME}_area_reports.log
report_power -hierarchy > ../../reports/timing_${DESIGN_NAME}_power_reports.log
change_names -rules verilog
Warning: In the design i2c_master_top, net 'sda_pad_o' is connecting multiple ports. (UCN-1)
1
write_file -format verilog -hierarchy -pg -output ../../input/${DESIGN_NAME}.v
Warning: No PG information is available for design. (UPF-663)
Writing verilog file '/home/m111/m111061621/lab_formal_release/input/i2c_master_top.v'.
Warning: Verilog 'assign' or 'tran' statements are written out. (VO-4)
1
quit

Memory usage for this session 324 Mbytes.
Memory usage for this session including child processes 324 Mbytes.
CPU usage for this session 15 seconds ( 0.00 hours ).
Elapsed time for this session 281 seconds ( 0.08 hours ).

Thank you...
date >  compile_for_timing
date >  all
```

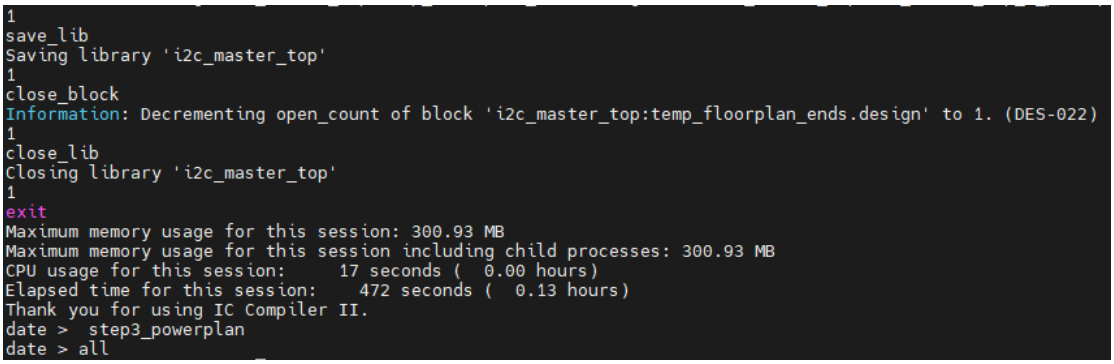
3. Discussion and observation:

```
Inferred memory devices in process
        in routine i2c_master_top line 160 in file
                '/home/m111/m111061621/lab_formal_release/lab_synthesis/work/../../common/i2c_project/rtl/verilog/i2c_master_top.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|    wb_ack_o_reg     | Flip-flop |   1   |  N  |  N |  N |  N |  N |  N |  N |
===============================================================================
```

Inferred memory devices in process in routine 這個部分會根據寫的 verilog code 有所不同。先進入 Beginning Implementation Selection，面積逐漸縮小，Beginning Delay Optimization Phase 也會嘗試縮小面積，Beginning Area-Recovery Phase 會把面積縮到最小。

Lab1 Floorplan:

1. Report contents must include the description of command in scripts (tcl file)
   make all:會執行 setup、step1_data_setup、step2_floorplan、step3_powerplan。
   step1_data_setup 會在 icc2_shell 執行 step1_data_setup.tcl 並複製結果至 step1_data_setup.log。
   step2_floorplan 會在 icc2_shell 執行 step2_floorplan.tcl 並複製結果至 step2_floorplan.log。
   step3_powerplan 會在 icc2_shell 執行 step3_powerplan.tcl 並複製結果至 tep3_powerplanlog。
   step1_data_setup.tcl:先執行 common.tcl 進行設定，設定連結和目標 lib，然後建立 lib，讀取 tlup、layermap、verilog，設定目前的 design 並執行 Constraints_file，進行保存之後關閉。
   step2_floorplan.tcl:先執行 common.tcl 進行設定，設定連結和目標 lib，打開 lib，生成 clocks、exceptions、disable 報告，設定 Net 和 Pin，之後設置其他選項並保存 block，設定希望的繞線方向後，建立布局，放置 Pin，設定 VDD、VSS 並保存 block。
   step3_powerplan.tcl:執行 common.tcl 進行設定，複製 block 後再打開複製的 block，設定和連接 VDD、VSS，建立 Power_Plan、STD_Cells_Rail、Top_Vertical_Mesh、Top_Horizontal_Mesh、Rectangular_Rings，當中包含刪除電源、set_pg_strategy、compile_pg –strategies、check_pg_connectivity，保存關閉後退出。
2. The screenshot of every stage in design flow



3. Discussion and observation
   從 Start GR phase0 可以看到有些 overflow，Start GR phase1 的 overflow 逐漸減少，到了 Start GR phase2、3 的 overflow 已經解決。

```
Start GR phase 0
Current Stage stats:
[End of Initial Routing] Elapsed real time: 0:00:00
[End of Initial Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Initial Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Initial Routing] Total (MB): Used  246  Alloctr  247  Proc 2742
Initial. Routing result:
Initial. Both Dirs: Overflow =    12 Max = 3 GRCs =    24 (0.12%)
Initial. H routing: Overflow =     8 Max = 3 (GRCs =  1) GRCs =    14 (0.14%)
Initial. V routing: Overflow =     3 Max = 1 (GRCs = 10) GRCs =    10 (0.10%)
Initial. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M2         Overflow =     8 Max = 3 (GRCs =  1) GRCs =    14 (0.14%)
Initial. M3         Overflow =     3 Max = 1 (GRCs = 10) GRCs =    10 (0.10%)
Initial. M4         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M5         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M6         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M7         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M8         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. M9         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
Initial. MRDL       Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

Initial. Total Wire Length = 4773.31
Initial. Layer M1 wire length = 32.93
Initial. Layer M2 wire length = 2112.95
Initial. Layer M3 wire length = 2476.79
Initial. Layer M4 wire length = 150.65
Initial. Layer M5 wire length = 0.00
Initial. Layer M6 wire length = 0.00
Initial. Layer M7 wire length = 0.00
Initial. Layer M8 wire length = 0.00
Initial. Layer M9 wire length = 0.00
Initial. Layer MRDL wire length = 0.00
Initial. Total Number of Contacts = 4480
Initial. Via VIA12SQ_C count = 1871
Initial. Via VIA23SQ_C count = 2575
Initial. Via VIA34SQ_C count = 34
Initial. Via VIA45SQ count = 0
Initial. Via VIA56SQ count = 0
Initial. Via VIA67SQ_C count = 0
Initial. Via VIA78SQ_C count = 0
Initial. Via VIA89_C count = 0
Initial. Via VIA9RDL count = 0
Initial. completed.
```

```
Start GR phase 1
Fri Apr 26 23:18:57 2024
Number of partitions: 1 (1 x 1)
[rtOvlpParts] Elapsed real time: 0:00:00
[rtOvlpParts] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
Current Stage stats:
[End of Phase1 Routing] Elapsed real time: 0:00:00
[End of Phase1 Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Phase1 Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Phase1 Routing] Total (MB): Used  246  Alloctr  247  Proc 2742
phase1. Routing result:
phase1. Both Dirs: Overflow =     1 Max = 1 GRCs =     3 (0.01%)
phase1. H routing: Overflow =     1 Max = 1 (GRCs =  2) GRCs =     2 (0.02%)
phase1. V routing: Overflow =     0 Max = 1 (GRCs =  1) GRCs =     1 (0.01%)
phase1. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M2         Overflow =     1 Max = 1 (GRCs =  2) GRCs =     2 (0.02%)
phase1. M3         Overflow =     0 Max = 1 (GRCs =  1) GRCs =     1 (0.01%)
phase1. M4         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M5         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M6         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M7         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M8         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. M9         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase1. MRDL       Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

phase1. Total Wire Length = 4779.30
phase1. Layer M1 wire length = 32.93
phase1. Layer M2 wire length = 2105.49
phase1. Layer M3 wire length = 2476.48
phase1. Layer M4 wire length = 161.22
phase1. Layer M5 wire length = 3.19
phase1. Layer M6 wire length = 0.00
phase1. Layer M7 wire length = 0.00
phase1. Layer M8 wire length = 0.00
phase1. Layer M9 wire length = 0.00
phase1. Layer MRDL wire length = 0.00
phase1. Total Number of Contacts = 4519
phase1. Via VIA12SQ_C count = 1871
phase1. Via VIA23SQ_C count = 2604
phase1. Via VIA34SQ_C count = 42
phase1. Via VIA45SQ count = 2
phase1. Via VIA56SQ count = 0
phase1. Via VIA67SQ_C count = 0
phase1. Via VIA78SQ_C count = 0
phase1. Via VIA89_C count = 0
phase1. Via VIA9RDL count = 0
phase1. completed.
```

```
Start GR phase 2
Fri Apr 26 23:18:58 2024
Number of partitions: 1 (1 x 1)
[rtOvlpParts] Elapsed real time: 0:00:00
[rtOvlpParts] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[updNetsDmd] Elapsed real time: 0:00:00
[updNetsDmd] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
Current Stage stats:
[End of Phase2 Routing] Elapsed real time: 0:00:00
[End of Phase2 Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Phase2 Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Phase2 Routing] Total (MB): Used  246  Alloctr  247  Proc 2742
phase2. Routing result:
phase2. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
phase2. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M4         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M5         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M6         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M7         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M8         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. M9         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase2. MRDL       Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

phase2. Total Wire Length = 4779.33
phase2. Layer M1 wire length = 32.93
phase2. Layer M2 wire length = 2105.19
phase2. Layer M3 wire length = 2474.19
phase2. Layer M4 wire length = 161.54
phase2. Layer M5 wire length = 5.47
phase2. Layer M6 wire length = 0.00
phase2. Layer M7 wire length = 0.00
phase2. Layer M8 wire length = 0.00
phase2. Layer M9 wire length = 0.00
phase2. Layer MRDL wire length = 0.00
phase2. Total Number of Contacts = 4523
phase2. Via VIA12SQ_C count = 1871
phase2. Via VIA23SQ_C count = 2604
phase2. Via VIA34SQ_C count = 44
phase2. Via VIA45SQ count = 4
phase2. Via VIA56SQ count = 0
phase2. Via VIA67SQ_C count = 0
phase2. Via VIA78SQ_C count = 0
phase2. Via VIA89_C count = 0
phase2. Via VIA9RDL count = 0
phase2. completed.
```

```
Start GR phase 3
Fri Apr 26 23:18:58 2024
Number of partitions: 1 (1 x 1)
[rtOvlpParts] Elapsed real time: 0:00:00
[rtOvlpParts] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[updNetsDmd] Elapsed real time: 0:00:00
[updNetsDmd] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
Current Stage stats:
[End of Phase3 Routing] Elapsed real time: 0:00:00
[End of Phase3 Routing] Elapsed cpu  time: sys=0:00:00 usr=0:00:00 total=0:00:00
[End of Phase3 Routing] Stage (MB): Used    0  Alloctr    0  Proc    0
[End of Phase3 Routing] Total (MB): Used  246  Alloctr  247  Proc 2742
phase3. Routing result:
phase3. Both Dirs: Overflow =     0 Max = 0 GRCs =     0 (0.00%)
phase3. H routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. V routing: Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M1         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M2         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M3         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M4         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M5         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M6         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M7         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M8         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. M9         Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)
phase3. MRDL       Overflow =     0 Max = 0 (GRCs =  0) GRCs =     0 (0.00%)

phase3. Total Wire Length = 4779.33
phase3. Layer M1 wire length = 32.93
phase3. Layer M2 wire length = 2105.19
phase3. Layer M3 wire length = 2474.19
phase3. Layer M4 wire length = 161.54
phase3. Layer M5 wire length = 5.47
phase3. Layer M6 wire length = 0.00
phase3. Layer M7 wire length = 0.00
phase3. Layer M8 wire length = 0.00
phase3. Layer M9 wire length = 0.00
phase3. Layer MRDL wire length = 0.00
phase3. Total Number of Contacts = 4523
phase3. Via VIA12SQ_C count = 1871
phase3. Via VIA23SQ_C count = 2604
phase3. Via VIA34SQ_C count = 44
phase3. Via VIA45SQ count = 4
phase3. Via VIA56SQ count = 0
phase3. Via VIA67SQ_C count = 0
phase3. Via VIA78SQ_C count = 0
phase3. Via VIA89_C count = 0
phase3. Via VIA9RDL count = 0
phase3. completed.
```

Lab2 Placement & Route

1. Report contents must include the description of command in scripts (tcl file)

   step4_place.tcl： 先執行 common.tcl 進行設定，設定連結和目標 lib，然後建立 lib，set_app_options -name ...等設置了一系列優化和佈局相關的選項，place_opt 和 legalize_placement 分別執行了佈局和合法化操作。最後輸出結果至 step4_place.log。

   step5_clock_tree_synthesis.tcl： 先執行 common.tcl 進行設定，設定連結和目標 lib，然後建立 lib，通過 set_clock_tree_options 命令設置了時脈樹的選項，包括了時脈 clocks 和 target_skew。使用 set_lib_cell_purpose 命令設置了 clock tree 中所需的細胞目的，進行了時脈不確定性的設置，並創建了時脈的 route 規則。最後輸出結果至 step5_clock_tree_synthesis.log。

   step6_route.tcl： 先執行 common.tcl 進行設定，設定連結和目標 lib，然後建立 lib，通過 set_app_option 命令設置了一個 route 的選項。進行了自動 route 和優化，同時自動連接電源，然後進行 LVS 檢查。最終輸出結果至 step6_route.log。

2. The screenshot of every stage in design flow

```
****************************************
  Report : Placement Attempts
  Site   : unit
****************************************

number of cells:                    702
number of references:                75
number of site rows:                 67
number of locations attempted:    15419
number of locations failed:           0  (0.0%)

Legality of references at locations:
0 references had failures.

Legality of references in rows:
0 references had row failures.

****************************************
  Report : Cell Displacements
****************************************

number of cells aggregated:         702 (7283 total sites)
avg row height over cells:        0.600 um
rms cell displacement:            0.000 um ( 0.00 row height)
rms weighted cell displacement:   0.000 um ( 0.00 row height)
max cell displacement:            0.000 um ( 0.00 row height)
avg cell displacement:            0.000 um ( 0.00 row height)
avg weighted cell displacement:   0.000 um ( 0.00 row height)
number of cells moved:               0
number of large displacements:       0
large displacement threshold:     3.000 row height
```

```
************************************************
Report          : create_qor_snapshot (clock)
Design          : i2c_master_top
Version         : R-2020.09-SP3
Date            : Sun Apr 28 03:25:26 2024
Time unit       : 1.00ns
Resistance unit : 1.00MOhm
Capacitance unit: 1.00fF
Voltage unit    : 1.00V
Current unit    : 1.00uA
Power unit      : 1.00pW
Location        : /home/m111/m111061631/asoc_lab3/lab_formal_release/lab2_pnr/work/./
************************************************
No. of scenario = 2
s1 = func_fast
s2 = func_slow
---------------------------------------------------------------------------
WNS of each timing group:                    s1       s2
---------------------------------------------------------------------------
wb_clk_i                                  1.3226   1.2999
---------------------------------------------------------------------------
Setup WNS:                                1.3226   1.2999      1.2999
Setup TNS:                                0.0000   0.0000      0.0000
Number of setup violations:                    0        0           0
Hold WNS:                                 0.0265   0.0272      0.0265
Hold TNS:                                 0.0000   0.0000      0.0000
Number of hold violations:                     0        0           0
Number of max trans violations:                0        0           0
Number of max cap violations:                  0        0           0
Number of min pulse width violations:          0        0           0
---------------------------------------------------------------------------
Area:                                                          331.668
Cell count:                                                        713
Buf/inv cell count:                                                150
Std cell utilization:                                           0.2046
CPU(s):                                                            87
Mem(Mb):                                                         1188
Host name:                                                       ws27
```

3. Discussion and observation

```
****************************************
Report : congestion
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Sun Apr 28 03:33:38 2024
****************************************

Layer     |    overflow     |              # GRCs has
Name      |  total  |  max  | overflow (%)      | max overflow
-------------------------------------------------------------
Both Dirs |      53 |     4 |      24  ( 0.12%) |       4
H routing |      53 |     4 |      24  ( 0.24%) |       4
V routing |       0 |     0 |       0  ( 0.00%) |       0
```

如上圖可以觀察出，整個設計中的擁擠情況相對較輕微，但在 "Both Dirs" 和 "H routing" 層中都存在一定程度的擁擠，還是會有些微的 overflow，可以進一步的分析和優化。

Lab StarRC

1. Report contents must include the description of command in scripts (tcl file)

   gen_star_cmd_gate_NDM.tcl 和 gen_star_cmd_gate_DEFLEF.tcl 是生成用於 StarRC 工具的命令文件(star_cmd_gate)，用於執行靜態分析和從設計中提取 RC 參數。gen_StarRC_smc.tcl 則是用於生成 StarRC.smc，用於描述電路模型和參數，使用 foreach 循環遍歷 $STARRC_SELECTED_CORNERS 列表中的每個元素，其中 $STARRC_SELECTED_CORNERS 是一個包含 "slow" 和 "fast" 兩個元素的變量，表示 StarRC 要生成的兩種角落情況。

2. The screenshot of every stage in design flow

```
Setup                  Elp=00:00:23 Cpu=00:00:01 Usr=1.6    Sys=0.0    Mem=505.0
Layers                 Elp=00:00:00 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=505.1
HN                     Elp=00:00:00 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=510.9
Cells                  Elp=00:00:01 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=513.9
Translate              Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=505.3
NetlistSetup           Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=475.6
GPD_XtractSetup        Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=505.2
GPD_NameMap            Elp=00:00:01 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=475.9
xTract                 Elp=00:00:01 Cpu=00:00:01 Usr=1.2    Sys=0.1    Mem=522.7
xTractPP               Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=338.6
ReportViolations       Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=475.6
ReportOpens            Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=475.5
GPD_PostProcess        Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=475.9
GPD_Converter1         Elp=00:00:00 Cpu=00:00:00 Usr=0.1    Sys=0.0    Mem=333.8
GPD_Converter2         Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.4
GPD_Converter_merge_c1 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.3
GPD_Converter_merge_c2 Elp=00:00:00 Cpu=00:00:00 Usr=0.0    Sys=0.0    Mem=332.3

Done          Elp=00:00:26 Cpu=00:00:03 Usr=3.2    Sys=0.1    Mem=522.7
```

3. Discussion and observation

進行完 StarRC 後，提供準確的 RC 參數以利後面設計人員進行設計分析和優化。且 StarRC 能夠與其他 EDA 工具完美兼容，可以輕鬆與設計流程中的其他工具進行交互，例如靜態時序分析工具、佈局工具等。

Lab PrimeTime

1. Report contents must include the description of command in scripts (tcl file)

   gen_pt_cmd.tcl : 使用 foreach 迴圈對 PT_SELECTED_SCENARIO 進行迭代打開一個文件，文件路徑，並將文件描述符存儲在變數 fp 中，將 PrimeTime 命令寫入文件中，對每個條件生成相應 PT 命令文件。

   run_pt_cmd_fast.tcl : 使用 PrimeTime 方法執行在 fast corner 執行時序分析和設計優化。

   run_pt_cmd_slow.tcl : 使用 PrimeTime 方法執行在 slow corner 執行時序分析和設計優化。

2. The screenshot of every stage in design flow

```
Initial cell usage:
Cell Group            Count                    Area
-----------------------------------------------------------
Combinational          560 ( 79%)          166.99 ( 50%)
Sequential             153 ( 21%)          164.64 ( 50%)
Clock                    0 (  0%)            0.00 (  0%)
Others                   0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                  713 (100%)          331.62 (100%)
```

```
Cell usage after iteration 1:
Cell Group            Count                    Area
-----------------------------------------------------------
Combinational          560 ( 79%)          166.99 ( 50%)
Sequential             153 ( 21%)          164.64 ( 50%)
Clock                    0 (  0%)            0.00 (  0%)
Others                   0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                  713 (100%)          331.62 (100%)
```

```
Cell usage after iteration 2:
Cell Group            Count                    Area
-----------------------------------------------------------
Combinational          560 ( 79%)          166.99 ( 50%)
Sequential             153 ( 21%)          164.55 ( 50%)
Clock                    0 (  0%)            0.00 (  0%)
Others                   0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                  713 (100%)          331.53 (100%)
```

```
Cell usage after iteration 3:
Cell Group            Count                  Area
-----------------------------------------------------------
Combinational          560 ( 79%)          166.19 ( 50%)
Sequential             153 ( 21%)          164.55 ( 50%)
Clock                    0 (  0%)            0.00 (  0%)
Others                   0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                  713 (100%)          330.74 (100%)
```

```
Cell usage after iteration 4:
Cell Group            Count                  Area
-----------------------------------------------------------
Combinational          560 ( 79%)          164.24 ( 50%)
Sequential             153 ( 21%)          164.55 ( 50%)
Clock                    0 (  0%)            0.00 (  0%)
Others                   0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                  713 (100%)          328.78 (100%)
```

```
Final cell usage:
Cell Group            Count                  Area
-----------------------------------------------------------
Combinational          560 ( 79%)          164.24 ( 50%)
Sequential             153 ( 21%)          164.55 ( 50%)
Clock                    0 (  0%)            0.00 (  0%)
Others                   0 (  0%)            0.00 (  0%)
-----------------------------------------------------------
Total                  713 (100%)          328.78 (100%)
```

3. Discussion and observation

進行完 PrimeTime 分析後，每一次迭代會造成些微的 Area 減少，也並未產生任何 violation，由此可知，PrimeTime 迭代後的效果是確保設計在滿足所有約束的同時進行最大程度優化性能。

Lab4 Chip Finishing

1. Report contents must include the description of command in scripts (tcl file)
   check_lvs > ../../reports/${DESIGN_NAME}.lvs.rpt：檢查 LVS 驗證，並將結果輸出到名為${DESIGN_NAME}.lvs.rpt 的報告檔案中。

   report_design -all > ../../reports/${DESIGN_NAME}.PR_summary.rpt：產生設計摘要報告，並將結果輸出到名為${DESIGN_NAME}.PR_summary.rpt 的報告文件中。

   report_timing -capacitance -transition_time -input_pins -nets -delay_type max > ../../reports/timing.max.tim：產生時序分析報告並將結果輸出到名為的 timing.max.tim 報告文件中。
   -delay_type 設定要為 Max Delay 還是 Min Delay

   write_verilog :它主要是負責將目前所設計的 netlist 轉成 verilog 的形式
   -compress gzip:在寫入 Verilog 檔案時，使用 Gzip 壓縮格式。
   -exclude:排除某些內容。
   -hierarchy all:輸出所有的設計結構。

   write_sdc -output ../../results/${DESIGN_NAME}.out.sdc：使用 write_sdc 命令產生約束文件，並將它輸出到${DESIGN_NAME}.out.sdc 文件中。

   report_timing -crosstalk_delta：透過 report_timing 命令產生時序分析報告，並包含 crosstalk。crosstalk 指的是一條線路會去影響離它很近的線路，兩條線路之間會互相影響產生雜訊。

   write_parasitics -format SPEF -output ../../results/${DESIGN_NAME}.out.spef：使用 write_parasitics 指令產生 SPEF 檔案，並將它輸出到 ${DESIGN_NAME}.out.spef 文件中。

   write_def ../../results/${DESIGN_NAME}.out.def：使用 write_def 命令產生 DEF 檔案，並將它輸出到${DESIGN_NAME}.out.def 文件中。

2. The screenshot of every stage in design flow

```
DRC-SUMMARY:
        @@@@@@@ TOTAL VIOLATIONS =      0



Total Wire Length =                    7081 micron
Total Number of Contacts =             4946
Total Number of Wires =                5853
Total Number of PtConns =              593
Total Number of Routed Wires =       5853
Total Routed Wire Length =           6661 micron
Total Number of Routed Contacts =       4946
```

```
****************************************
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
        -input_pins
        -crosstalk_delta
Design : i2c_master_top
Version: R-2020.09-SP3
Date   : Sat Apr 27 09:17:35 2024
****************************************

  Startpoint: byte_controller/bit_controller/cnt_reg[6] (rising edge-triggered flip-flop clocked by wb_clk_i)
  Endpoint: byte_controller/bit_controller/cnt_reg[0] (rising edge-triggered flip-flop clocked by wb_clk_i)
  Mode: func
  Corner: slow
  Scenario: func_slow
  Path Group: wb_clk_i
  Path Type: max

  Point                                    Delta     Incr      Path
  -----------------------------------------------------------------------------
  clock wb_clk_i (rise edge)                         0.00      0.00
  clock network delay (ideal)                        0.00      0.00

  byte_controller/bit_controller/cnt_reg[6]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)
                                                     0.00      0.00 r
```

```
                                                     0.00      0.39 r
  data arrival time                                            0.39

  clock wb_clk_i (rise edge)                         2.00      2.00
  clock network delay (ideal)                        0.00      2.00
  byte_controller/bit_controller/cnt_reg[0]/CK (SAEDRVT14_FDPRBQ_V2LP_0P5)
                                                     0.00      2.00 r
  clock uncertainty                                 -0.30      1.70
  library setup time                                 0.00      1.70
  data required time                                           1.70
  -----------------------------------------------------------------------------
  data required time                                           1.70
  data arrival time                                           -0.39
  -----------------------------------------------------------------------------
  slack (MET)                                                  1.31
```

```
save_block
Information: Saving block 'i2c_master_top:temp_route_ends.design'
1
save_lib
Saving library 'i2c_master_top'
1
close_block
Information: Decrementing open_count of block 'i2c_master_top:temp_route_ends.design' to 1. (DES-022)
1
close_lib
Closing library 'i2c_master_top'
Information: The net parasitics of block i2c_master_top are cleared. (TIM-123)
1
exit
Maximum memory usage for this session: 519.24 MB
Maximum memory usage for this session including child processes: 2741.88 MB
CPU usage for this session:     48 seconds (  0.01 hours)
Elapsed time for this session:    705 seconds (  0.20 hours)
Thank you for using IC Compiler II.
date >  step7_finishing
date > all
```

3. Discussion and observation

在一開始合成時，它的 DRC violation 會很大，它會慢慢地修正直到 violation 降為 0。

在這一步驟中，還會產生出 Timing Report，這能夠幫助我們了解電路是否能夠滿足我們所設定的 Timing constraint

Lab IC Validator - DRC

1. Report contents must include the description of command in scripts (tcl file)

icv : IC Validator 的 Command。

-c $(TOP_CELL) :選定 TOP Module 的 Cell

-f $(FORMAT) :選擇 layout 的格式

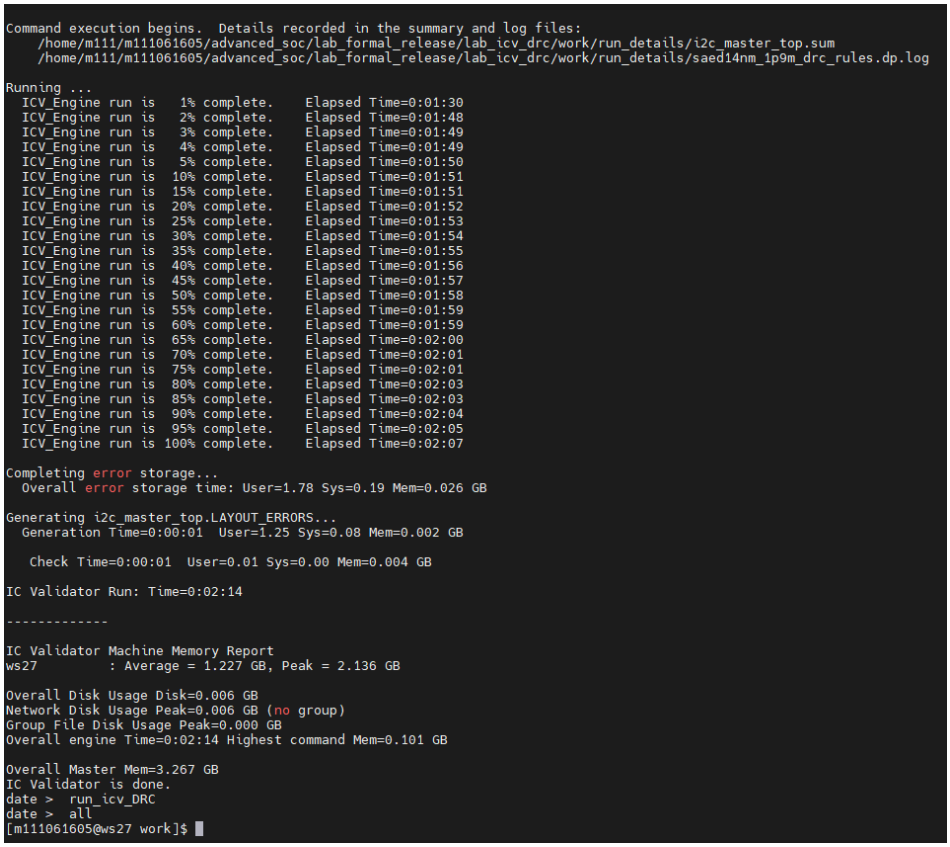
-lf $(LAYER_MAPPING_FILE) :選擇 layout 映射的檔案

-p $(INPUT_LIBRARY_PATH) :選擇輸入的 library，這個指向了前面所有步驟所產生的 result

-i $(LAYOUT_FILE) :選擇要檢查的 layout 檔案

-I $(RUN_DIR) :設定工作目錄

2. The screenshot of every stage in design flow



3. Discussion and observation

在 DRC 驗證中，它所輸入的參數內包含了 layout 檔案，主要是透過 layout 檔案來檢查它們是否有違反晶圓代工廠所設下的 DRC rule。如果有違反的話，在晶片實際做出來後，會有高機率功能會出現一些問題。

Lab IC Validator – LVS

1. Report contents must include the description of command in scripts (tcl file)

   icv: IC Validator 的 Command。

   -i $GDSII_FILE :選定 GDSII 檔案，用來驗證 gate level 電路的功能

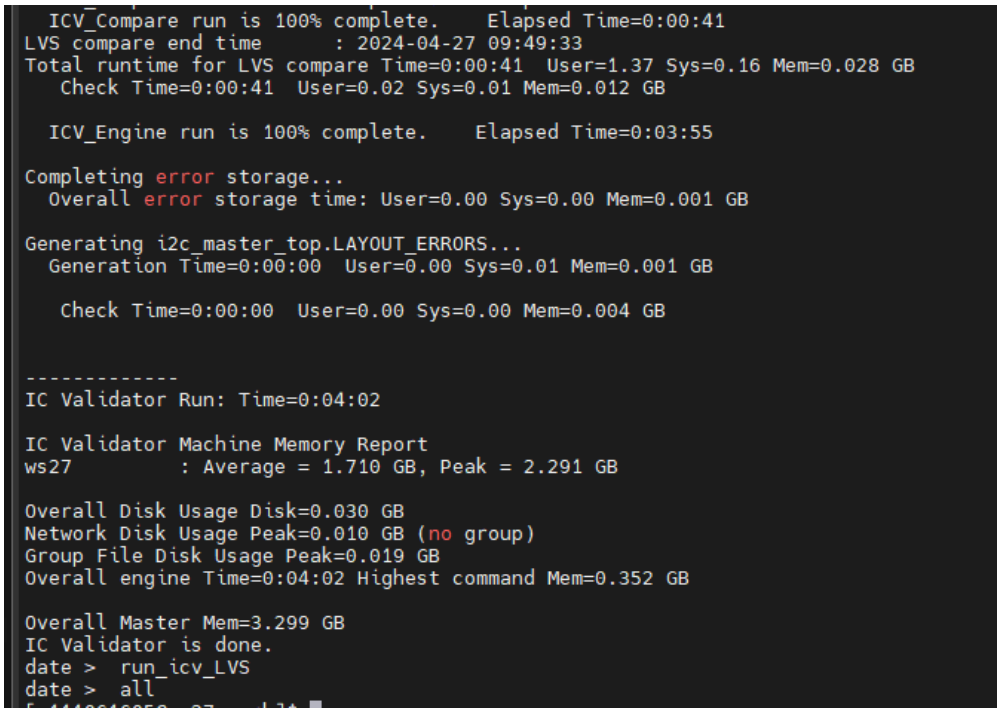
   -c $GDSII_TOPCELL_NAME :選定 Top Module

   -s $SPICE_FILE :選定 SPICE 檔案，SPICE 檔案是一開始

   -stc $NETLIST_TOPCELL_NAME 選擇 SPICE 檔案中 Top Module 的名字

   -sf SPICE :告知 icv -s 選項中的格式為 SPICE。

2. The screenshot of every stage in design flow



3. Discussion and observation

在 LVS 驗證中，需要輸入 GDSII 和 SPICE 檔案，這是為了要能夠去比較合成出來的電路和 SPICE 中原始的電路之間的動作是否一致。

Lab formality:

1. Report contents must include the description of command in scripts (tcl file)
   gen_formality_cmd.tcl:將一些設定、環境寫入 run_formality_cmd.tcl。
   run_formality_cmd.tcl: 先執行 common.tcl 進行設定，讀取 lib、設置黑盒，讀取參考的設計跟實際的設計 verilog 的.v 檔。設置驗證環境，set verify_set_undriven_signals BINARY 是將非驅動訊號設置為 BINARY，set verify_check_gate_reserve_gating true 是檢查 gate reserve gating，verify 啟動 formality 開始驗證。
2. The screenshot of every stage in design flow

```
****************************** Verification Results ******************************
Verification SUCCEEDED
---------------------
 Reference design: r:/WORK/i2c_master_top
 Implementation design: i:/WORK/i2c_master_top
 167 Passing compare points
--------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT   TOTAL
--------------------------------------------------------------------------------
Passing (equivalent)           0       0       0       0      14     153       0     167
Failing (not equivalent)       0       0       0       0       0       0       0       0
********************************************************************************
1
quit

Maximum memory usage for this session: 615 MB
CPU usage for this session: 3.11 seconds ( 0.00 hours )
Current time: Sat Apr 27 02:04:52 2024
Elapsed time: 105 seconds ( 0.03 hours )

Thank you for using Formality (R)!
date > run_formality_cmd
date >  all
```

3. Discussion and observation

```
********************************************************************************

Status:  Verifying...

****************************** Matching Results ******************************
 167 Compare points matched by name
 0 Compare points matched by signature analysis
 0 Compare points matched by topology
 19 Matched primary inputs, black-box outputs
 0(0) Unmatched reference(implementation) compare points
 0(0) Unmatched reference(implementation) primary inputs, black-box outputs
 2(0) Unmatched reference(implementation) unread points
********************************************************************************


****************************** Verification Results ******************************
Verification SUCCEEDED
---------------------
 Reference design: r:/WORK/i2c_master_top
 Implementation design: i:/WORK/i2c_master_top
 167 Passing compare points
--------------------------------------------------------------------------------
Matched Compare Points     BBPin    Loop   BBNet     Cut    Port     DFF     LAT   TOTAL
--------------------------------------------------------------------------------
Passing (equivalent)           0       0       0       0      14     153       0     167
Failing (not equivalent)       0       0       0       0       0       0       0       0
********************************************************************************
```

```
module i2c_master_top ( wb_clk_i , wb_rst_i , arst_i , wb_adr_i , wb_dat_i ,
    wb_dat_o , wb_we_i , wb_stb_i , wb_cyc_i , wb_ack_o , wb_inta_o ,
    scl_pad_i , scl_pad_o , scl_padoen_o , sda_pad_i , sda_pad_o ,
    sda_padoen_o , VDD , VSS ) ;
```

19 個 primary inputs、outputs 符合在 results 資料夾中的 i2c_master_top.v 的數量。