112-1 SoC Design Laboratory
Lab4-1 submission guide

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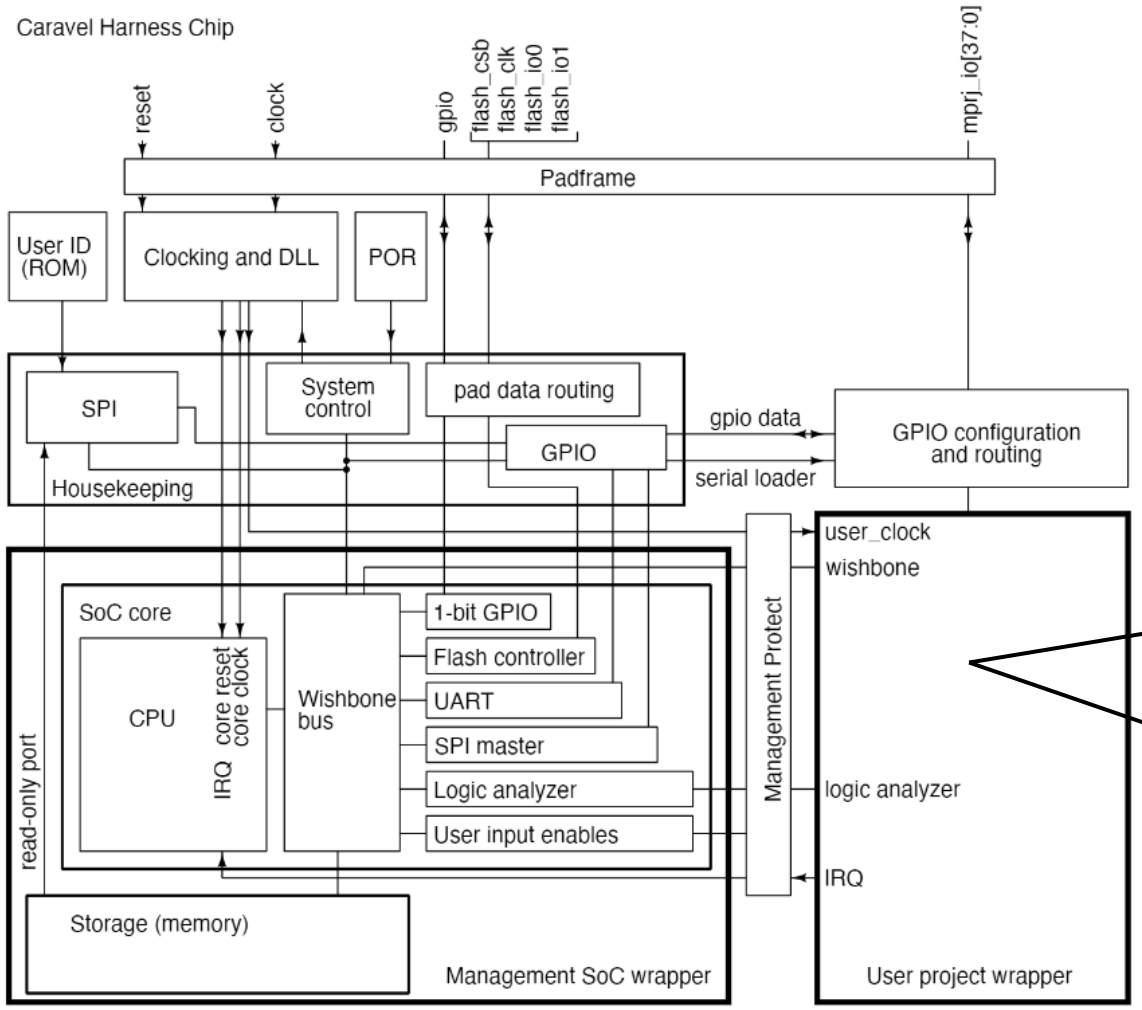
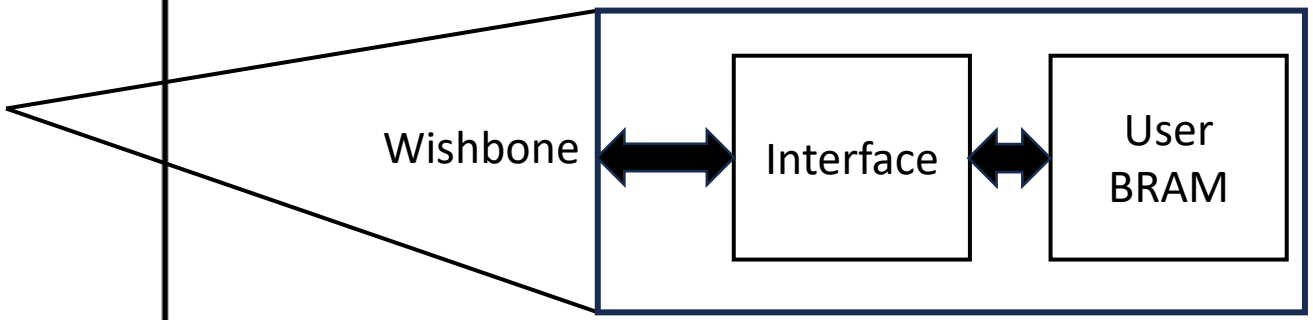
Requirements

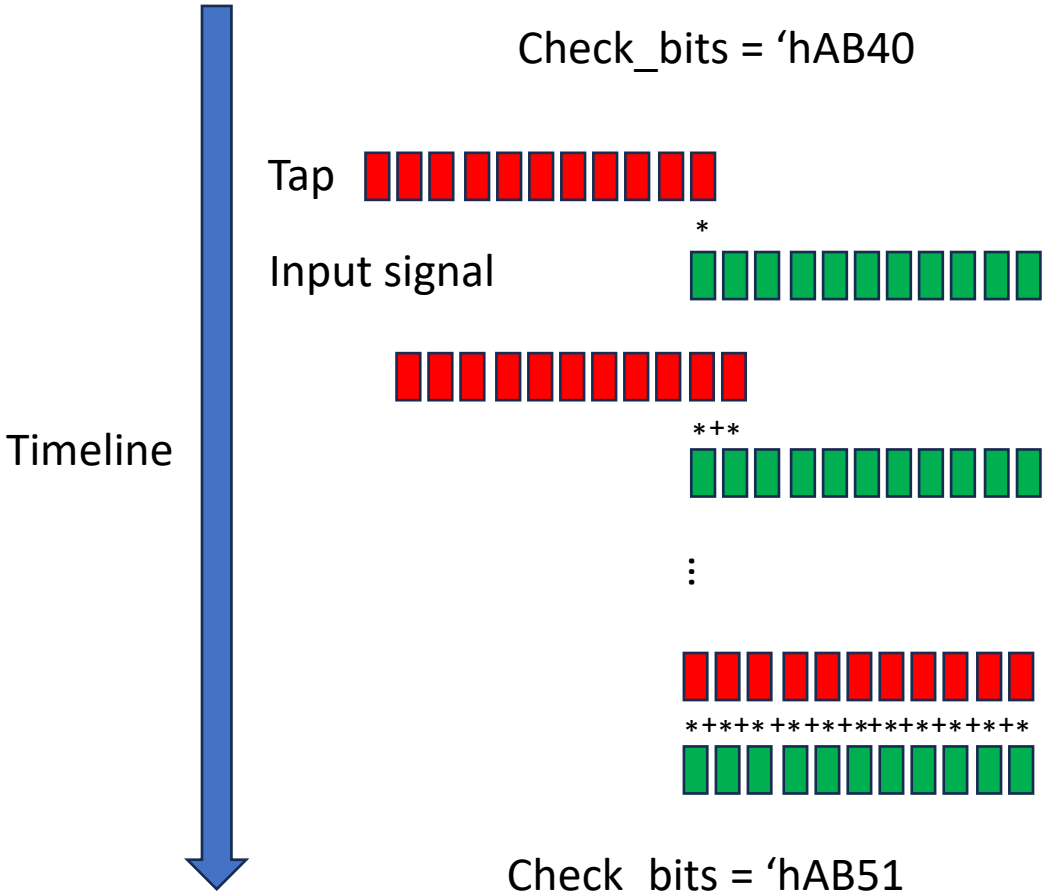


- FIR C code
  - fir.c
  - fir.h
- Interface between user BRAM and wishbone
- Synthesize user project



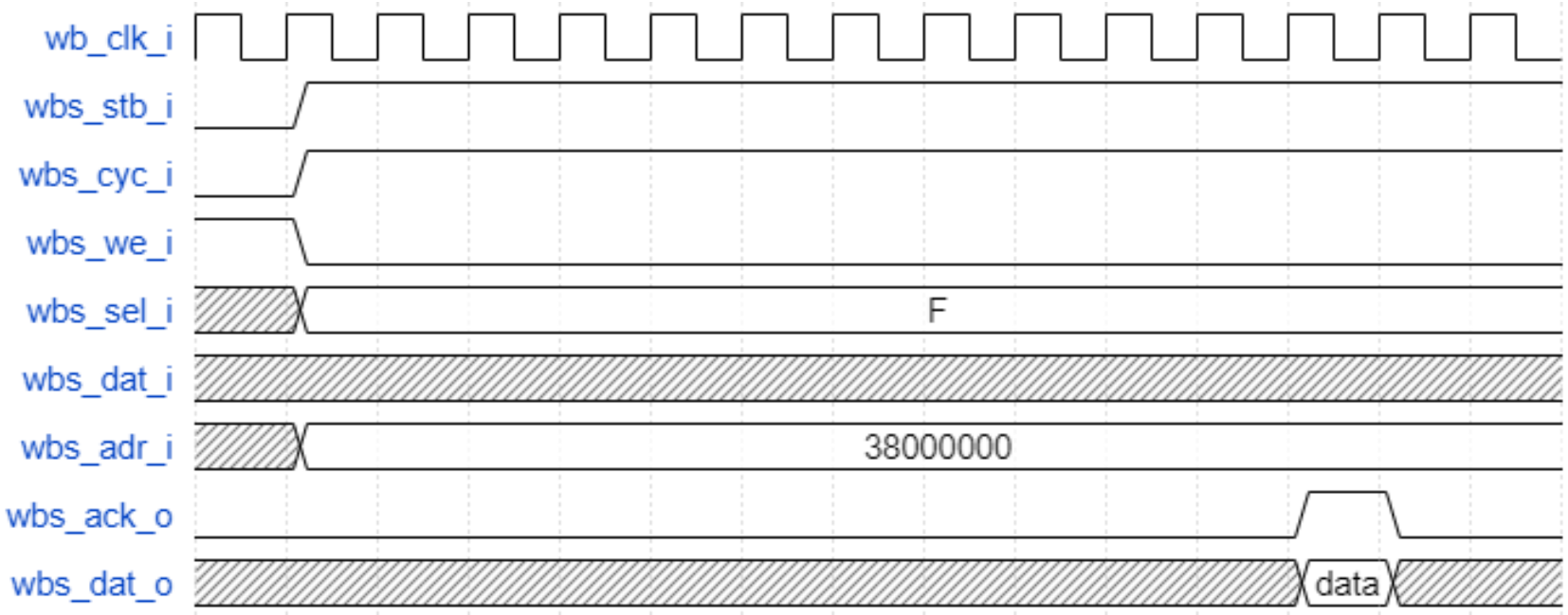
FIR Specification

- Tap number = 11
- Input signal number = 11
- Start mark = ‘hAB40
- End mark = ‘hAB51



Interface

```
48      input wb_clk_i,
49      input wb_rst_i,
50      input wbs_stb_i,
51      input wbs_cyc_i,
52      input wbs_we_i,
53      input [3:0] wbs_sel_i,
54      input [31:0] wbs_dat_i,
55      input [31:0] wbs_adr_i,
56      output wbs_ack_o,
57      output [31:0] wbs_dat_o,
```



Submission (1/2)

- Hierarchy:
  - StudentID_lab4-1/
    - Report.pdf
    - .hex
    - fir.c
    - fir.h
    - User
      - bram.v
      - user_proj_example.counter.v
    - Github link
- Your Github link should attach the file
  - Design, Synthesis report(Including FF, LUT, Bram), Waveform, simulation.log, makefile,…etc.
  - Report

Submission (2/2)

- Compress all above files in a single zip file named
  - StudentID_lab4-1.zip
- Submit to Submit to eeclass
- Deadline: **11/2 (Thu.) 23:59**
  - 20% off for the late submission penalty within 3 days

What is included in the report

- Explanation of your firmware code
  - How does it execute a multiplication in assembly code
  - What address allocate for user project and how many space is required to allocate to firmware code
- Interface between BRAM and wishbone
  - Waveform from xsim
  - FSM
- Synthesis report
- Other discoveries