Huangxu Chen

Personal Resume

Age: 21 years old

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Research Interests

- Soc architecture design
- High-performance computing circuit optimization
- Low power consumption circuit technology
- FPGA application development

Education

Sep 2020 - Present

South China University of technology — **Microelectronics Science and Engineering（Bachelor）**

Grade-Point Average: 3.68/4 (27/112)

Major courses: Analog Electronic Technology (90), Digital Electronic Technology (98), Signals and Systems (89), Digital Signal Processing (92), Integrated Design of Electronic systems (88), Verilog Design and FPGA (96), etc.

Publication

- Huangxu Chen, Mingjian Zhao, "Low Resource-Cost Depthwise Separable Convolutional Co-Processor Architecture", **International Conference on Electronic Information Engineering and Computer Science (EIECS)**, 2023.(Accepted)

Honor & Award

- The president of the Microelectronics Association in 2022
- The second prize of provincial Electronic Design Competition in 2021
- The third prize of provincial Embedded Design Competition in 2021
- The third prize of South China IC Innovation Competition in 2022
- The winner price of FPGA Innovation Competition in 2022
- The first prize of South China IC Innovation Competition in 2023
- The second prize of National IC Innovation Competition in 2023

Competition Experience

May 2021 - Sep 2021

2021 Embedded Design Competition — **Member**

- Competition content: Based on STM32H750 platform and RTthread operating system, deploy optimized lightweight neural network YOLO fastest for human target detection.This competition won the third prize in Guangdong Province.
- Responsible for: 1. Build the hardware platform of the whole system, complete the basic function of camera image display; 2. Deploy the neural network to the embedded C language project; 3. Design and code writing of the output decoding function of the neural network model and non-maximum suppression algorithm.

Jan 2022 - Aug 2022

2022 IC Innovation Competition — **Leader**

- Competition content: Build a fruit recognition system using the PGL22G FPGA development board of Unigroup Pango, and implement fruit detection and classification using the optimized YOLOV3tiny neural network.
- Responsible for: 1. Complete the training and testing process of neural network, reproduce the operation process of Yolov3tiny in matlab and python; 2. Adjust the structural parameters of neural network according to the hardware characteristics of FPGA; 3. Write output decoding circuit and non-maximum suppression state machine Verilog code.

Sep 2022 - Nov 2022

2022 FPGA Innovation Competition **Leader**

- Competition content: Using GW2A-18 FPGA development board, run Lenet5 CNN to realize image classification. This competition won the winning prize and won the FPGA development board presented by organizer.
- Responsible for: 1. Training and testing of neural network, and realizing the calculation process of Lenet5 neural network on matlab and python; 2. Writing Verilog code of convolutional circuit to realize image processing and feature extraction.

Jan 2023 - Aug 2023

2023 IC Innovation Competition **Member**

- Competition content: Optimize the microarchitecture of Hummingbird E203 processor, complete the expansion of floating point instruction set, and design an oscilloscope with spectrum display function based on floating point instruction.
- Responsible for: 1. Analyze the correlation of RAW data and the problem of write back blockage, optimize the microarchitecture design, and improve the efficiency of instruction execution; 2. Write the hardware circuit of part of floating point instruction set; 3. Write the hardware circuit of XADC peripheral and HDMI display.

Project experience

Dec 2021 - Jan 2023

EMG pattern recognition system based on FPGA **Leader**

- Project content: Using FPGA platform to build the EMG signal pattern recognition system, realize the EMG signal collection, preprocessing, feature extraction and classification recognition.
- Responsible for: 1. Design and test of the EMG signal acquisition circuit and filter circuit, the realization of communication between the FPGA and the ADC; 2. The realization of FPGA and the PC data communication and the results showed.

Jul 2022 - Nov 2022

One Life One Chip Project **Personal**

- Project content: 1. Able to use Chisel agile development language to generate verilog code, such as decoder,FIFO, decoupling IO and other circuit modules; 2. Able to use Verilator and GTKWave tools for circuit simulation and waveform analysis; Able to realize running simulation and waveform display based on makefile commands.

Dec 2022 - Feb 2023

MIPS five-stage pipeline processor design **Personal**

- Project content: 1. Learn and master the instruction set and operation mechanism of MIPS architecture; 2. Realize the various components of the processor, including instruction memory, data memory, control unit and five-stage pipeline.

Dec 2022 - Aug 2023

Hardware Acceleration Circuit for depthwise separable Convolution **Personal**

- Project content: 1. Design the multiplier multiplexing channel and AXI4 control module for depthwise separable convolution computation based on the DDR3 memory interface of the AXI4 protocol; 2. Support the configuration of the neural network through the AXI4-Lite interface; 3. High computational efficiency. When the neural network parameters are properly configured, the multiplier load rate reaches 93%;

Skills

Language ability: CET4 (481); CET6 (439);
Software mastery: 1. Master a variety of FPGA software use, such as **Vivado, Quartus, Pango, Gowin;** 2. Master the use of verilog simulation software such as **Modelsim, Vcs+Verdi, Verlitor+GTKWave;** 3. Master **Design Compile+Encounter** back-end software can complete the whole process of digital IC from verilog code to layout and post-simulation; 4. Master **python,C,matlab** programming languages, familiar with tensorflow and pytorch for neural network training and interface.
Team ability: 1. **Acted as a team leader for many times**, with rich experience in team formation and expansion, project management and coordination; 2. **Many times as the school's technical interpreter to share technical experience** in the competition, due to excellent technical level was elected as the president of the Microelectronics Association.