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Movidius MV0182 User Manual

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Revision History

Revision	Description	Author
1.0	First Internal Draft for review	David Nicholls
1.1	External release for MV0182-R2 PCB revision	David Nicholls
1.2	<p>Updated to include support for MV0182-R3 revision.</p> <p>Added section Differences Between MV0182-R2 and MV0182-R3 PCB Revisions</p> <p>Updated section Design Errata</p> <p>Added Figure 7: Identifying PCB Revision and Serial Number (MV0182-R3)</p> <p>Added Figure 5: MV0182-R3 PCB Bottom Overview</p> <p>Removed MIP RX2 from Figure 26: MV0182 MIPI Connections Example as this is non-functional in Myriad2 due to a silicon errata. Leaving it in the diagram could lead to confusion.</p> <p>Added section Daughtercard Compatibility Issues</p>	David Nicholls
1.3	<p>Added additional Errata item on USB clock component in section 11.1.8</p> <p>Clarified paths in section 12</p>	David Nicholls
1.4	Updated to included additional design Errata; PCB revision differences between R3 and R4 PCB revisions	David Nicholls
1.5	Formatting and layout edits. Corrected typos.	Daniel Grigoras
1.6	<p>Updated Errata after testing the MA2150 population option</p> <p>Specifically added section 11.1.14 MV0182-R2-14 in relation to the SD Card interface operation for designs populated with MA2150 silicon.</p> <p>Added section 1.10 Board Revisions with MA2100 or MA2150 to highlight the board revisions containing the new MA2150 silicon</p>	David Nicholls
1.7	<p>Updated documentation to support MV0182-R5 PCB revision</p> <p>Specifically updated section 1.2 added section 1.9; Updated chapter 2; updated sections 4.1.1 and chapter 7</p>	David Nicholls
1.8	Added Errata MV0182-R2-15	David Nicholls

1 Introduction

This document is the System Reference Manual for the MV0182 evaluation board. It provides detailed information on the overall design and usage of the MV0182 board. It is not intended to provide detailed documentation for Myriad 2 processor or any other component used on the board. It is expected that the user refers to the appropriate documents for these devices to access detailed information.

This revision of the System Reference Manual specifically refers only to the MV0182-R2,MV0182-R3,MV0182-R4 and MV0182-R5 PCB revisions¹.

For specific details on the software SDK released with the MV0182 platform, see the separate "MDK_GettingStarted.pdf" document in the release pack.

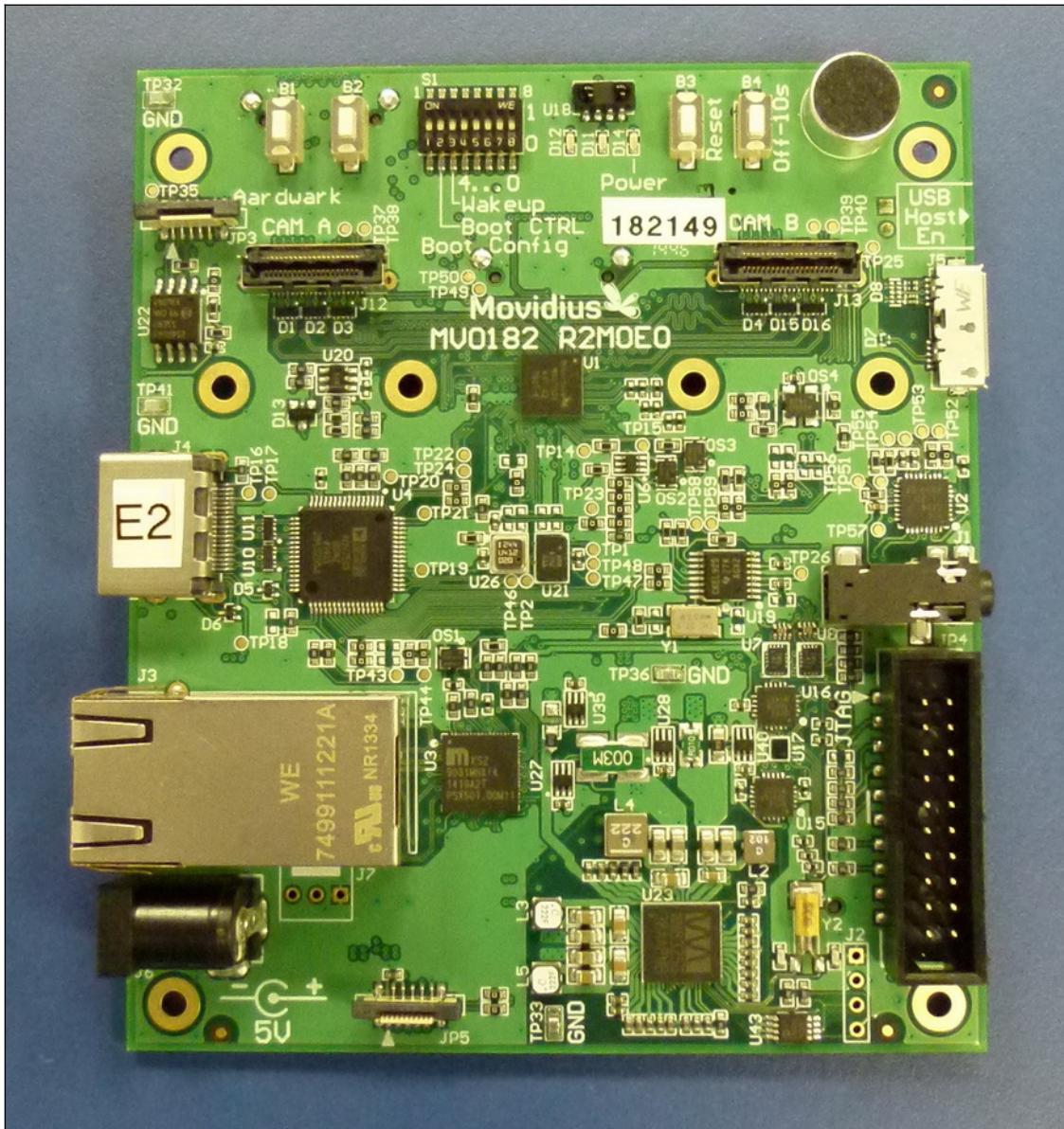


Figure 1: The MV0182 Development Board

¹ See section [1.6 Movidius PCB Revision System](#) for a details of the re visioning system

1.1 MV0182 Board Specification

This section covers the specifications of the MV0182 board and provides a high level description of the major components and interfaces that make up the MV0182 board.

1.2 Key Top-Level Features

	Feature
Processor	Myriad 2 Multicore processor with stacked 128MB LPDDR2 MA2100 – Board Revision <= MV0182-R4M0E0 MA2150 – Board Revision >= MV0182-R4M0E1
Boot Memory	8MB SPI Flash Memory (N25Q064A11ESE40G)
HDMI Video Output	ADV7513 HDMI Transmitter
PC Connectivity	USB 2.0 Device Interface (Note: USB 3.0 Micro-AB Connector, but compatible with USB 2.0 Micro) Gigabit Ethernet Port (Micrel KSZ9031MNX PHY)
Storage	SD Card/SDIO Expansion slot
User Interface	8 way DIP Switch for Boot Device Selection 2 User Push Buttons 2 User LEDs Reset Button Power Off Button
System Debug	20 Pin 0.1" ARM compatible JTAG Debug Connector 10 Pin FPC Aardvark (IIC/SPI) Debug Connector
System Power	Wolfson WM8325 Power Management IC 5V DC Power Supply Jack
Expansion Headers	40 Pin LCD & AP Expansion Port with support for 4 lane MIPI DSI / CSI-TX 40 Pin Camera_A Expansion Port with support for a single MIPI CSI-RX camera with up to 4 MIPI lanes 40 Pin Camera_B Expansion Port with support for up to two MIPI CSI-RX cameras of 2 lanes each Myriad2 Power Consumption Monitoring Expansion header for connecting a custom power measurement daughter-card.
Sensors	BMX_055 Gyroscope, Accelerometer and Magnetometer => PCB Rev R2,R3,R4 BMI160 Inertial Measurement Unit => PCB Rev R5 BMP_180 Pressure Sensor Infrared Remote Control Sensor
Audio	On board Microphone, Mono Audio input jack and Stereo Audio output jack

Table 1: Key Top Level Features

1.3 Top-Level Block Diagram

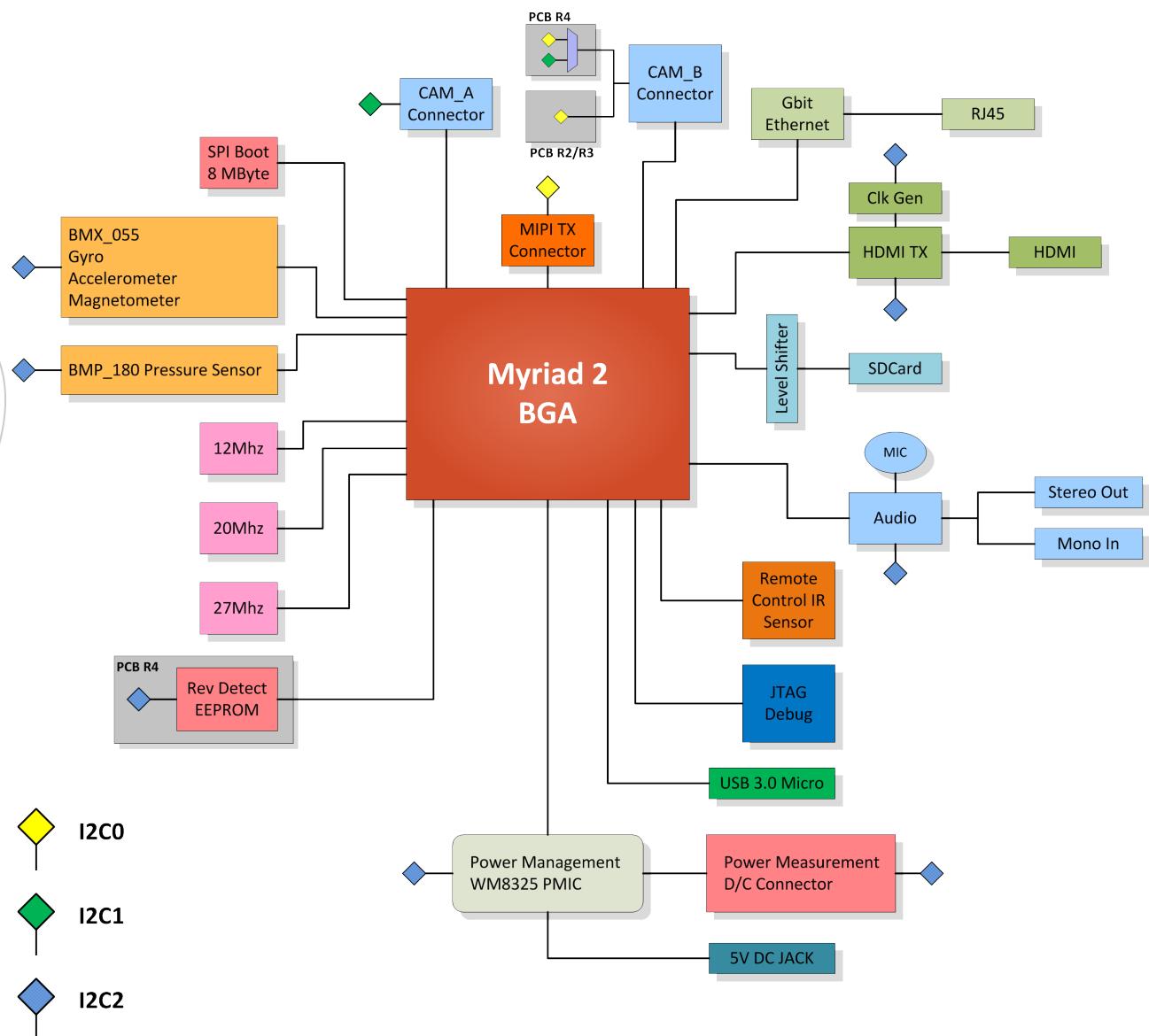


Figure 2: MV0182 System Block Diagram

1.4 PCB Overview

This section illustrates the location of the key system features on the PCB.

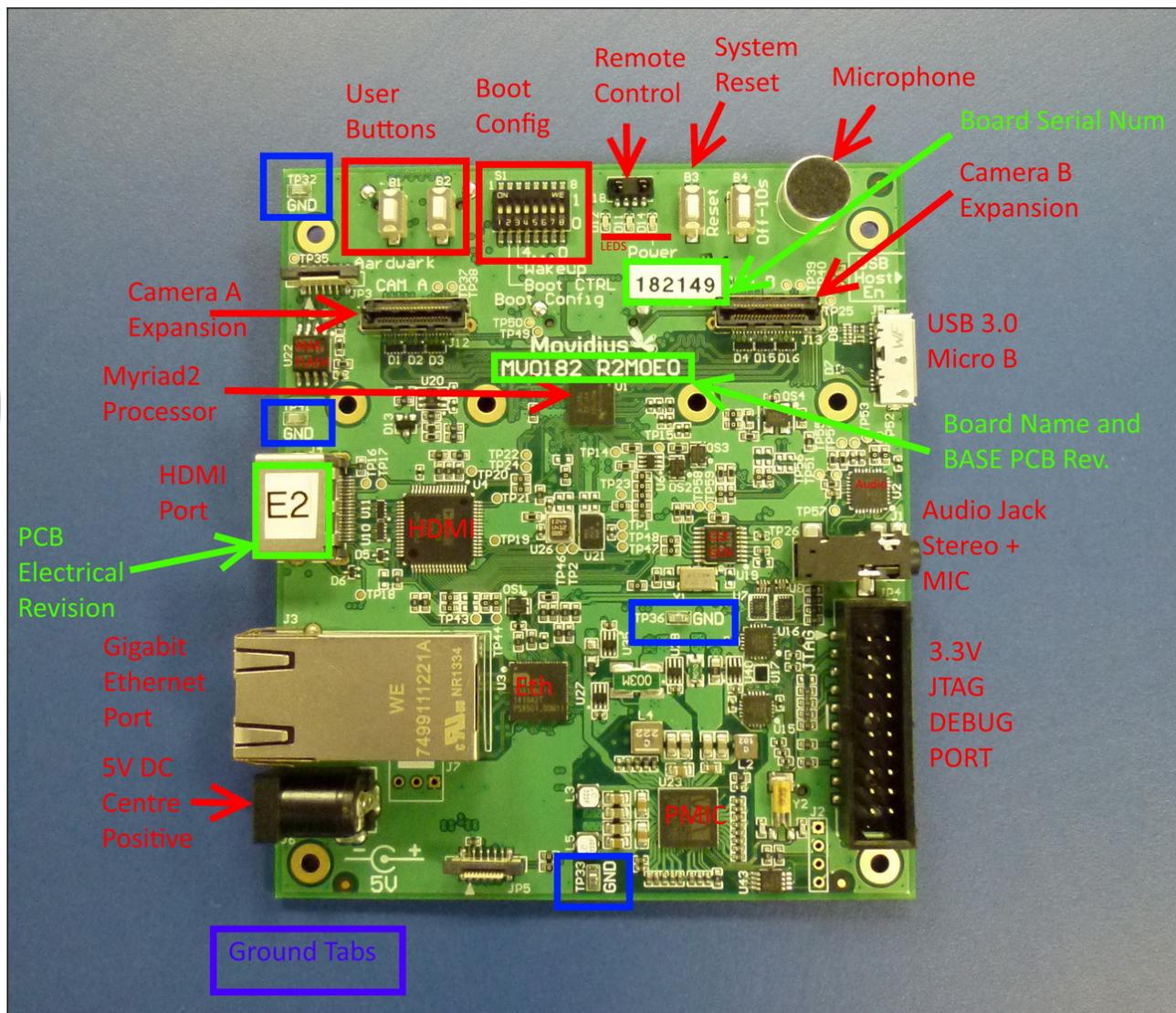


Figure 3: PCB Top Overview

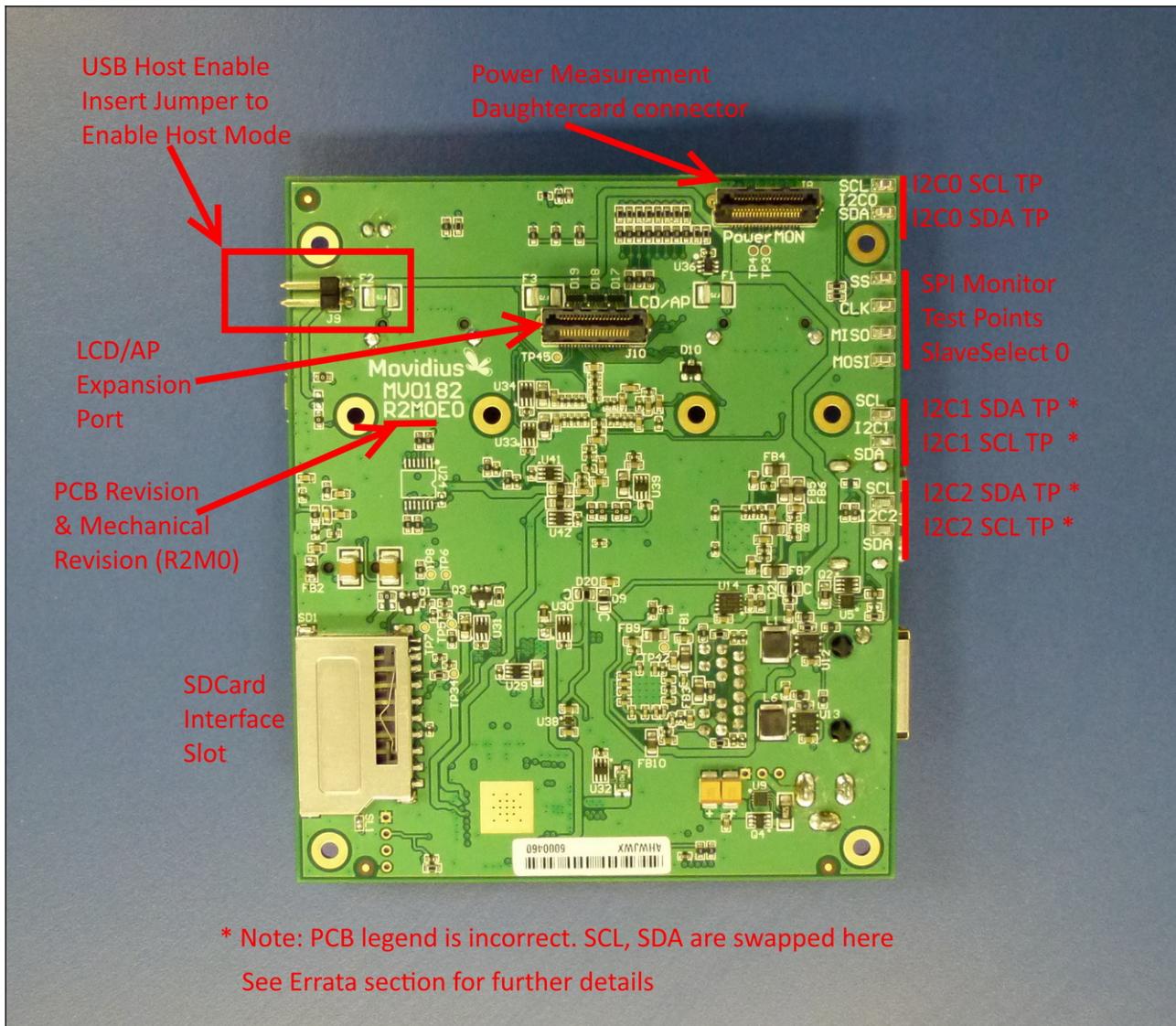


Figure 4: MV0182-R2 PCB Bottom Overview

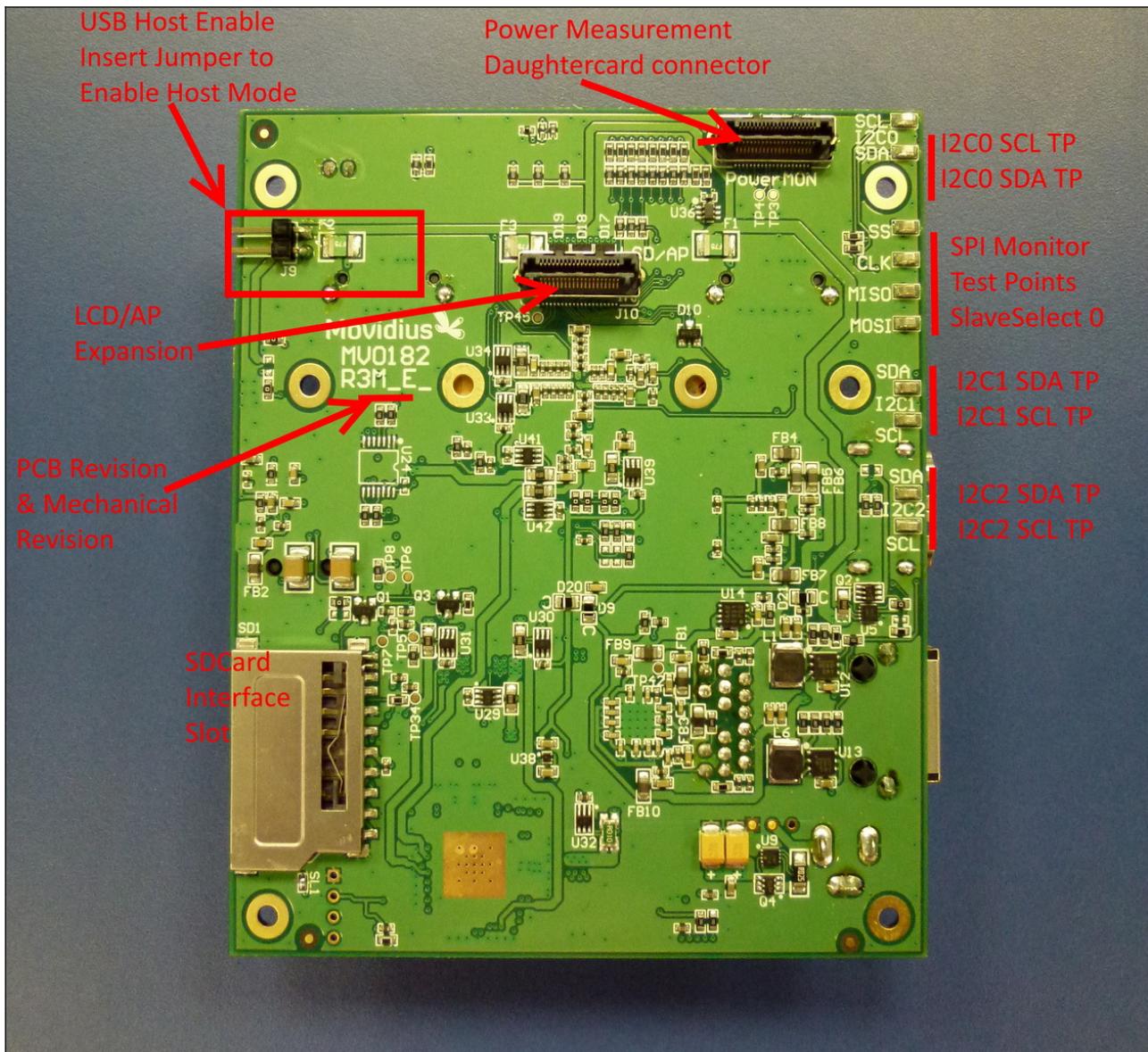


Figure 5: MV0182-R3 PCB Bottom Overview

1.5 Daughtercard Connections

The three daughtercard connections on the PCB use a common connector type. However, it is important to note that this does not imply that daughtercards are compatible between the different expansion ports.

Some specific camera daughtercards may be designed to be compatible between the CAM_A and CAM_B interfaces, but as a general rule daughtercards are designed specifically for the intended expansion port.

Users must take care to ensure that daughtercards are only attached to the intended expansion port. There are no physical interlocks in the design to prevent incorrect daughtercard attachments.

1.6 Movidius PCB Revision System

This section is intended to allow the user to correctly identify the MV0182 board revision and serial number. The Movidius board revision system is comprised of three components as follows:

Field	Description
RX	PCB Revision Number. Directly relates to the Printed Circuit Board. Any design change to the PCB will result in an increment of this field
MX	Mechanical Revision Number. This relates to a component change which changes the mechanical characteristics of the board. Example: Changing a pin header to a shrouded header would increment this field.
EX	Electrical Revision Number. This reflects any electrical modification to the design which does not involve a PCB change. Examples: Changing resistor values, or green wire modification of an existing design.

Table 2: PCB Revision Numbering System

All designs start at **R0M0E0** and increment fields as necessary from there.

The PCB silkscreen will contain the base revision for the PCB and supplemental labels are used thereafter to increase the MX or EX fields.

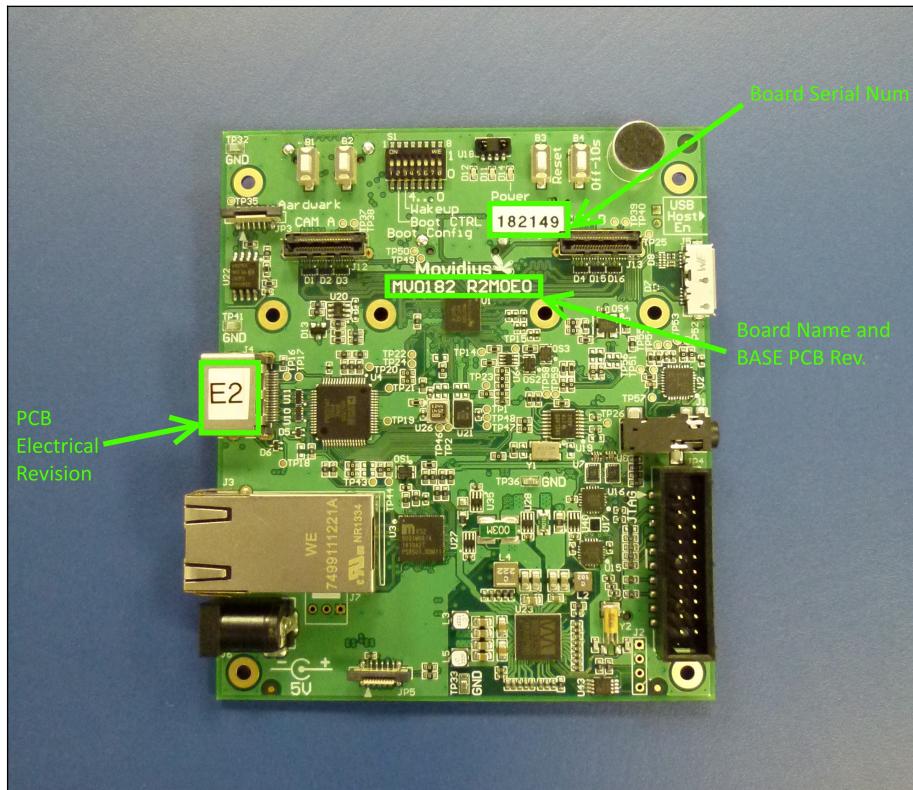


Figure 6: Identifying PCB Revision and Serial Number (MV0182-R2)

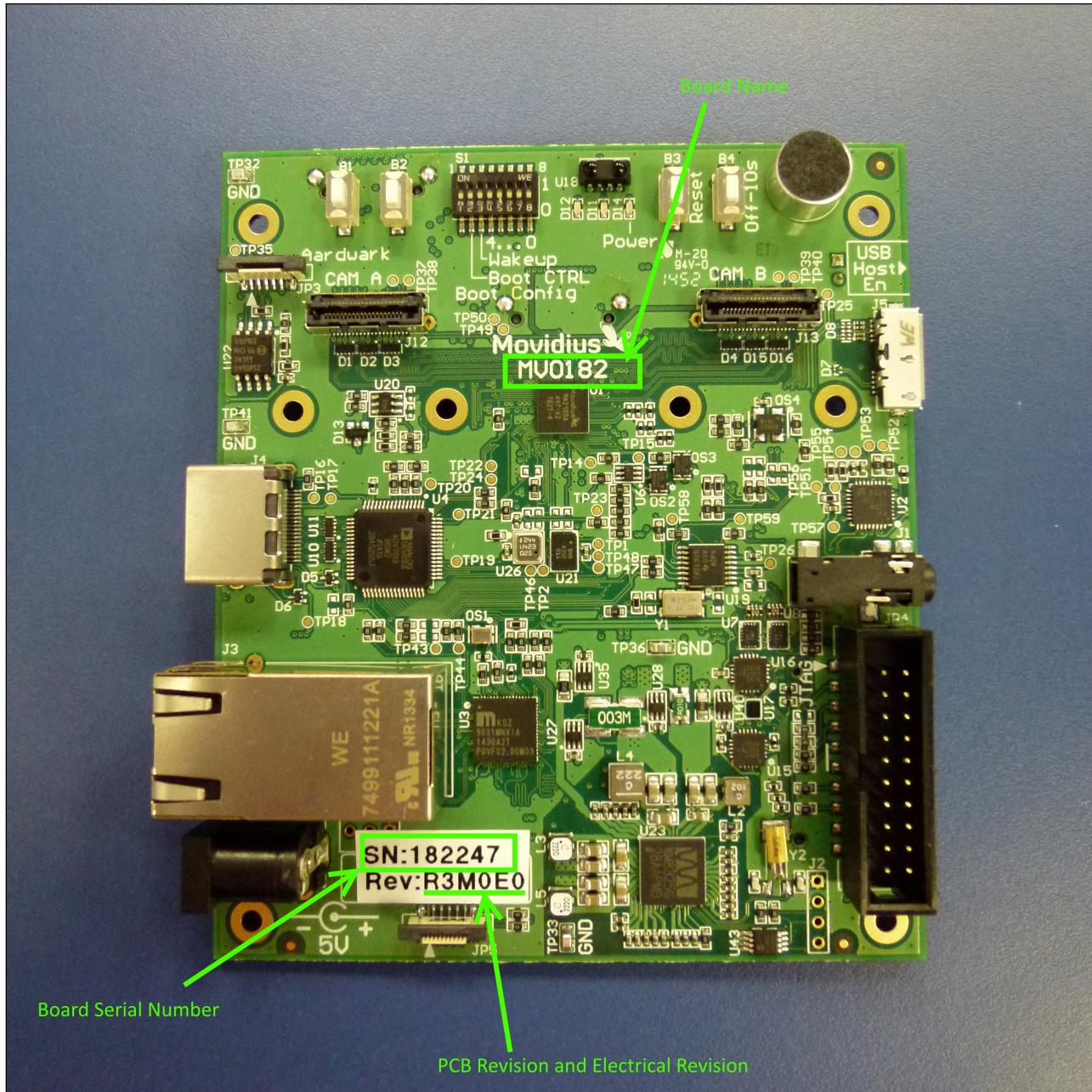


Figure 7: Identifying PCB Revision and Serial Number (MV0182-R3)

1.7 Differences Between MV0182-R2 and MV0182-R3 PCB Revisions

This section describes the key changes between the R2 and R3 PCB revisions of the MV0182 evaluation board.

1.7.1 BMX_055(U21) and TLV320AIC3204(U2) I2C Address Fixes

- Corrected design errata [MV0182-R2-3](#)
- This modification adds support for the TLV320AIC3204 Audio code which was not possible on MV0182-R2
- This update creates a functional change between R2 and R3 revisions of MV0182 a
- I2C Address Changes as follows

Device	Function	Rev R2 7-Bit I2C Address	Rev R3 7-Bit I2C Address
BMX_055	Accelerometer	0x18	0x19
BMX_055	Gyroscope	0x68	0x68
BMX_055	Magnetometer	0x10	0x11
TLV320AIC3204	Audio DAC	0x18 (Not Accessible on R2)	0x18

1.7.2 BMP180 (U26) I2C Connection Fix

- Corrected design errata [MV0182-R2-3](#) by swapping SDA/SCL connections
- This update is functionally equivalent to MV0182-R2M0E1/E2 revisions

1.7.3 MP2012DQ(U12,U13) Regulation Fix

- Corrected design errata [MV0182-R2-4](#)
- Improved regulation output of U12, U13 by making the following changes
 - U12
 - Added 100 K feedback resistor R85
 - Added 10 µF additional capacitance C129
 - U13
 - Added 100 K feedback resistor R86
 - Added 10 µF additional capacitance C130

1.7.4 CDCEL925(U19) Clock Outputs Fix

- Corrected design errata [MV0182-R2-5](#) by using clock outputs Y4,Y5 to feed CAM_A and CAM_B respectively
- This update is functionally equivalent to MV0182-R2M0E2 revisions

1.7.5 PCB Silkscreen error on I2C1/I2C2 Testpoints

- Corrected design errata [MV0182-R2-6](#)
- The silkscreen descriptions of the I2C testpoints are correct on MV0182-R3



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1.7.6 Length Matched the GMII data signals for KSZ9031MNX Ethernet device.

- On the MV0182-R3 PCB revision the GMII datasignals have been length matched.

1.7.7 WM8325(U23) Footprint adjustment

- Corrected design errata [MV0182-R2-7](#)
- This footprint has been modified for the MV0182-R3 to correct the alignment issue.

1.8 Differences Between MV0182-R3 and MV0182-R4 PCB Revisions

1.8.1 USB Reference Oscillator Component Change

- Corrected design errata [MV0182-R2-8](#)
- Updated OS4 to Abraccon ASDMB-20.000MHZ-LC-T

1.8.2 USB Oscillator Resistor Divider Change

- Corrected design errata [MV0182-R2-9](#)
- See errata notes for details of the motivation for this change
- Updated values of R156 (240R) and R189 (187R)

1.8.3 Updated Auto-on circuit

- Corrected design errata [MV0182-R2-10](#)
- See errata notes for full details of this change
- R38 now pulled up to 1.8VLDO0 instead of 1.8VDC4

1.8.4 Corrected connection of VDDCV shunt resistance

- Corrected design errata [MV0182-R2-11](#)
- Fixed connections to 4 wire resistor so that the measurement is genuinely 4 wire in nature
- See errata notes for full details of this change

1.8.5 Component Change for Regulator U38

- Corrected design errata [MV0182-R2-12](#)
- Component U38 was changed from LD6805K/33P to TLV70033DCKT
- This change was made purely to optimize the manufacturing process as the original part footprint was very small and was proving quite difficult to solder reliably.

1.8.6 Added Revision detect EEPROM (U45)

- This is a new feature for MV0182-R4 which provides a software addressable EEPROM that can be used for PCB revision detection. (Part Number: Microchip 24AA32A-I/MS)
- Existing mechanisms (Pre-R4) for detecting PCB revision differences relied on software detecting differences in the board behavior. This mechanism is not ideal and in particular is not very future proof.
- As of revision R4 software has the potential to detect PCB revision by querying this EEPROM on I2C 7 bit address 0x50 to determine the PCB revision.
- Revisions prior to R4 must still be determined using the per-existing mechanisms.
- Note: PCB revision detection is handled transparently by the MV0182 board driver in the MDK

1.8.7 Added feature to support choice of I2C bus for Camera B

- One of the use-cases for this platform is a configuration option where

- CAM_B is connected to dual 2 lane cameras
- LCD/AP connector is used with MV0191 to connect to a dragon board
- In this use case it is often convenient in the Android software to have the MV0182 board model a camera. To do this, the most convenient option is to use the I2C0 bus on the LCD/AP connector in a mode where the Dragon board is master and the MV0182 is slave.
- From a software perspective the MV0182 now looks like a MIPI camera sensor with an I2C control interface, just like many regular sensors.
- The problem with this configuration, is that the I2C0 bus is also shared with the CAM_B connector and is normally used to configure the camera sensors on the CAM_B daughtercard. As such there is a direct conflict between the two desired uses of the I2C bus.
- The normal solution to this problem is to modify the Android software to use the SPI interface as the control interface for the MV0182 and reserve I2C0 for CAM_B. This avoids the problem but does create slightly more work on the Android host side. This method remains the recommended solution to this problem for use-cases that incur the conflict.
- However as of MV0182-R4 there is a new hardware feature which gives the software developer slightly more flexibility in dealing with this potential problem.
- In this revision a mux has been added to the CAM_VB I2C connections which allows the user to select via software control, either I2C0 (default) or I2C1 for the CAM_B I2C interface.
- The mux is controlled using the WM8325 PMIC GPIO#3 and the default behavior in the absence of any software changes is to select I2C0 (i.e. directly backwards compatible with previous revisions)
- This change has two collateral implications as follows:
 - WM_SW1 (DIP Switch 1) is no longer connected to PMIC_GPIO#3
 - This DIP switch is thus no longer accessible by software and it is recommended that it is not used in any application to avoid any compatibility issues between boards
 - PMIC_GPIO#3 is now reserved for I2C bus selection of CAM_B interface (previously WM_SW1)
 - PMIC_GPIO#3 LO => CAM_B uses I2C0 – Default and compatible with R2/R3
 - PMIC_GPIO#3 HI => CAM_B uses I2C1 – New option to share I2C bus with CAM_A

NOTE: It is important to note that the recommended approach in software is still to use SPI communications for control of MV0182. This provides maximum compatibility and doesn't create any risk of additional I2C conflicts with the CAM_A connector. This mode of operation should be reserved strictly for limited usecases where software alternatives are not possible.

NOTE: For example if using the shipping MV0200/MV0201 daughtercards connected to CAM_A/CAM_B; selecting this alternative I2C connection for CAM_B creates an I2C address conflict between the IMX214 and IMX208 sensors where both parts share the same I2C 7-bit addresses 0x10 & 0x14.

1.8.7.1 Implementation Details of CAM_B I2C Bus Mux

- This feature is implemented by the addition of U37 and U44 of Schematic page 4
- The mux selection is handled by connecting CAM_B_I2C_SEL to PMIC_GPIO#3 via RZ50 on schematic page 13
- In the absence of any software, PMIC_GPIO#3 is high-Z and the net is pulled low by R90 (P4)

1.8.8 Updates to support MA2150 or MA2100 on the same PCB

- There are a number of changes to the MV0182-R4 design to provide forwards compatibility with the new Myriad MA2150 device footprint.
- These changes are fully discussed in the following chapter [Support for MA2100 and MA2150 \(PCB Revision R4 Only\)](#)

1.9 Differences Between MV0182-R4 and MV0182-R5 PCB Revisions

1.9.1 Support for MA2100 population Removed

MV0182-R4 PCB revision was designed to allow population of either MA2100 or MA2150 silicon. The intention here was to demonstrate how board designs could be adopted from MA2100 to MA2150. As of MV0182-R5 support for MA2100 silicon has been deprecated on the platform.

As such, the details in chapter 2, “[Support for MA2100 and MA2150 \(PCB Revision R4 Only\)](#)”, does not apply to this PCB revision and the board is designed to directly support MA2150.

1.9.2 Change reference IMU from BMX-055 to BMI-160

As of MV0182-R5 the default IMU on the platform has been changed from BMX-055 to BMI-160

1.9.3 USB 3.0 Connector changed from Micro-B to Micro-AB

The USB connector has been changed to a Micro-AB connector. The intention here is to future proof the design for potential use cases where the USB host functionality might be used. USB Micro-AB receptacles are compatible with both USB Micro-B plugs for the use-case where MV0182 is the USB device and also with USB Micro-A plugs for the use-case where MV0182 is the USB host. Note: Host functionality also requires the connection of Jumper J9 and is not hot switchable. Also USB host functionality is dependent on the availability of a suitable USB host software stack.

1.9.4 USB compatibility changes

- 10uF capacitor (C127) added to USB-VBUS signal to ensure compliance with USB specification inrush current requirements.
- Added R40 10K bleed resistor for C127
- Added R84 1K resistor so that usb_vbus sense isn't directly connected to the VBUS pin
- USB 3.0 ESD protection diodes D7, D8 are now populated.

1.9.5 SD Card Changes to Support MA2150 Only Design

In PCB revisions MV0182-R4 and earlier, the SD Card design required the use of a 3.3V level shifter in order to deal with the I/O voltage requirements of MA2100. The MA2150 SoC now has an independent supply rail (VDDIO_B) which allows GPIOs 16-21 to be configured between 3.3V and 1.8V to support direct interface to SD Cards.

As MV0182-R5 no longer supports MA2100 it was possible to remove the level shifter and associated circuitry. The new SD Card design is simply a direct connection to the Myriad processor.

In addition a switch has been added to allow the direct control of the SD Card 3.3V power rail from Myriad. GPIO_57 has been re purposed (Previously BMX055_INT3)

When GPIO_57 is high impedance or driven low the SD Card will be powered. When GPIO_57 is driven high the SD Card power is cut. LED D22 has also been added to the design and is illuminated when the SD Card is powered.



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1.9.6 Workaround for MV0200 Compatibility Issue

Chapter [11.2 Daughtercard Compatibility Issues](#) describes a problem where some common pins are shared between the daughtercard control signals and the boot configuration GPIOS. This contravenes the limitations described in chapter [10.2 Common I/O Bus Description](#).

In order to workaround this issue and to increase the flexibility of the design some additional logic has been added in the MV0182-R5 PCB design which isolates the COM_IO bus pins during the rising edge of system reset. This prevents daughtercard use of the COM_IO bus from interfering with the boot mode selection process as the boot configuration is only sampled on the rising edge of reset.

1.10 Board Revisions with MA2100 or MA2150

MV0182-R4 PCB revision supports either MA2100 or MA2150 depending on population option. (see Section: [Support for MA2100 and MA2150 \(PCB Revision R4 Only\)](#))

To know which processor is present you need to look at the Electrical revision (EX) of the PCB as follows

Revision	Processor
MV0182-R4M0E0 or Earlier	MA2100
MV0182-R4M0E1 or Later	MA2150

2 Support for MA2100 and MA2150 (PCB Revision R4 Only)

The MV0182 PCB was designed initially to support the MA2100 processor, and MV0182 PCB revisions R2,R3 only support MA2100. MV0182 PCB revision R4 was designed to support both IC versions MA2100 and MA2150 using the same PCB. PCB revisions R5 and later only support MA2150.

This chapter specifically deals with the R4 revision which supports both processors. While MA2100 and MA2150 don't share the same footprint, their footprints are designed to be closely matched, so that designers have the option to build PCBs which can accommodate both parts with only minimal component population changes.

This section aims to describe these changes and explain the component population differences.

NOTE: This chapter is only relevant to users for MV0182-R4 PCB revisions or those who are attempting to re-design their own boards to support both MA2100 and MA2150. If you are have a PCB revision other than R4 you should skip this chapter.

2.1 Footprint differences between MA2100 and MA2150

2.1.1 Power Rails VDDCV and VDDCC are internally connected

In MA2100 it was necessary to supply VDDCC and VDDCV from independent supply rails as the supported voltage range for VDDCC was not as wide as the supported voltage range for VDDCV.

This limitation is no longer present in MA2150 and VDDCC and VDDCV are actually connected to the same power net within with MA2150 package. For consistency, the package ball names retain the same naming conventions of VDDCC and VDDCV but it is important to understand that in reality they now represent the same power rail.

For this reason on MA2150 designs it is no longer advisable to supply VDDCC and VDDCV from independent power sources and in practice both VDDCC and VDDCV should be supplied from a common power net

2.1.2 New DDR calibration resistor ball DRAM_ZQ_EXT

In MA2100, there is a DRAM calibration resistor connection (DRAM_ZQ) on BGA ball H12.

This ZQ calibration resistor is used as a reference point for the internal impedance matching of the DDR interface. Both the Myriad IC DDR_Phys and the integrated Micron DDR die have a need to perform ZQ calibration in order to achieve the correct impedance levels. However on MA2100 both devices share a common ZQ calibration resistor (DRAM_ZQ). This limitation creates additional complexity in the DDR driver, in order to manage this shared resource.

In MA2150 this complication has been resolved by adding a new connection in the package (DRAM_ZQ_EXT) so that the DDR die has an independent ZQ calibration resistor dedicated for its own use.

In order to achieve this additional connection, one of the VSS Balls (J12) has been re-assigned to the function DRAM_ZQ_EXT on MA2150.

In practice this means that designs which need to support MA2100 and MA2150 should:

- MA2100 => J12 connected to GND
- MA2150 => J12 connected to GND via a 240R 1% resistor

2.1.3 New VDDIO Rail for SDIO to support both 1.8V and 3.3V I/O levels

In MA2100 there is a single VDDIO rail which is nominally 1.8V. This creates a particular challenge in the use-case where MA2100 is connected to an SD Card as the SD Card standard requires that cards initially

communicate using 3.3V I/O levels. While it is possible to work around this problem using a custom bidirectional level shifter IC, this creates a new limitation as these devices are typically limited in the maximum SDCLK frequency supported. Furthermore the mandatory use of a level shifter increases the BOM cost of any product using MA2100 with an SD interface.

This limitation is resolved in MA2150 by creating a new independent I/O power rail called VDDIO_B.

This rail is used to provide the I/O voltage to a very limited subset of GPIOs as follows:

GPIO	I/O Rail	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Mode 5
gpio_16	VDDIO_B	cam_data12	eth_125_ref_i	lcd_data_24	sd_hst1_dat_3	spi0_ss_0	lcd_data_13
gpio_17	VDDIO_B	cam_data13	eth_tx_clk	lcd_data_25	sd_hst1_clk	spi0_sclk_out	lcd_data_14
gpio_18	VDDIO_B	cam_data14	eth_tx_en	lcd_data_26	sd_hst1_cmd	spi0_mosi	lcd_data_15
gpio_19	VDDIO_B	cam_data15	eth_tx_err	lcd_data_27	sd_hst1_dat_0	spi0_miso	lcd_data_16
gpio_20	VDDIO_B	cam_data16	eth_rx_clk	lcd_data_28	sd_hst1_dat_1	i2c0_scl	lcd_data_17
gpio_21	VDDIO_B	cam_data17	eth_rx_dv	lcd_data_29	sd_hst1_dat_2	i2c0_sda	lcd_data_18

Table 3: Subset of GPIOs powered from VDDIO_B in MA2150

The table above illustrates that GPIOs 16-21 inclusive are supplied from VDDIO_B in MA2150 whereas all other GPIOs are powered from VDDIO. This allows for independent control of the I/O voltage on these 6 pins and is particularly intended for their use in MODE3 where they function as an SDHost interface.

The anticipated operation is that a user would select these GPIOs for their SDHost interface and supply VDDIO_B with 3.3V by default. In the SDCard software it is then possible to renegotiate with a connected card to request higher speed operation but at a 1.8V I/O level. While performing this switchover it is possible for software running on MA2150 to request that the external regulator supplying VDDIO_B switch from 3.3V to 1.8V, thereby achieving both 3.3V and 1.8V operational modes without the need for an external level shifter.

It is important to point out that the SDHost interface is also accessible via different GPIO ranges (e.g. GPIO_46-51) but all of these alternative SDHost pinouts are connected to the primary VDDIO rail (VDDIO) and thus don't support this new feature of configurable voltage operation. Designers who want to take advantage of the flexibility added by the VDDIO_B rail need to ensure that they select the SD_Host interface on GPIOs 16-21.

In order to facilitate the new power pin VDDIO_B, BGA ball E9 has been re-purposed on MA2150 from VSS on MA2100 to VDDIO_B on MA2150

In practice this means that designs which need to support MA2100 and MA2150 should:

- MA2100 => E9 connected to GND
- MA2150 => E9 connected to suitable I/O rail voltage, either 1.8V or 3.3V or configurable for SDIO.

2.2 MA2100 vs MA2150 footprint comparison

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	MIPI_DP4	MIPI_DN5	MIPI_DPS	MIPI_DN6	MIPI_DP6	MIPI_DN7	MIPI_DP7	usb_rx0_p	usb_rx0_n	usb_tx0_p	usb_tx0_n	usb_dp	usb_dn	GPIO_26	GPIO_19
B	MIPI_DN4	GPIO_53	GPIO_49	GPIO_48	GPIO_54	GPIO_47	GPIO_55	GPIO_45	GPIO_50	GPIO_51	GPIO_52	usb_ref_clk_p	usb_ref_clk_n	GPIO_40	GPIO_42
C	MIPI_C2	MIPI_C3	MIPI_CP4	MIPI_C5	MIPI_DN10	MIPI_DP10	MIPI_DN11	MIPI_DP11	MIPI_REXT5	GPIO_46	GPIO_56	GPIO_15	GPIO_16	GPIO_41	GPIO_25
D	MIPI_CN2	MIPI_CN3	MIPI_CN4	MIPI_CNS	MIPI_REXT1	MIPI_REXT2	MIPI_REXT3	MIPI_REXT4	usb_resref	usb_id	usb_vbus	usb_vp_VDD	usb_vdd330	GPIO_9	GPIO_14
E	MIPI_C1	MIPI_CPO	MIPI_REXT0	MIPI_VDD	MIPI_VDD	DRAM_MVDDA	VDDIO	VDDIO	VSSIO	VSSIO	VSSC	usb_VSS	PLL_AVDD	GPIO_44	GPIO_43
F	MIPI_CN1	MIPI_CNO	MIPI_DP9	MIPI_VDD	MIPI_VDD	DRAM_VDD1	VDDIO	VDDIO	VSSIO	VSSIO	VSSC	VSSC	PLL_AVSS	GPIO_11	GPIO_10
G	MIPI_DP3	GPIO_2	MIPI_DN9	MIPI_VSS	DRAM_MVDDQ	DRAM_MVDDQ	VDDCV	VDDCV	VSSC	VSSC	VSSC	test_enable	wake_up	osc2_j	osc1_j
H	MIPI_DN3	GPIO_4	MIPI_DP8	MIPI_VSS	DRAM_MVDDQ	DRAM_MVDDQ	VDDCV	VDDCV	VDDCV	VSSC	VSSC	DRAM_ZQ	GPIO_13	osc2_o	osc1_o
J	MIPI_DP2	GPIO_6	MIPI_DN8	MIPI_VSS	MIPI_VSS	DRAM_MVDDQ	VDDCV	VDDCV	VDDCV	VSSC	VSSC	VSSC	GPIO_18	GPIO_12	ref_clk
K	MIPI_DN2	GPIO_8	DRAM_VSS	DRAM_VSS	DRAM_VSS	DRAM_VDD2	DRAM_VDD2	VDDCV	VDDCC	VDDCC	VSSC	VSSC	GPIO_32	GPIO_17	reset
L	MIPI_DP1	GPIO_64	DRAM_VSS	DRAM_VSS	DRAM_VSS	DRAM_VDD2	DRAM_VDD2	VDDCV	VDDCC	VDDCC	VSSC	VSSC	GPIO_21	GPIO_20	GPIO_33
M	MIPI_DN1	GPIO_66	GPIO_68	trst	tck	tdi	DRAM_VDDQ	VDDCR	VDDCC	VDDCC	VSSC	efuse_vddq	GPIO_23	GPIO_22	GPIO_34
N	MIPI_DPO	GPIO_0	GPIO_7	GPIO_65	tms	tdo	GPIO_38	GPIO_30	GPIO_39	GPIO_31	GPIO_35	GPIO_24	GPIO_29	GPIO_37	GPIO_28
P	MIPI_DNO	GPIO_71	GPIO_72	GPIO_58	GPIO_73	GPIO_60	GPIO_3	GPIO_61	GPIO_70	GPIO_82	GPIO_83	GPIO_77	GPIO_78	GPIO_27	GPIO_36
R	GPIO_5	GPIO_67	GPIO_57	GPIO_74	GPIO_59	GPIO_75	GPIO_69	GPIO_76	GPIO_80	GPIO_81	GPIO_79	GPIO_62	GPIO_63	GPIO_1	GPIO_84

Figure 8: MA2100 Ballout, highlighting the Balls that change function in MA2150

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	MIPLDP4	MIPLDN5	MIPLDP5	MIPLDN6	MIPLDP6	MIPLDN7	MIPLDP7	usb_rx0_p	usb_rx0_n	usb_tx0_p	usb_tx0_n	usb_dp	usb_dn	GPIO_26	GPIO_19
B	MIPLDN4	GPIO_53	GPIO_49	GPIO_48	GPIO_54	GPIO_47	GPIO_55	GPIO_45	GPIO_50	GPIO_51	GPIO_52	usb_ref_clk_p	usb_ref_clk_n	GPIO_40	GPIO_42
C	MIPLCP2	MIPLCP3	MIPLCP4	MIPLCP5	MIPLDN10	MIPLDP10	MIPLDN11	MIPLDP11	MIPLREXT5	GPIO_48	GPIO_56	GPIO_15	GPIO_16	GPIO_41	GPIO_25
D	MIPLCN2	MIPLCN3	MIPLCN4	MIPLCN5	MIPLREXT1	MIPLREXT2	MIPLREXT3	MIPLREXT4	usb_resref	usb_id	usb_vbus	usb_vp_VDD	usb_vdd330	GPIO_9	GPIO_14
E	MIPLCP1	MIPLCP0	MIPLREXT0	MIPLVDD	MIPLVDD	DRAM_MVDDA	VDDIO	VDDIO	VDDIO_8	VSSIO	VSSC	usb_VSS	PLL_AVDD	GPIO_44	GPIO_43
F	MIPLCN1	MIPLCN0	MIPLDP9	MIPLVDD	MIPLVDD	DRAM_VDD1	VDDIO	VDDIO	VSSIO	VSSIO	VSSC	VSSC	PLL_AVSS	GPIO_11	GPIO_10
G	MIPLDP3	GPIO_2	MIPLDN9	MIPLVSS	DRAM_MVDDQ	DRAM_MVDDQ	VDDCV	VDDCV	VSSC	VSSC	VSSC	test_enable	wake_up	osc2_j	osc1_j
H	MIPLDN3	GPIO_4	MIPLDP8	MIPLVSS	DRAM_MVDDQ	DRAM_MVDDQ	VDDCV	VDDCV	VDDCV	VSSC	VSSC	DRAM_ZQ	GPIO_13	osc2_o	osc1_o
J	MIPLDP2	GPIO_6	MIPLDN8	MIPLVSS	DRAM_MVDDQ	VDDCV	VDDCV	VDDCV	VDDCV	VSSC	VSSC	DRAM_ZQ_EXT	GPIO_16	GPIO_12	ref_clk
K	MIPLDN2	GPIO_8	DRAM_VSS	DRAM_VSS	DRAM_VSS	DRAM_VDD2	DRAM_VDD2	VDDCV	VDDCC	VDDCC	VSSC	VSSC	GPIO_32	GPIO_17	reset
L	MIPLDP1	GPIO_64	DRAM_VSS	DRAM_VSS	DRAM_VSS	DRAM_VDD2	DRAM_VDD2	VDDCV	VDDCC	VDDCC	VSSC	VSSC	GPIO_21	GPIO_20	GPIO_33
M	MIPLDN1	GPIO_66	GPIO_68	trst	tck	tdi	DRAM_VDDQ	VDDCR	VDDCC	VDDCC	VSSC	efuse_vddq	GPIO_23	GPIO_22	GPIO_34
N	MIPLDPO	GPIO_71	GPIO_72	GPIO_58	GPIO_73	GPIO_60	GPIO_3	GPIO_61	GPIO_70	GPIO_82	GPIO_83	GPIO_77	GPIO_78	GPIO_27	GPIO_36
P	MIPLDNO	GPIO_71	GPIO_72	GPIO_58	GPIO_73	GPIO_60	GPIO_3	GPIO_61	GPIO_70	GPIO_82	GPIO_83	GPIO_77	GPIO_78	GPIO_27	GPIO_36
R	GPIO_5	GPIO_67	GPIO_57	GPIO_74	GPIO_59	GPIO_75	GPIO_69	GPIO_76	GPIO_80	GPIO_81	GPIO_79	GPIO_62	GPIO_63	GPIO_1	GPIO_84

VDDCV and VDDCC share a common rail within MA2150

Figure 9: MA2150 Ballout, highlighting changes

2.3 MV0182 Schematic Changes to support both MA2100 and MA2150 footprints

2.3.1 Support for common VDDCV/VDDCC Rail on MA2150

To support this feature of MA2150 the MV0182-R4 PCB was modified to include RZ51 which connects the VDDCV and VDDCC rails on the design.

When the design is used with an MA2100 part RZ51 is not mounted and the PMIC is configured to drive both VDDCV and VDDCC independently.

When MA2150 is populated, RZ51 is mounted so that VDDCC is supplied from VDDCV and R170 is not mounted so as to disconnect 0.9VDC1

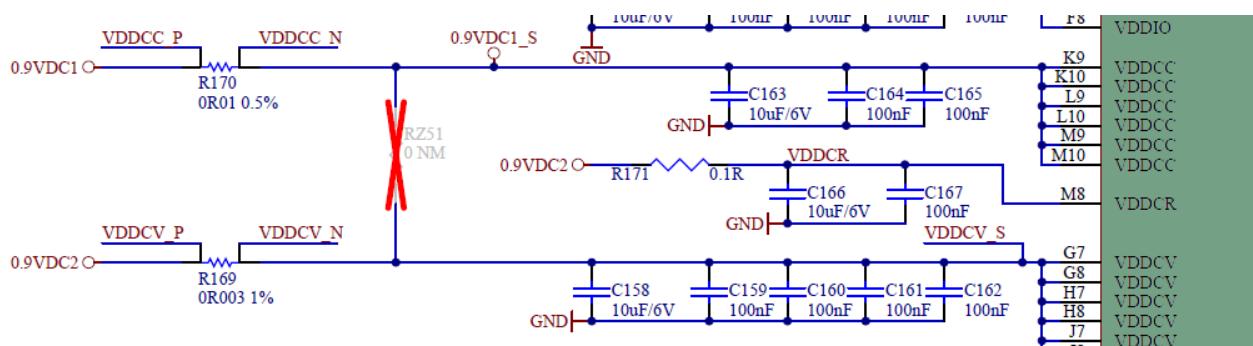


Figure 10: MA2100 Population Option VDDCV/CC

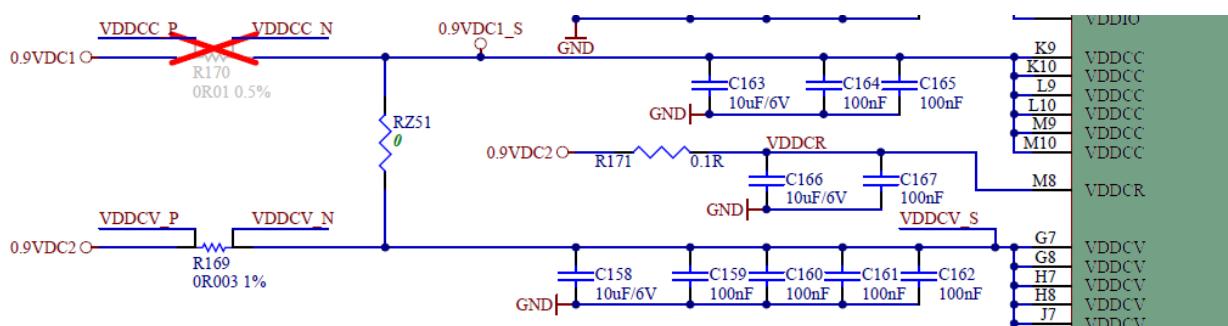


Figure 11: MA2150 Population Option VDDCV/CC

2.3.2 Support for DRAM_ZQ_EXT on MA2150

To support this feature of MA2150 a resistor R87 was added between BGA Ball J12 and GND.

When MA2100 is populated R87 is mounted with a zero ohm link to correctly supply this ball with VSS.

When MA2150 is populated R87 is mounted with a 240R 1% resistor so that the ball can be used for ZQ calibration.

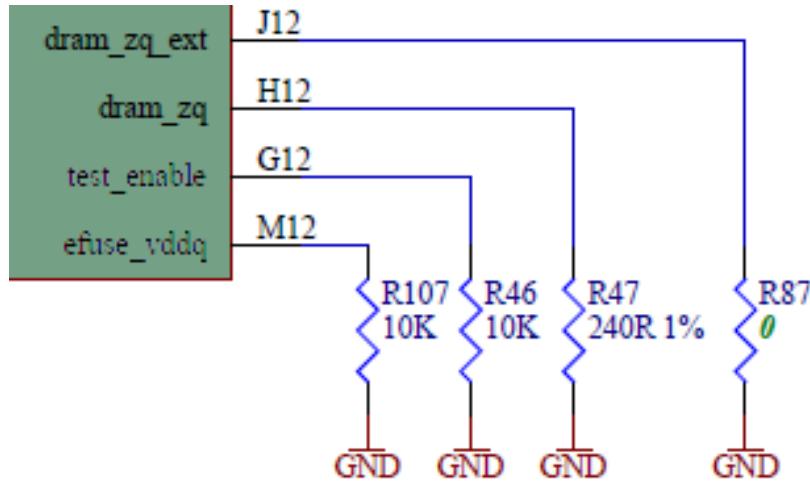


Figure 12: MA2100 Population Option DRAM_ZQ_EXT

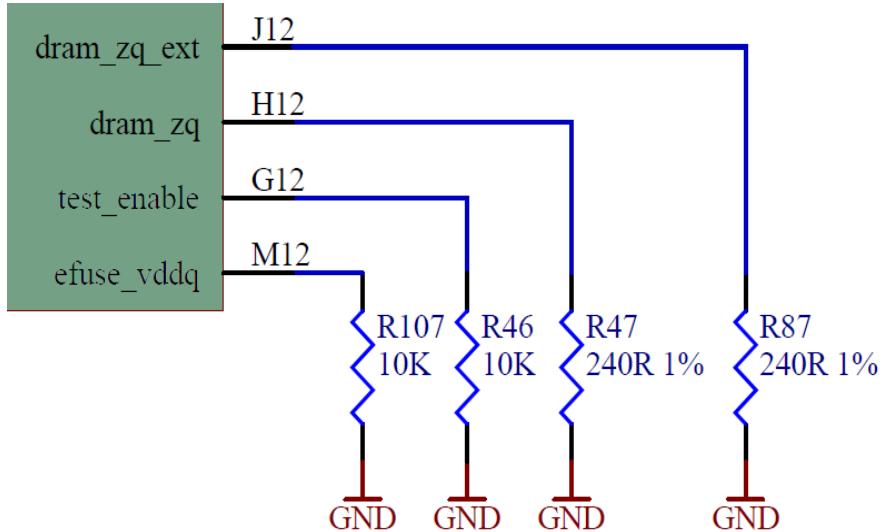


Figure 13: MA2150 Population Option DRAM_ZQ_EXT

2.3.3 Support for VDDIO_B on MA2150

To support this feature of MA2150 the MV0182-R4 PCB was modified so that BGA ball E9 could be sourced from 2 alternative paths as follows.

For MA2100 designs, RZ47 is mounted with a zero ohm link and E9 is thus connected to VSS as per previous revisions. In this case RZ48, RZ49 and R89 are not mounted so as to disconnect the alternative circuit.

For MA2150 designs RZ47, is not mounted and E9 (VDDIO_B) is supplied from PMIC_LDO2 via the current shunt resistor R89. In this case both RZ48 and RZ49 are also mounted

NOTE: Components RZ48 and RZ49 are used so that current measurement function of VDDCC can be repurposed when operating in MA2150 mode, as in that mode there is no independent VDDCC current consumption. Instead the corresponding ADC input is used to measure the current through R89 to the new rail VDDIO_B.

The MV0182-R4 based design also directly supports the use-case where VDDIO_B is used to enable SDCard connection without the use of level shifters. When the PCB is populated as described above for MA2150, LDO2 will be normally used to provide the I/O voltage to GPIO16-21. The voltage on LDO2 is also used on page 13 of the schematics to drive the SD_LS_DISABLE signal. Page 12 of the schematics shows how this signal when active is used to disable level-shifter U17 and enable analog switches U15/U16. Using this mechanism the design defaults to bypassing the level shifter once the VDDIO_B voltage is present.

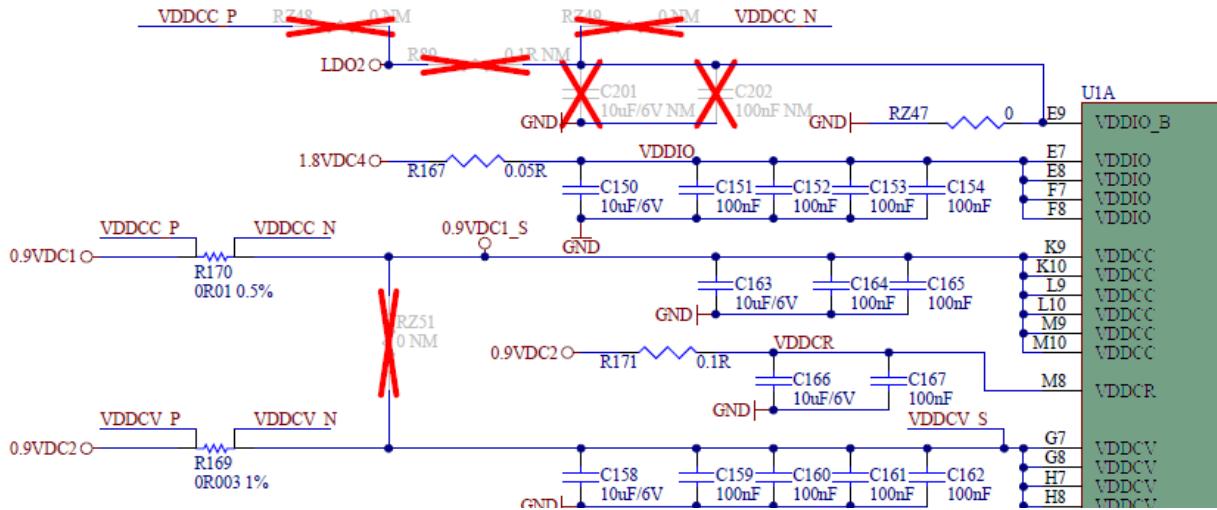


Figure 14: MA2100 Population Option VDDIO_B

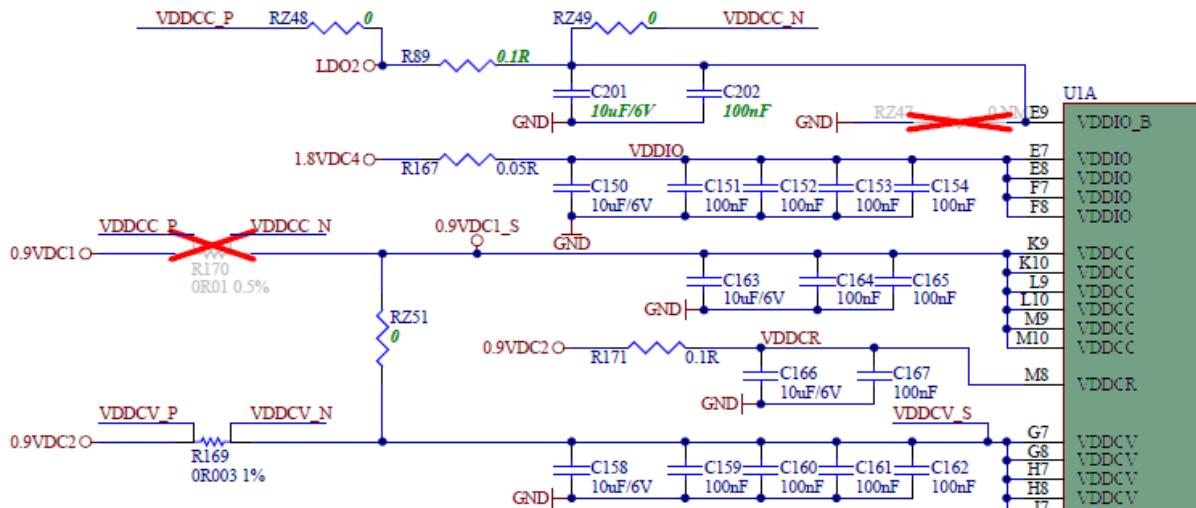


Figure 15: MA2150 Population Option VDDIO_B



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2.3.4 Table of Component Population Changes for MA2100 vs MA2150 usage

Component	Feature	Sch Page	MA2100 Value	MA2150 Value
RZ51	VDDCV/VDDCC	14	NM	OR
R170	VDDCV/VDDCC	14	OR01 0.5%	NM
R87	DRAM_ZQ_EXT	2	OR	240R 1%
RZ47	VDDIO_B	14	OR	NM
R89	VDDIO_B	14	NM	OR1
C201	VDDIO_B	14	NM	10 µF
C202	VDDIO_B	14	NM	100 nF
RZ48	VDDIO_B	14	NM	OR
RZ49	VDDIO_B	14	NM	OR

3 Getting Started Guide

This section explains how to connect up the development board and debug an application running on the board.

3.1 Equipment Required

The following pieces should have been supplied in the development kit:

- MV0182 Development Board + Mounting Metal Bracket
- JTAG Ribbon Cable
- Olimex Debugger Dongle
- USB 2.0 Cable for Olimex
- 5V Power Supply
- Mounting Tripod
- Plastic DIP Switch adjustment pen.

Optionally you may also have received the MV0200 and/or MV0201 camera daughtercards and/or the MV0191 board which can be used to interface to the Qualcomm DragonBoard™ AP.

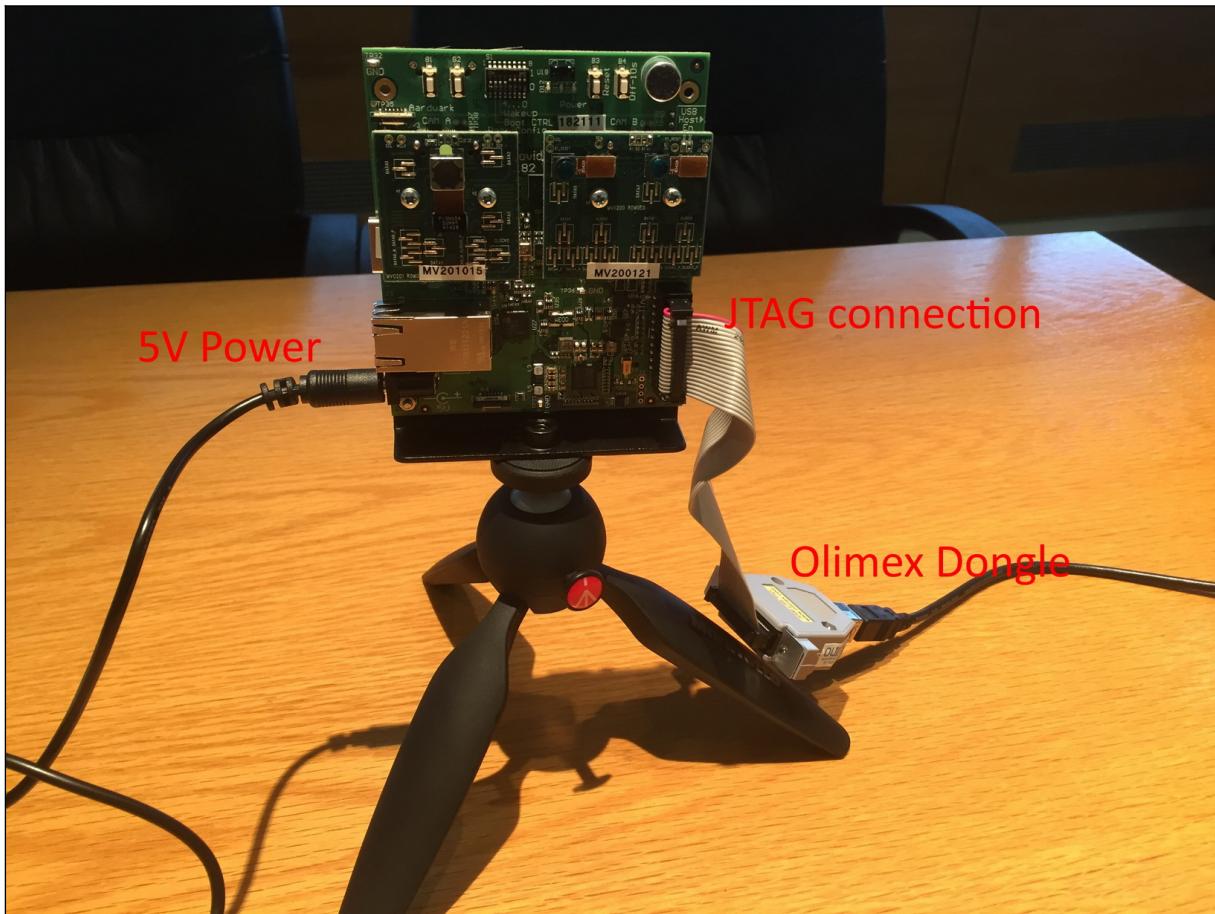


Figure 16: Illustration of Required Parts

3.2 Powering the Board

Once the board has been mounted on the included tripod and the JTAG connected as shown in [Figure 16](#), the power supply can be applied.

The MV0182-R2 board automatically powers up.

Initially LED D14 will light to indicate standby power, followed by D11, D12 after approximately 1 second² which indicates that the PMIC has started correctly.

NOTE: D11, D12 are user configurable LEDs driven by the PMIC chip which default to illuminated.

² This assumes no user application is booted. An application booted from Flash can take control for D11, D12 and change the default behaviour of the LEDs.



Figure 17: LED State immediately after applying Power



Figure 18: LED State After PMIC has initialized to default ON state

To power cycle the board, the user should remove the DC power connector from J6 and then reconnect it.

NOTE: There is a soft-power-off button (B4) connected to the PMIC which allows for a controlled PMIC shutdown by holding this button for 10 seconds. After shutting down using this mechanism a board restart can only be achieved by removing and replacing the DC power connector from J6 as described above. This button is intended for users who need to develop custom applications using the PMIC controller IC.

3.3 Running your first application

See [MDK_GettingStarted.pdf](#) for details on setting up the software environment and running your first application.

4 Boot Configuration and Switches

This section gives detailed information about the dip switch (8 channel) S1 and the four tactile switches B1, B2, B3, B4.

4.1 DIP Switch Connectivity

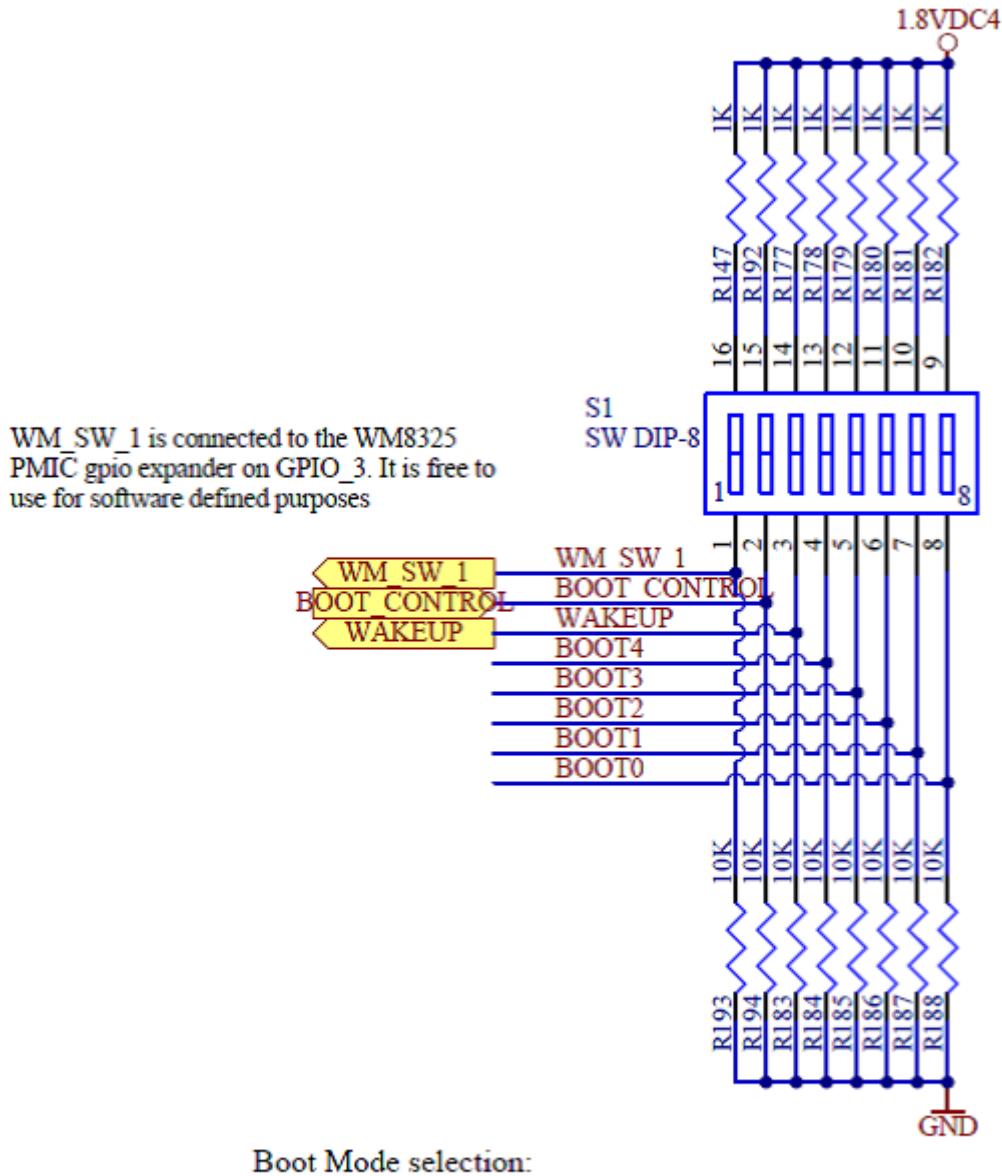


Figure 19: Schematic snippet showing DIP Switch Connections

DIP_SW_NUM	Name	Function	Alternate Function	Default State
1	WM_SW_1	Reserved, not accessible via software	None	OFF
2	BOOT_CONTROL	Select between FLASH and AP Boot	Dedicated	OFF
3	WAKEUP	Myriad WAKEUP PIN	Dedicated	OFF
4	BOOT4	Myriad GPIO_58 (Boot 4)	CLK_SEL (CDCEL925PW)	OFF
5	BOOT3	Myriad GPIO_56 (Boot 3)	COM_IO_5	ON
6	BOOT2	Myriad GPIO_53 (Boot 2)	COM_IO_2	ON
7	BOOT1	Myriad GPIO_52 (Boot 1)	COM_IO_1	OFF
8	BOOT0	Myriad GPIO_81 (Boot 0)	AUDIO_MCLK	OFF

Table 4: MV0182-R2 DIP Switch Description

The MV0182 DIP Switches are primarily used for boot mode configuration as follows:

- Switches 4 to 8 select the boot MODE using a 5 bit code BOOT4..0;
- Switch 3 configures the WAKEUP pin which should be low for normal boot operation;
- Switch 2 allows the user to select between SPI_FLASH boot using onboard flash memory when OFF (Default) or host driven boot from an external processor where Myriad should be configured in SPI Slave MODE;
- In MV0182 PCB revisions R2/R3 switch 1 is connected to GPIO_3 on the WM8325 and is therefore accessible in software. As of R4 revision, this feature is deprecated and as such, software developers should avoid the use of WM_SW1 so as to maintain compatibility across all MV0182 boards. See section [1.8.7](#) for further details on the motivation for this feature change.

NOTE: The MV0182 board uses a very small low profile DIP switch to achieve a compact design. Due to the small size of the DIP switch, this part is inherently fragile and care is needed when modifying the DIP switch settings so as not to damage this part. The MV0182 board is supplied with a sharp plastic pen which is intended for modification of DIP switch settings. DIP switch settings should always be changed using this part to avoid damage to your system.

4.1.1 Boot Configuration GPIO Sharing

BOOT Configuration pins 4..0 are shared with alternate functions in the design as described above. For example BOOT0 is shared with the master clock needed for Audio operation. This works because the boot pins are only sampled on the rising edge of reset, after the device has come out of reset, it is then possible to reconfigure these pins for their alternate function. The actual function is isolated from the effects of the boot selection resistors via a 100K resistor in series.

As a general rule the following recommendations should be applied when sharing functionality with Boot pins:

- The shared alternate function should be an output from Myriad
 - The problem with pins that are inputs to Myriad is that they may be driven by the external device at the time of reset. In limited cases it may be possible to use input pins if this possibility can be

precluded.

- For the boot modes to be supported it is important that the state of the shared pin at reset is valid for the connected external peripheral.
 - e.g. On this board two boot modes are supported 0xC (SPIM) and 0xD (SPIS)
 - For both supported boot modes BOOT4 is always low so it is safe to use this signal to also drive CLK_SEL which needs to have a default state of low.

This is particularly relevant for the BOOT1, BOOT2 and BOOT3 pins. These pins have an alternate function on the COMMON_IO bus which is a set of pins shared with the AP/LCD and camera connectors. Their function is determined by the daughtercards they are connected to. As such designers of daughtercards need to take care to satisfy the boot pin sharing requirements listed above.

NOTE: As described in Chapter 1.9.6 “Workaround for MV0200 Compatibility Issue” the issue of sharing GPIOs with boot configuration function has been resolved for PCB revision R5 and later due to the addition of circuitry which isolates the boot configuration GPIO's during the rising edge of reset.

4.1.2 Default DIP Switch Selection

The factory default setting for the BOOT Selection DIP Switch is shown below.

This setting selects Boot MODE 0xC which is SPIM 24 bit from the onboard 8 MB SPI Flash device.

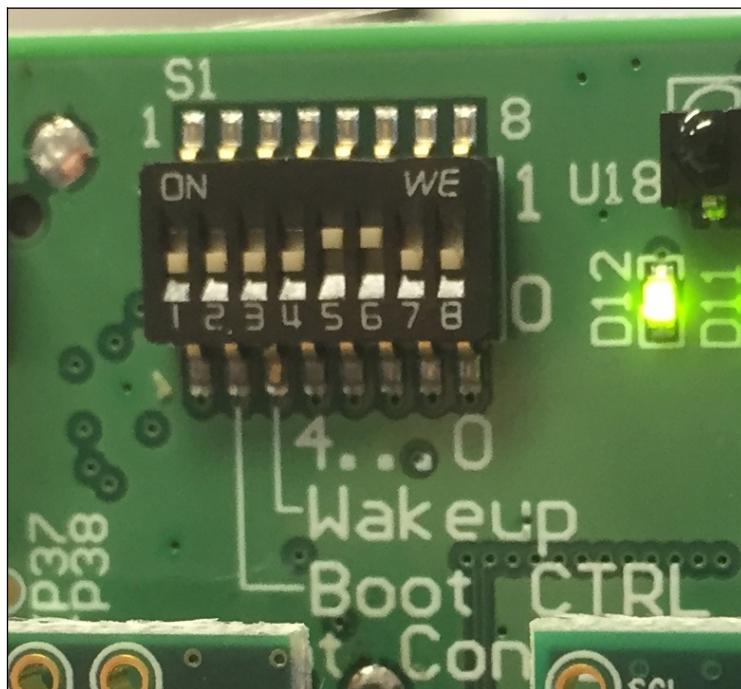


Figure 20: Default Boot Mode Configuration

4.2 Push Button Switch Functions

There are 4 tactile push button switches on the MV0182 board as follows:

Button ID	Function	Connection
B1	User Defined push button under software control	PMIC AUX GPIO1
B2	User Defined push button under software control	PMIC AUX GPIO2
B3	System Reset	Myriad2 Reset Control Pin
B4	PMIC Soft Power OFF button. Hold for 10 seconds to trigger system power off. (Note: This button cannot turn ON the system)	PMIC WM_ON signal

Table 5: Push Button Specification

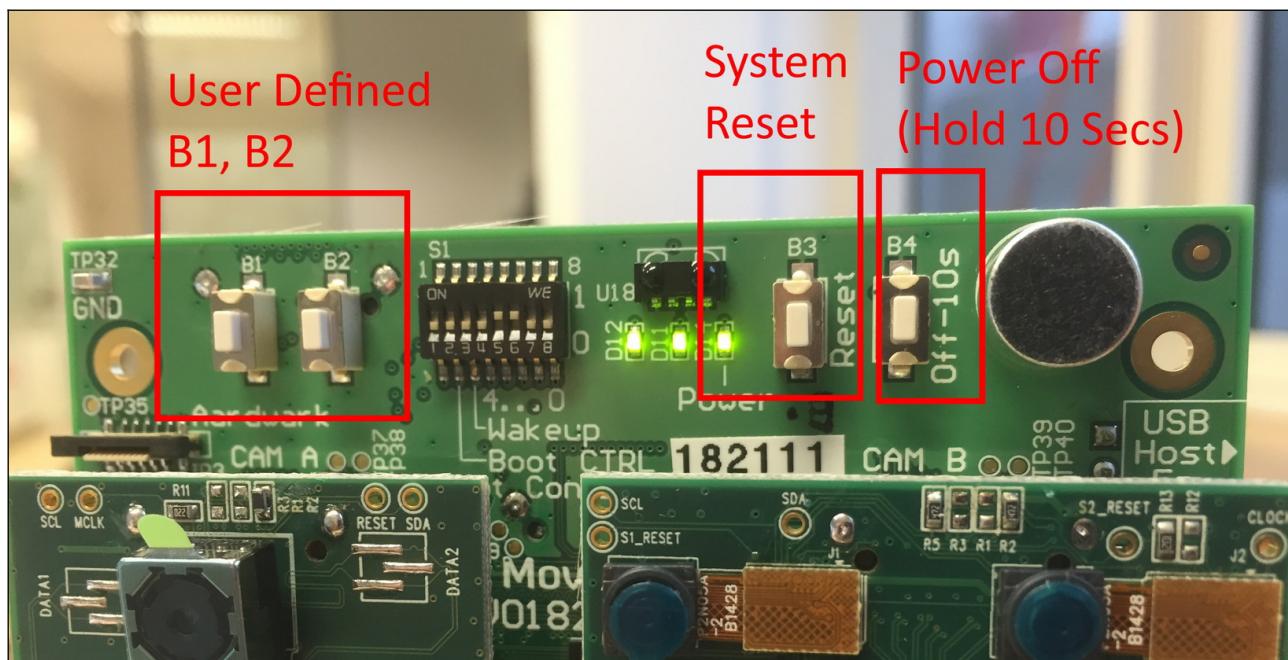


Figure 21: Location of the push button switches

5 System Clocks

5.1 Myriad Clock Sources

The Myriad 2 processor on the MV0182-R2 PCB is provided with the following clock sources:

Clock Name	Frequency	Description
OSC1	12 Mhz	Primary System Clock for Myriad
OSC2	27 Mhz	Secondary System Clock for Myriad
USB_REF_CLK	20 Mhz	USB Auxiliary clock source
RTC_CLK	32.768 KHz	Myriad RTC clock source

5.2 External PLL

To allow for maximum flexibility and to account for the constrained availability of GPIOs on the MV0182 platform an external PLL peripheral is used.

The device used is the CDCE925 with a 27 Mhz external oscillator source.

FUNCTIONAL BLOCK DIAGRAM for CDCE925, CDCE925

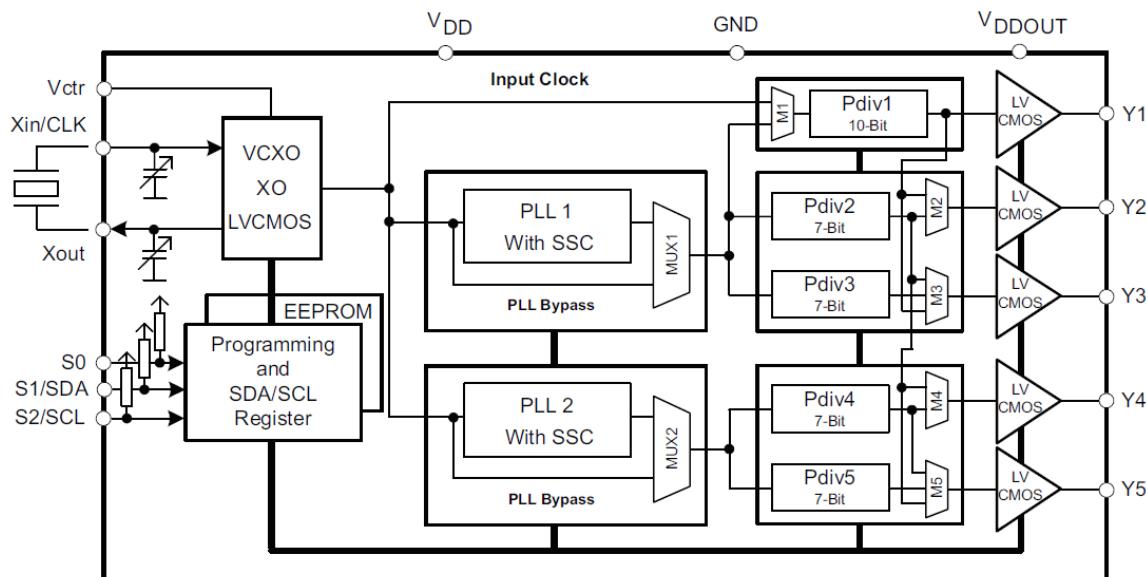


Figure 22: Block diagram of the CDCE925 Clock Generator



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This device is configured via I2C to provide the following System Clock Sources:

PLL Output	PLL Num	Connection	Description
Y1	PLL1	HDMI_PCLK_GEN	Clock Source for HDMI-TX (ADV7513)
Y4	PLL2	CAM_A_CLK_GEN	Optional Clock source for Camera daughtercards on CAM_A interface
Y5	PLL2	CAM_B_CLK_GEN	Optional Clock source for Camera daughtercards on CAM_B interface

Table 6: Clock Generator Output Utilization

6 Auxiliary GPIO Usage

The GPIO allocation on the MV0182 is optimized to support the maximum number of features on this development board. As such there are very few GPIOs remaining for general purpose usage.

To work around this limitation the design makes use of the Auxiliary GPIOs available on the WM8325 power management IC. These GPIOs are accessible via the I2C2 interface to the PMIC.

Some of the pins are used to control static signals such as the Ethernet reset, whereas others are assigned to the daughtercard interfaces for user expansion purposes. It is important to take this into consideration while designing daughtercards, as these I/O pins are most suited for static functions such as reset control. It is not advised to use these pins for functions where low latency operation is a requirement due to the overhead of the I2C communications needed to control them.

A special case is the Ethernet Phy IRQ signal. The intention here is that the PMIC supports a configuration where the GPIO can be configured as an IRQ. When the Ethernet_IRQ is asserted, the PMIC can be configured to signal this event to the Myriad processor using the WM_IRQ output of the PMIC. WM_IRQ is connected to GPIO_28 on myriad.

Furthermore the PMIC has 2 dedicated LED driver pins, these pins are used to directly control LED1 and LED2 on the board. As such, controlling these LEDs requires I2C communication with the PMIC controller.

The following table describes the function of the GPIOs allocated on the PMIC auxiliary interface:

GPIO	Function	Notes
1	WM_PB_1	Push Button
2	WM_PB_2	Push Button
3	WM_SW_1	DIP Switch #1
4	ETH_BOOT	Used to select between ethernet phy powerdown mode and GMII/MII mode
5	HDMI_PD	HDMI TX Power Down Control Signal
6	AP_IO_EXP1	General purpose IO#1 for use by LCD/AP Connector
7	BOOT_CONTROL	Switches between SPI Flash boot and AP SPI on SSO
8	Ethernet RST#	Ethernet PHY Reset control
9	Ethernet IRQ#	Ethernet Interrupt can be routed to WM_IRQ in SW
10	CAM_A IO EXP	General purpose IO for use by Camera A interface
11	CAM_B IO_EXP	General purpose IO for use by Camera B interface
12	AP_IO_EXP2	General purpose IO#2 for use by LCD/AP Connector
LED1	LED1 (D11 on PCB)	Dedicated PMIC LED1 control (Default on)
LED2	LED2 (D12 on PCB)	Dedicated PMIC LED2 control (Default on)

Table 7: PMIC Auxiliary I/O Allocation

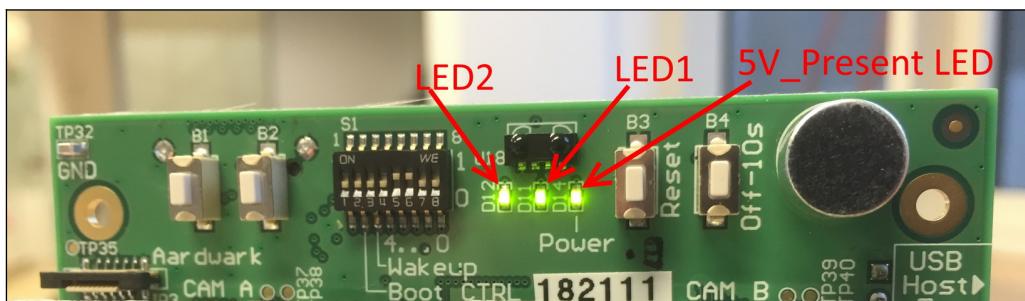


Figure 23: AUX LED Placement

7 USB Subsystem

MV0182 Board revisions with MA2100 silicon support USB Operation in USB 2.0 mode only.

This limitation is due to a hardware limitation in current silicon (see Errata section [11.1.1](#)).

The board supports operation as either a USB Device or a USB Host (subject to software support), however the user must take care to ensure that the jumper J9 is mounted only when operating in host mode. This jumper provides the 5V VBUS supply which would be needed by external devices in this case.

On MV0182 board revisions R2,R3 and R4 the physical USB interface is a USB 3.0 Micro-B receptacle which is backwards compatible with USB 2.0 Micro cables. On MV0182 board revision R5 the USB connector is a USB 3.0 Micro-AB receptacle.

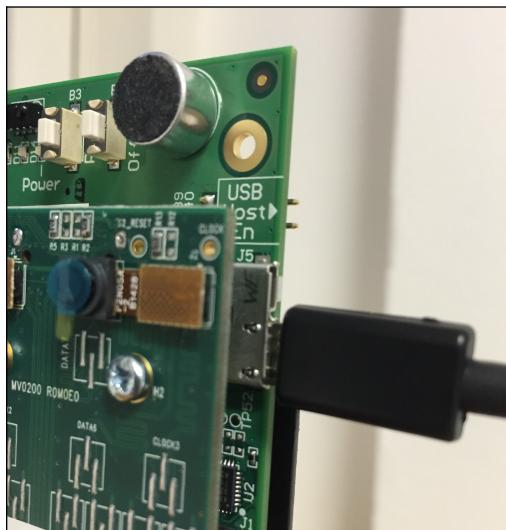


Figure 24: Example of USB2.0 Micro Cable Connection to MV0182

7.1 USB 2.0 Host support on PCB Revisions R2,R3,R4

In order to operate USB in host mode (subject to software support), it is necessary to use an adapter cable between USB-Micro-B and a USB-A-Receptacle. An example of such a cable is:

Manufacturer	Man Part Number	Distributor	Distributor Part Num	Description
Tensility	10-00769	Digikey	839-1124-ND	CBL USB A RCPT-MCR B PLUG 1M

Table 8: USB Host Mode Adapter Cable

7.2 USB 3.0 Host support on PCB Revision R5

On MV0182-R5, USB host support is possible by connecting a USB 3.0 micro A plug to the USB 3.0 micro-AB receptacle. This is subject to software support for USB host stack.

7.3 USB Host Enable Jumper

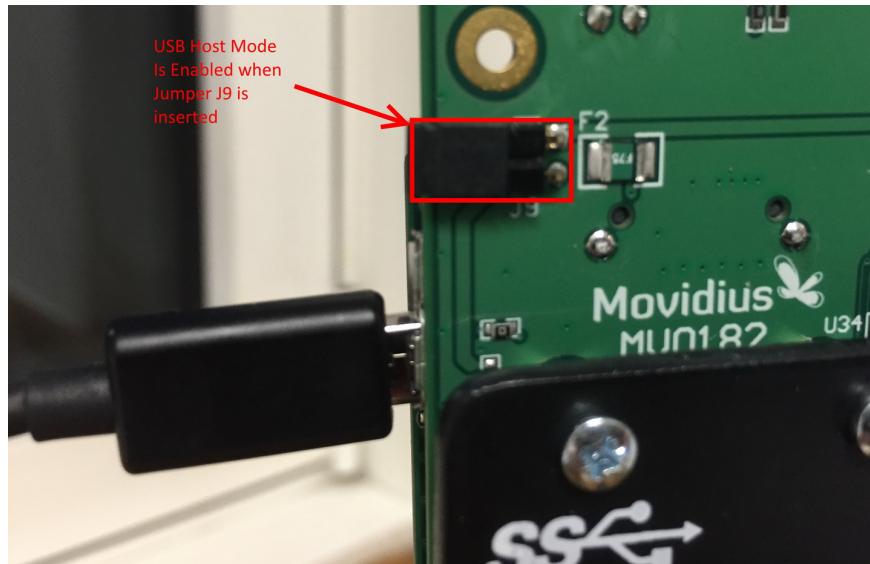


Figure 25: Jumper to Enable USB Host Mode

In order to enable host support Jumper J9 must be mounted to drive 5V out on VBUS as required by the USB host specification. Note: This jumper must never be mounted when operating as a USB device.

8 LCD & AP Expansion Port

The LCD & AP Expansion port on the MV0182 development board is intended to facilitate either the connection of TFT LCD panels to the development board or facilitate the interfacing of MV0182 to an Applications Processor (AP) board via a MIPI interface. This section describes this interface and the features it supports.

8.1 LCD & AP Expansion Port Feature Overview

	Feature
Power	Fixed 5V supply
LCD I/F	Dual MIPI D-PHY supporting MIPI DSI / CSI-TX in 1, 2 or 4 lane configuration
GPIO Signals	IRQ from LCD or Applications Processor (AP_IRQ)
Control Bus	<p>2 Pin I2C Interface (MV0182 is Master)</p> <p>SPI Interface (MV0182 is Slave) with SS0, SS1</p> <p>Slave Select 0 is used to Boot Myriad2 from AP and as control channel from AP to Myriad2. Note: Requires appropriate boot switch config.</p> <p>Slave Select 1 is reserved for future use.</p>
Reset Control	MB_RESET pin can be pulled low by the AP to reset the MV0182 Board. This can be used to force the Myriad2 to reboot with a different firmware image.
WAKEUP	The WAKEUP signal to Myriad2 is normally pulled low by the boot configuration DIP switch to facilitate normal boot. However this signal may be overridden by an AP using this port to utilise its alternate function of waking Myriad from power down mode.
COM_IO	<p>There is a single connection to this connector from the shared COMMON_IO bus using COM_IO1. This can be used as an additional direct GPIO connection to Myriad from the AP, HOWEVER, as this pin is shared with both the CAM_A and CAM_B connectors it is crucial that any applications making use of this feature ensure that the usage of this pin does not conflict with camera daughtercard functionality.</p> <p>As a general rule the use of the COM_IO should be avoided on daughtercard designs unless absolutely necessary. This maximises the flexibility of the system to mix and match different camera and AP expansion daughter-cards.</p>
AP_IO_EXP1/2	These are two general purpose Auxiliary I/O's which are available for use by the AP/LCD interface. They are driven by the PMIC auxiliary I/O function and control of these pins via software requires I2C communication from Myriad to the PMIC. As such they are most useful for functions such as static I/O configuration.

Table 9: LCD Expansion Port Feature Overview

8.2 LCD/AP Expansion Port J10 Pinout

Pin	Signal	Connection	Description	Direction
1	GND	GND	Common Ground	N/A
3	MIPI_PHYO_CLK_N	MIPI_C4_N	MIPI PHY4 Clock Pair	FROM_MV0182
5	MIPI_PHYO_CLK_P	MIPI_C4_P	MIPI PHY4 Clock Pair	FROM_MV0182
7	GND	GND	Common Ground	N/A
9	MIPI_PHYO_D0_N	MIPI_D8_N	MIPI PHY4 Data Pair 0	FROM_MV0182
11	MIPI_PHYO_D0_P	MIPI_D8_P	MIPI PHY4 Data Pair 0	FROM_MV0182
13	GND	GND	Common Ground	N/A
15	MIPI_PHYO_D1_N	MIPI_D9_N	MIPI PHY4 Data Pair 1	FROM_MV0182
17	MIPI_PHYO_D1_P	MIPI_D9_P	MIPI PHY4 Data Pair 1	FROM_MV0182
19	GND	GND	Common Ground	N/A
21	MIPI_PHY1_CLK_N	MIPI_C5_N	MIPI PHY5 Clock Pair	FROM_MV0182
23	MIPI_PHY1_CLK_P	MIPI_C5_P	MIPI PHY5 Clock Pair	FROM_MV0182
25	GND	GND	Common Ground	N/A
27	MIPI_PHY1_D0_N	MIPI_D10_N	MIPI PHY5 Data Pair 0	FROM_MV0182
29	MIPI_PHY1_D0_P	MIPI_D10_P	MIPI PHY5 Data Pair 0	FROM_MV0182
31	GND	GND	Common Ground	N/A
33	MIPI_PHY1_D1_N	MIPI_D11_N	MIPI PHY5 Data Pair 1	FROM_MV0182
35	MIPI_PHY1_D1_P	MIPI_D11_P	MIPI PHY5 Data Pair 1	FROM_MV0182
37	GND	GND	Common Ground	N/A
39	VDD_5V	VDD_5V	5V Power to Daughtercard, Max 0.5A total	FROM_MV0182
2	COM_IO1	GPIO_52	Common general purpose I/O; Shared with CAM_A, CAM_B	BI_DIR (if safe to share)
4	GND	GND	Common Ground	N/A
6	SPI_SCLK	SPI0_SCLK	SPI clock input	TO_MV0182
8	GND	GND	Common Ground	N/A
10	SPI_MISO	SPI0_MISO	SPI MISO	FROM_MV0182
12	GND	GND	Common Ground	N/A
14	SPI莫斯	SPI0莫斯	SPI MOSI	TO_MV0182
16	GND	GND	Common Ground	N/A
18	SPI_SSO	SPI0_SS_0_AP	SPI Slave Select 0 (For boot or AP Uplink communications)	TO_MV0182
20	I2C_SCL	I2C0_SCL	I2C0 Control bus to AP (shared with CAMB)	FROM_MV0182
22	I2C_SDA	I2C0_SDA	I2C0 Control bus to AP (shared with CAMB)	FROM_MV0182
24	GND	GND	Common Ground	N/A
26	MB_RESET	EXT_RST	Reset Input from AP (Active Low)	TO_MV0182
28	AP_IRQ	GPIO_22	IRQ from AP to Myriad	TO_MV0182
30	SPI_SS1	SPI0_SS_1	SPI Slave Select 1 (Reserved for future use)	TO_MV0182
32	MB_WAKEUP	WAKEUP	AP Control of WAKEUP Signal	N/A
34	AP_IO_EXP_1	WM8325_GPIO_6	General purpose I/O from PMIC	FROM_MV0182
36	AP_IO_EXP_2	WM8325_GPIO_12	General purpose I/O from PMIC	FROM_MV0182
38	RESERVED	TP45	Reserved for Future Use	N/A
40	VDD_5V	VDD_5V	5V Power to Daughtercard, Max 0.5A total	FROM_MV0182

Table 10: LCD Expansion Port Pinout

NOTE: All digital logic signal levels are based on 1.8V I/O logic unless otherwise specified.

9 Camera Expansion Port

The Camera Expansion port on the MV0182 development board is intended to facilitate the connection of either single or dual MIPI camera modules to the development board. This section describes this interface and the features it supports.

NOTE: All digital logic signal levels are based on 1.8V I/O logic unless otherwise specified.

9.1 Camera Expansion Port Feature Overview

	Feature
Power	Fixed 5V supply
MIPI I/F	The CAM A interface supports a single MIPI CSI camera in either 1, 2 or 4 lane configuration.
	The CAM B interface supports up to two MIPI CSI cameras each with either 1 or 2 MIPI lane support.
GPIO Signals	Each Camera interface has a two dedicated Myriad GPIOs, one of which has support for GPIO_PWM output mode; CAM_A_GPIO0 -> GPIO_59 CAM_A_PWM -> GPIO_27 CAM_B_GPIO0 -> GPIO_15 (Note: Also optionally UART_TX) CAM_B_PWM -> GPIO_33 (Note: Also optionally UART_RX)
Control Bus	2 Pin I2C Interface (MV0182 is Master)
	CAM_A uses I2C1 (dedicated)
	CAM_B uses I2C0 (Shared only with LCD/AP I2C interface)
Clock Source	Each Camera Interface has a dedicated clock source from the MV0182 CDCEL925 external PLL (CAM_A_CLK_GEN, CAM_B_CLK_GEN). Typically this clock source is used to provide a master clock to camera sensors.
COM_IO	Each camera interface shares 5 common GPIOs as part of the COM_IO bus. The shared nature of these GPIOs is a compromise between the shortage of free GPIOs on the overall design and the need for maximum flexibility on Camera and AP daughterboards. Please see section 9.2 for important notes on the use of these pins.
CAM_A_IO_EXP CAM_B_IO_EXP	These are two dedicated general purpose Auxiliary I/O's which are available for use by the camera interface. They are driven by the PMIC auxiliary I/O function and control of these pins via software requires I2C communication from Myriad to the PMIC. As such they are most useful for functions such as control of static signals (e.g. reset)

Table 11: Camera Expansion Port Feature Overview

9.2 Camera A Expansion Port (J12) Pinout

Pin	Signal Name	Connection	Description	Direction
1	GND	GND	Common Ground	N/A
3	MIPI_PHY0_CLK_N	MIPI_CO_N	PHY0 Clock Pair	TO_MV0182
5	MIPI_PHY0_CLK_P	MIPI_CO_P	PHY0 Clock Pair	TO_MV0182
7	GND	GND	Common Ground	N/A
9	MIPI_PHY0_D0_N	MIPI_D0_N	PHY0 Data0 Pair	TO_MV0182
11	MIPI_PHY0_D0_P	MIPI_D0_P	PHY0 Data0 Pair	TO_MV0182
13	GND	GND	Common Ground	N/A
15	MIPI_PHY0_D1_N	MIPI_D1_N	PHY0 Data1 Pair	TO_MV0182
17	MIPI_PHY0_D1_P	MIPI_D1_P	PHY0 Data1 Pair	TO_MV0182
19	GND	GND	Common Ground	N/A
21	RESERVED 3		NOT CONNECTED	N/C
23	RESERVED 4		NOT CONNECTED	N/C
25	GND	GND	Common Ground	N/A
27	MIPI_PHY1_D0_N	MIPI_D2_N	PHY1 Data0 Pair	TO_MV0182
29	MIPI_PHY1_D0_P	MIPI_D2_P	PHY1 Data0 Pair	TO_MV0182
31	GND	GND	Common Ground	N/A
33	MIPI_PHY1_D1_N	MIPI_D3_N	PHY1 Data1 Pair	TO_MV0182
35	MIPI_PHY1_D1_P	MIPI_D3_P	PHY1 Data1 Pair	TO_MV0182
37	GND	GND	Common Ground	N/A
39	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0182
2	CAM_COM_IO1	GPIO_52	General purpose I/O; Shared with CAM_B, AP, BOOT1	FROM_MV0182 (if safe to share)
4	GND	GND	Common Ground	N/A
6	CAM_COM_IO2	GPIO_53	General purpose I/O; Shared with CAM_B, BOOT2	FROM_MV0182 (if safe to share)
8	GND	GND	Common Ground	N/A
10	CAM_COM_IO3	GPIO_54	General purpose I/O; Shared with CAM_B, AP	BI_DIR (if safe to share)
12	GND	GND	Common Ground	N/A
14	CAM_COM_IO4	GPIO_55	General purpose I/O; Shared with CAM_B, PWR_MON	BI_DIR (if safe to share)
16	GND	GND	Common Ground	N/A
18	CAM_COM_IO5	GPIO_56	General purpose I/O; Shared with CAM_B, BOOT3	FROM_MV0182 (if safe to share)
20	I2C_SCL	I2C1_SCL	I2C Control Bus for Camera	FROM_MV0182
22	I2C_SDA	I2C1_SDA	I2C Control Bus for Camera	FROM_MV0182
24	GND	GND	Common Ground	N/A
26	CAM_CLK_GEN	CDCEL925PW_Y4	Clock Source for camera daughterboard, configured via i2c	FROM_MV0182
28	CAM_GPIO	GPIO_59	Dedicated daughterboard GPIO	BI_DIR
30	CAM_PWM	GPIO_27	Dedicated daughterboard GPIO+PWM	BI_DIR
32	RESERVED5	N/C	Reserved for future use	N/A
34	CAM_IO_EXP_1	WM8325_GPIO_10	Dedicated AuxiGPIO, I2C config	FROM_MV0182
36	RESERVED1	TP37	Reserved for future use	N/A
38	RESERVED2	TP38	Reserved for future use	N/A
40	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0182

Table 12: Camera Expansion Port Pinout

9.3 Camera B Expansion Port (J13) Pinout

Pin	Signal Name	Connection	Description	Direction
1	GND	GND	Common Ground	N/A
3	MIPI_PHY0_CLK_N	MIPI_C2_N	PHY2 Clock Pair	TO_MV0182
5	MIPI_PHY0_CLK_P	MIPI_C2_P	PHY2 Clock Pair	TO_MV0182
7	GND	GND	Common Ground	N/A
9	MIPI_PHY0_D0_N	MIPI_D4_N	PHY2 Data0 Pair	TO_MV0182
11	MIPI_PHY0_D0_P	MIPI_D4_P	PHY2 Data0 Pair	TO_MV0182
13	GND	GND	Common Ground	N/A
15	MIPI_PHY0_D1_N	MIPI_D5_N	PHY2 Data1 Pair	TO_MV0182
17	MIPI_PHY0_D1_P	MIPI_D5_P	PHY2 Data1 Pair	TO_MV0182
19	GND	GND	Common Ground	N/A
21	MIPI_PHY1_CLK_N	MIPI_C3_N	PHY3 Clock Pair	TO_MV0182
23	MIPI_PHY1_CLK_P	MIPI_C3_P	PHY3 Clock Pair	TO_MV0182
25	GND	GND	Common Ground	N/A
27	MIPI_PHY1_D0_N	MIPI_D6_N	PHY3 Data0 Pair	TO_MV0182
29	MIPI_PHY1_D0_P	MIPI_D6_P	PHY3 Data0 Pair	TO_MV0182
31	GND	GND	Common Ground	N/A
33	MIPI_PHY1_D1_N	MIPI_D7_N	PHY3 Data1 Pair	TO_MV0182
35	MIPI_PHY1_D1_P	MIPI_D7_P	PHY3 Data1 Pair	TO_MV0182
37	GND	GND	Common Ground	N/A
39	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0182
2	CAM_COM_IO1	GPIO_52	General purpose I/O; Shared with CAM_A, AP, BOOT1	FROM_MV0182 (if safe to share)
4	GND	GND	Common Ground	N/A
6	CAM_COM_IO2	GPIO_53	General purpose I/O; Shared with CAM_A, BOOT2	FROM_MV0182 (if safe to share)
8	GND	GND	Common Ground	N/A
10	CAM_COM_IO3	GPIO_54	General purpose I/O; Shared with CAM_A, AP	BI_DIR (if safe to share)
12	GND	GND	Common Ground	N/A
14	CAM_COM_IO4	GPIO_55	General purpose I/O; Shared with CAM_A, PWR_MON	BI_DIR (if safe to share)
16	GND	GND	Common Ground	N/A
18	CAM_COM_IO5	GPIO_56	General purpose I/O; Shared with CAM_A, BOOT3	FROM_MV0182 (if safe to share)
20	I2C_SCL	I2C0_SCL	I2C Control Bus for Camera	FROM_MV0182
22	I2C_SDA	I2C0_SDA	I2C Control Bus for Camera	FROM_MV0182
24	GND	GND	Common Ground	N/A
26	CAM_CLK_GEN	CDCEL925PW_Y5	Clock Source for camera daughterboard, configured via i2c	FROM_MV0182
28	CAM_GPIO	GPIO_15	Dedicated Camera daughterboard GPIO	BI_DIR
30	CAM_PWM	GPIO_33	Dedicated Camera daughterboard GPIO with PWM Support	BI_DIR
32	RESERVED3	TP39	Reserved for future use	N/A
34	CAM_IO_EXP_1	WM8325_GPIO_11	Dedicated Auxiliary GPIO, configured via I2C	FROM_MV0182
36	RESERVED1	TP39	Reserved for future use	N/A
38	RESERVED2	TP40	Reserved for future use	N/A
40	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0182

Table 13: Camera Expansion Port Pinout

10 Daughtercard Design Considerations

10.1 AP Uplink and Camera Interface MIPI connections Diagram

The following diagram illustrates at block level how the Camera and AP uplink connections are made to Myriad2. The diagram illustrates how the following use case would be achieved using the MV0182:

- Daughtercard with 4 lane MIPI camera connected to the CAM_A Interface
- Daughtercard with dual 2 lane MIPI cameras connected to the CAM_B Interface.
- Daughtercard which provides uplink to an Applications processor using a 4 lane MIPI configuration

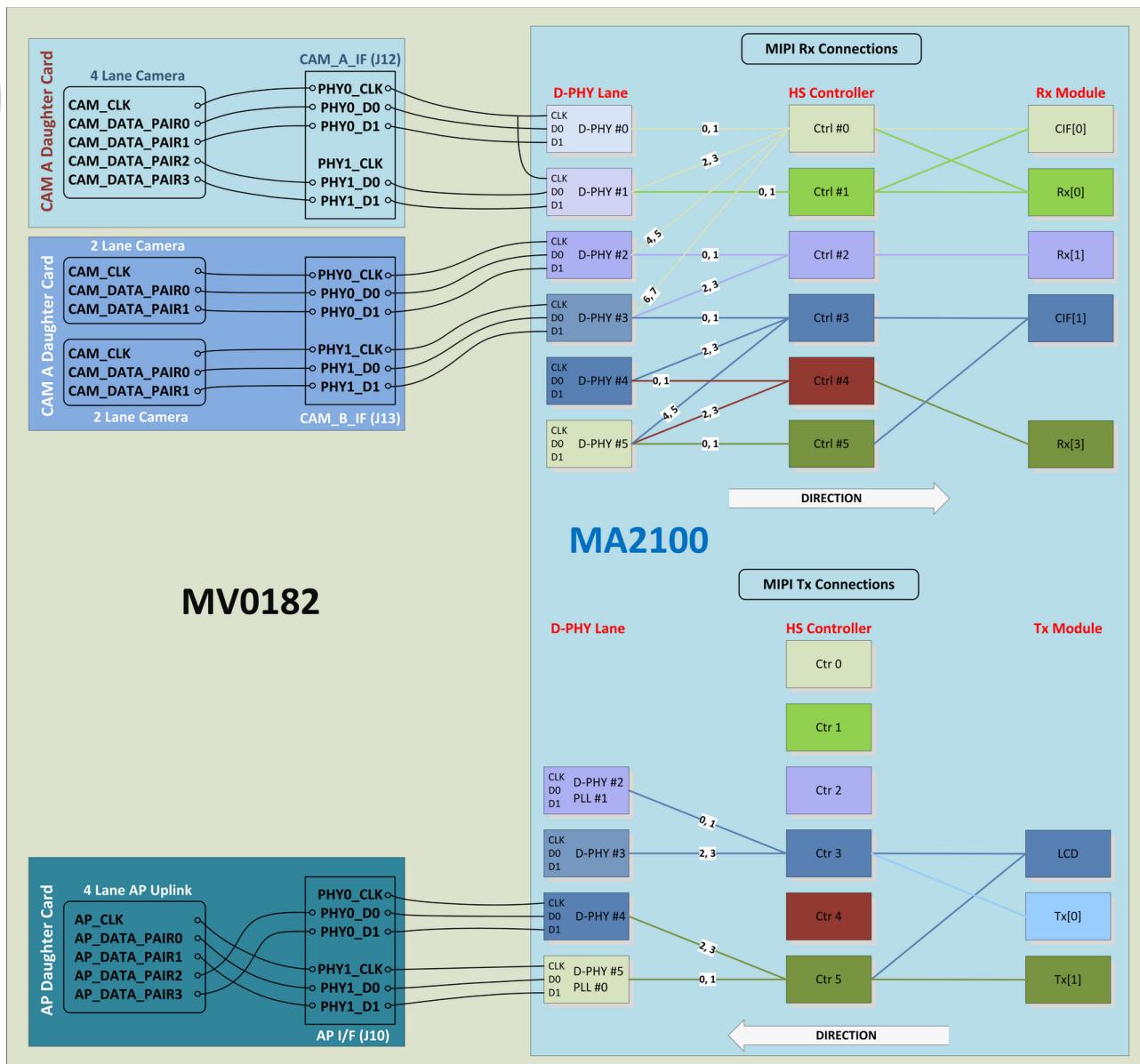


Figure 26: MV0182 MIPI Connections Example

Some Important points to note:

- The MIPI TX for D-PHY4,5 has reversed numbering 0,1 then 2,3 (see [Figure 26](#) above)
 - As such the AP Uplink Pair 0,1 are connected to D-PHY5 and Pairs 2,3 are connected to DPHY4
 - The clock source must come from D-PHY#5 as it is the only connected D-PHY containing a PLL
- It is not possible to build an AP daughtercard that supports a dual 2 lane MIPI output
 - This is because D-PHY4 does not contain an independent means of generating a clock
- The 4 lane MIPI-RX use case illustrated on the CAM_A interface shows a connection between DPHY-0 CLK and DPHY-1 CLK. This is needed to support 4 lane MIPI operation. This connection is made on the MV0182 motherboard directly under the Myriad2 BGA balls as directed in the Myriad2 platform datasheet.

10.2 Common I/O Bus Description

The MV0182 design maximizes the use of system GPIOs to support as many features as possible on this development platform.

This design goal means that there are very few GPIOs remaining for allocation to the various expansion interfaces (CAM_A, CAM_B, AP/LCD, POWER_MON). In order to maximize the flexibility of the expansion interface while working within the constraints of limited GPIOs, the decision was made to share 5 GPIOs between the 3 expansion headers.

This has the benefit of allowing certain expansion cards to use a maximum number of GPIOs when needed, but does so at the cost of introducing potential incompatibilities between different daughtercard configurations.

The general advice is that daughtercard designers should avoid the use of these common IO pins unless absolutely necessary for the application. For example it is better to use CAM_A_IO_EXP as a camera sensor reset control than use COM_IO1 for this purpose. Daughtercards which do not use any of the shared resources can safely be combined in any combination, however if the shared resources have been used then the user must take care to avoid any resource conflicts.

In addition to the constraints placed on these I/O's due to sharing across the expansion ports, further constraints result from the fact the 3 of the pins also double as boot pins. Please see section [4.1.1](#) for details of the specific constraints this imposes.

The following table provides a breakdown of the functions of the COM_IO bus and illustrates which pins are shared on each interface.

Signal	GPIO	CAM_A	CAM_B	AP_LCD	PWR_MON	Function A	Function B	Function C
COM_IO_1	gpio_52	2	2	2	-	BOOT1	GPIO_OUT	cpr_io_clk_3
COM_IO_2	gpio_53	6	6	-	-	BOOT2	GPIO_OUT	-
COM_IO_3	gpio_54	10	10	-	-	-	GPIO_IN_OUT	-
COM_IO_4	gpio_55	14	14	-	30	-	GPIO_IN_OUT	-
COM_IO_5	gpio_56	18	18	-	-	BOOT3	GPIO_OUT	-

Table 14: Common IO Function Sharing Breakdown

10.3 Mating Connector Descriptions

The MV0182 is designed with a view to having daughtercards which are mounted using a direct PCB to PCB

mounting strategy. To achieve the correct PCB Mating height Movidius recommends the use of the following connector type for MV0182 daughtercard designs:

Manufacturer	Part Number	Distributor	Part Number
Samtec	LSHM-120-06.0-L-DV	Farnell	2433941

Table 15: Recommended Daughtercard Connector Specification

For diagnostic or debug purposes Samtec also produce a cable that is compatible with this connector type.

Manufacturer	Part Number	Distributor	Part Number
Samtec	HLCR-20-09.80-BD-TD-2	Samtec Direct	N/A

Table 16: Recommended Daughter card Connector Specification

10.4 Connector Pin Numbering Convention

The MV0182 design uses a common connector for each daughtercard interface.

This connector is a hermaphroditic connector and as such it is important that a common convention is adopted to ensure the correct connection of daughtercard signals.

The following convention has been adopted by Movidius for the MV0182 design:

- In order to keep the schematic symbol the same for both motherboards and daughtercards Movidius opted to use different footprints on motherboard and daughtercard PCBs.
- To keep things easy for external daughtercard designers, the official pinout (as described in the Samtec datasheet) is used for all daughtercard layouts.
- As such only the Movidius MV0182 motherboard uses this non-standard footprint.
- To ensure compatibility daughtercard designers should only need to apply the following two steps:
 1. Use the same schematic symbol for daughtercard designs as in the MV0182 Schematics
 2. Follow the default layout footprint guidelines as documented by Samtec.
- The pin numbering will then match that of the schematic symbol, e.g. MIPI_PHY0_CLK_N goes to pin 3 for camera daughtercard designs.

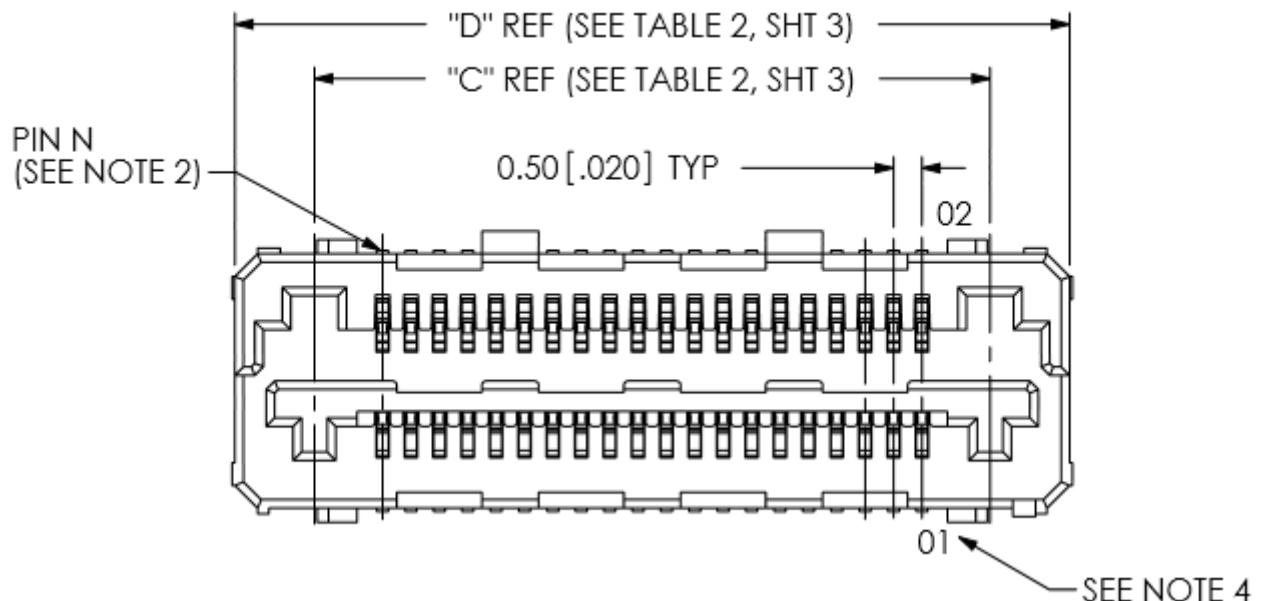


Figure 27: Example Samtec Footprint Recommendation

10.5 Daughtercard Mechanical Specification

This section provides mechanical details of the PCB hole placement and connector positions.

It applies to all PCB revisions up to and including MV0182-R4

Please see section 12 for details of other aspects of the mechanical specification.

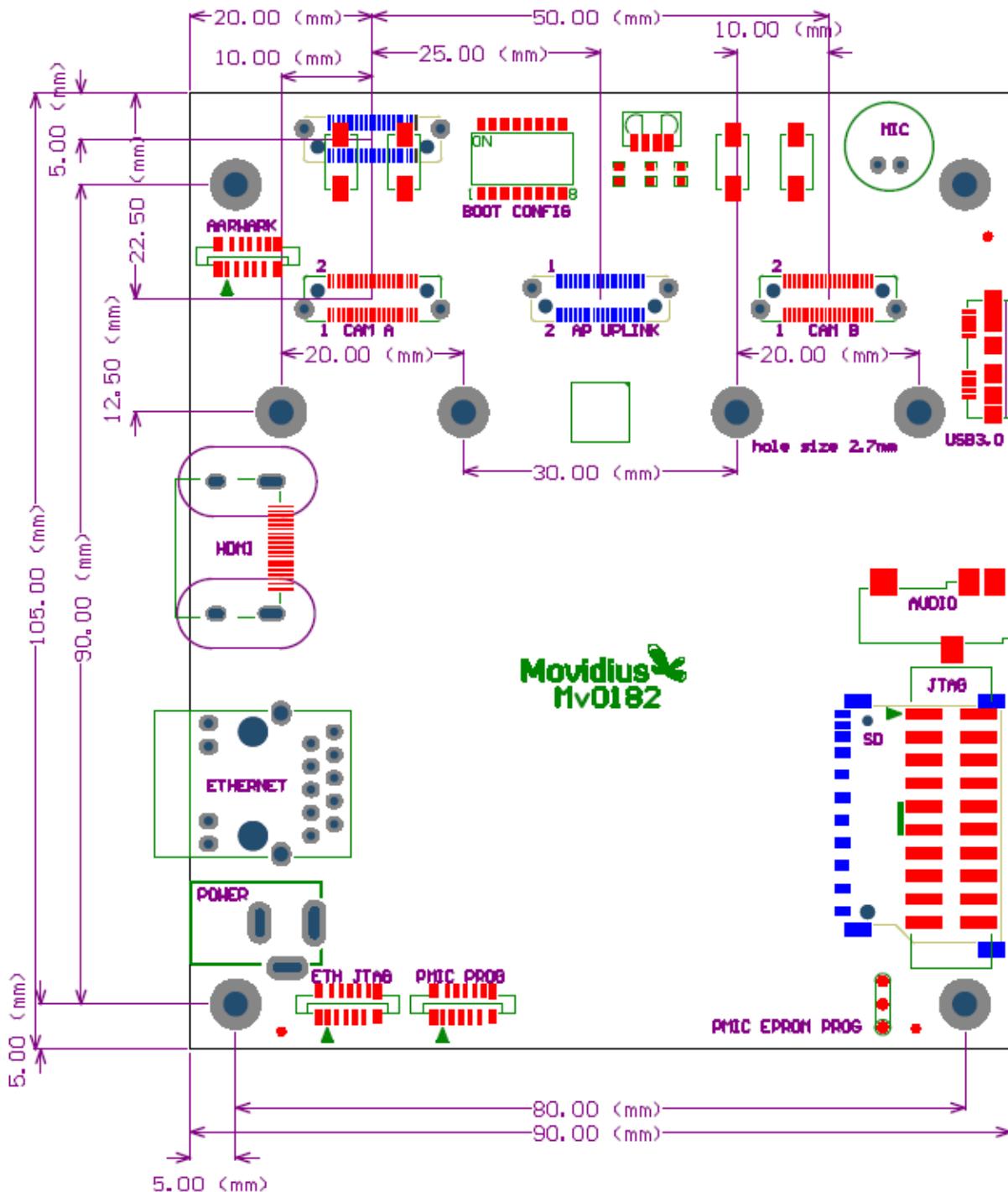


Figure 28: MV0182 Board Mechanical Specification

11 Known Limitations MV0182

This section details the known issues with the MV0182 design. It documents the severity of each issue any known workarounds if applicable. If issues have been resolved in subsequent PCB revisions this is noted in the solution field.

The scope of this document is limited to the hardware features of this board. It makes no reference to any software or driver limitations, as any such issues are documented as part of the general MDK software deliverable package.

11.1 Design Errata

11.1.1 MV0182-R2-1

Name	USB 3.0 Support is not functional.
Severity	High
Description	This support is not possible due to a silicon limitation in this version of silicon.
Limitation	Feature Reduction. Limited to USB 2.0 Support.
Solution	No Workaround available for revisions prior to MV0182-R4M0E1. However for revisions MV0182-R4M0E1 and later (which make use of new MA2150 silicon) USB 3.0 device support is now present.

11.1.2 MV0182-R2-2

Name	I2C clash between Audio TLV320 IC and Accelerometer BMX055 on I2C
Severity	Medium
Description	The Audio IC TLV320 has the same I2C Address as the BMX055, but shares the same I2C bus.
Limitation	Feature Reduction. It is not possible to support both features on MV0182-R2, audio device removed.
Solution	A) For MV0182-R2, electrical Revision E1 or later removes support for the Audio device B) For MV0182-R3 this limitation has been removed by selecting a different address for BMX055 using its I2C address configuration inputs.

11.1.3 MV0182-R2-3

Name	Barometer BMP180 has I2C_SCL,SDA swapped
Severity	Low
Description	There is a design error in the connection of I2C bus to this device.
Limitation	No Limitation with workaround.
Solution	This issue is corrected in electrical revision E1 or later (R2M0E1) which swaps the SCL/SDA lines to this device to fully resolve the issue This issue is resolved in PCB revision R3



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11.1.4 MV0182-R2-4

Name	Poor voltage regulation of 3.3V and 1.8V rail
Severity	Low
Description	There is excessive voltage ripple on these rails in initial design revision.
Limitation	No Limitation with workaround.
Solution	This issue is corrected in electrical revision E1 or later (R2M0E1) by applying 10µF of additional capacitance to each rail. This issue is resolved in PCB revision R3

11.1.5 MV0182-R2-5

Name	All generated clocks share a common PLL
Severity	Low
Description	The published schematics use outputs Y1,Y2, Y3 to supply HDMI and camera interfaces respectively. This creates a limitation that all outputs must share a common PLL which restricts the flexibility of the clock generator.
Limitation	No Limitation with workaround.
Solution	This issue is corrected in electrical revision E2 or later (R2M0E2) This revision modifies the design so that outputs Y4,Y5 are used to supply CAM_A, CAM_B respectively This issue is resolved in PCB revision R3

11.1.6 MV0182-R2-6

Name	PCB Silkscreen legend incorrectly labels I2C1 and I2C2 SDA/SCL testpoints
Severity	Low
Description	The bottom of the MV0182-R2 PCB has testpoints for the 3 I2C interfaces on the PCB. These testpoints have silkscreen legend to help the user correctly identify the relevant signals when probing the board. However there is an error in this silkscreen where the SDA/SCL labels are swapped for I2C1 and I2C2 (I2C0 is not effected)
Limitation	No functional limitation.
Solution	This issue is addressed in the documentation. See Figure 4 for clarification The MV0182-R3 revision fixes this error by correctly labelling the I2C signals.

11.1.7 MV0182-R2-7

Name	PCB Footprint for WM8325 (U23) not optimum
Severity	Low
Description	During manufacture it was observed that the footprint for U23 was not an exact match for the part as certain pins were very slightly out of alignment. While this caused no issues during the manufacture process it is the type of problem which

could cause yield losses in high volume runs.

Limitation No Limitation

Solution This issue caused no problems for MV0182-R2 and the footprint has been corrected in MV0182-R3

11.1.8 MV0182-R2-8

Name Component OS4 (USB Reference Oscillator) has incorrect part number

Severity Medium

Description The part specified for OS4 in MV0182-R2/R3 is 501JCA20M0000CAG

This part number is actually the 3.3V variant of the Si501 series but is being supplied with a 1.8V VDD voltage.

Testing has shown that this part still operates correctly at this voltage, but it is not advised that new designs should copy this error as there could be some fallout in high volume production runs.

For 1.8V operation the part number should start with 501H or 501L/M/N/P

Please see the Silabs datasheet for further authoritative information on this.

Limitation No Limitation

Solution This issue is not known to cause any problems in MV0182-R2/R3 but will be resolved in MV0182-R4 in any case by changing to part # Abracan ASDMB-20.000MHZ-LC-T

11.1.9 MV0182-R2-9

Name USB Reference Clock Input Voltage specification update

Severity Medium

Description In MV0182 PCB Revisions R3 and earlier, the USB_REF_CLK input is supplied using a resistor divider network composed of 2 resistors R189 (63.4R) and R156 (187R)

This results in a clock input on USB_REF_CLK_N with a peak voltage of 456mV based on an input 1.8V square wave from OS4.

In reviewing this signal level with the USB IP provider it was determined that this level is marginally out of specification.

While this signal level is proven to work on each shipped MV0182 board, there is a small risk that this issue could cause yield problems on higher volume production runs. As such all new designs are advised to use updated values for this resistor divider.

Limitation No Limitation

Solution This issue is not known to cause any problems in MV0182-R2/R3 but will be resolved in MV0182-R4 in any case.

The approved target signal level for this clock input is an approx 750mV square wave.

As of MV0182-R4 this resistor divider has been updated as follows:

- R156: 240R
- R189: 187R

This results in a square wave input of around 788mV

11.1.10 MV0182-R2-10

Name	Auto-On Circuit may have problems when connected to AP via MV0191
Severity	Medium
Description	<p>In MV0182 PCB Revisions R3 and earlier, there is a potential problem when the system is connected to the Dragon AP via the MV0191 Interface board.</p> <p>If the system is connected up and the Dragon board is powered before the MV0182, the MV0182 board may not automatically power on as is normally expected.</p> <p>The reason for this, relates to the way the auto-power on mechanism works.</p> <p>The auto-power on feature relies on R39 to pull the WM_ON# signal low at startup. This assumes that the rail connected to R38 is at a low level as the PMIC is, by definition not yet started. On MV0182-R3 and earlier revisions R38 is connected to the 1.8VDC4 regulator.</p> <p>The problem arises because the Dragon board SPI interface is powered while the MV0182 is not. This causes the I/O pins of U22 (SPI Flash) to be energised while its supply 1.8VDC4 is not enabled. Under these conditions the ESD protection diodes within the Flash become forward biased and feed some voltage from the I/O pins to the 1.8VDC4 power rail. This voltage on 1.8VDC4 causes a voltage across R38 which causes the PMIC to see a high value on its WM_ON# input. This high value prevents the PMIC from automatically powering on.</p> <p>While this mode of operation is obviously not ideal in any case, it does have the potential to confuse the user and may cause them to incorrectly think that their MV0182 board is faulty.</p>
Limitation	On MV0182-R3 and earlier, the MV0182 board must be powered before powering a connected Dragon board. (For all revisions this is actually the recommended sequence in any case)
Solution	<p>On MV0182-R3 and earlier this issue can be avoided by powering the MV0182 board before powering the Dragon board.</p> <p>On MV0182-R4 this issue is further mitigated by changing the default pull-up rail for R38. This is changed from being 1.8VDC4 to 1.8VLDO9. The 1.8VLDO9 has no indirect connection to the Dragon board and as such does not suffer from the same problem.</p>

11.1.11 MV0182-R2-11

Name	VDDCV Current Shunt Resistance connection not optimal
Severity	Low
Description	<p>In MV0182 PCB Revisions R3 and earlier, the current shunt resistor for the VDDCV rail is not optimally connected.</p> <p>The design intention was to use a 4 terminal resistor to perform a 4 wire measurement of the voltage across the shunt resistor. However in the schematic the high-side pair of terminals is shorted thus negating some of the benefit of the four wire measurement.</p>
Limitation	<p>No Measurable Limitation</p> <p>Theoretically this could cause a minor degradation in the precision of the VDDCV current measurement, but experimentally we have been unable to demonstrate any loss of</p>

performance.

Solution	This issue is corrected in MV0182-R4 PCB revision or later so that this design error is not repeated in derived designs.
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11.1.12 MV0182-R2-12

Name	U38 NXP LD6805K/33P footprint is very small and reflows poorly
Severity	Low
Description	In MV0182 PCB Revisions R3 and earlier, the chosen regulator for U38 is NXP LD6805K/33P and this part has a very small footprint that has proven difficult to solder reliably. To avoid the risk of a manufacturing defect an alternate regulator choice is recommended.
Limitation	None for MV0182 Potential manufacturing yield challenges if original design adopted for large volume production.
Solution	This issue is corrected in MV0182-R4 PCB revision or later by selecting a different regulator (TI TLV70033DCKT) for U38

11.1.13 MV0182-R2-13

Name	Power Sequence Table in the schematic is incorrectly documented
Severity	Low
Description	In MV0182 Schematic versions R3 and earlier, the table describing the regulator power sequence is incorrectly documented. Note: This is purely a documentation error and there is no negative impact for design itself. In summary the table describes a 3 state sequence whereas the shipped PMIC EEPROM implements a 4 state sequence as follows: S1 All Myriad rails S2 DRAM_VDD1 S3 DRAM_VDD2 S4 DRAM_VDDQ
Limitation	None. This errata simply highlights a documentation error to avoid confusion.
Solution	The implemented power sequence is now correctly described in the MV0182-R4 Schematic release.

11.1.14 MV0182-R2-14

Name	Invalid pullup voltage for SDCard interface when MV0182-R4 is populated for MA2150
Severity	Medium
Description	<p>The MV0182-R4 PCB design was intended to seamlessly support the transition between MA2100 and MA2150.</p> <p>For the SD Interface the mechanism by which this is intended to work is fully described in section 2.3.3 of this user manual.</p> <p>However, due to an oversight in the design, when operating in MA2150 mode, the SD pullup resistors R43,R44,R62,R63,R64,R65 are pulled up to the fixed rail 1.8VDC4.</p> <p>This is incorrect, as the SDCard standard demands that the bus initially operate at 3.3V.</p> <p>In MA2100 versions of the design, this is not a problem as the 1.8VDC4 rail is automatically disconnected when the level shifter is operational, and the level shifter has its own internal pullups to 3.3V.</p>
Limitation	In MV0182-R4M0E2 electrical revision, a workaround for this problem is adopted. With this workaround the design is limited to only operating with SDCards in 3.3V signalling mode.
Solution	<p>This issue is addressed by MV0182-R4 electrical revision E2.</p> <p>In MV0182-R4M0E2 the following changes are made:</p> <p>Page 13: RZ34 is not populated</p> <ul style="list-style-type: none"> → This prevents the enabling of LDO2 from disabling the level shifters → By forcing the system to always keep the level shifter active and never enable the analog switches, the level shifter internal 3.3V pullup resistors are used. → In this mode of operation it is never possible to negotiate down to 1.8V signalling levels, thereby limiting the max operational frequency of the design. <p>Note: MV0182-R4M0E2 also contains one other change which while not essential does provide a level of convenience to the end user. In this revision the PMIC config EEPROM (U43) is reprogrammed to default enable LD02 to output 1.8V. Without this change, user software would be needed to enable this power rail via I2C before making use of the SDCard interface.</p> <p>In the case of a PCB respin this issue can be completed solved by simply connecting pins U15-5 and U16-4 to LDO2 rather than 1.8VDC4. This solution will be considered for MV0182-R5 PCB revision.</p>



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11.1.15 MV0182-R2-15

Name Misleading text on Schematic page 10

Severity Low

Description Page 10 of the schematic has the following text:

“if RZ52 is mounted then BMI160 will use I2C - unmount for SPI”

This text is found beside U21 BMI160. It incorrectly implies that it is possible to operate U21 from SPI rather than I2C. This is not correct as there are no SPI connections to this IC.

Limitation No functional limitation. This is purely a cosmetic issue.

Solution This text will be removed in the event of any subsequent respin of this board.

11.2 Daughtercard Compatibility Issues

This section details any known compatibility problems between MV0182 and its daughtercard Modules.

11.2.1 MV0200-R0-A

Name	MV0200-R0 Boot Restrictions with MV0182 all revisions
Severity	Low
Description	<p>MV0200 is a camera daughtercard for MV0182 which supports dual Sony IMX208 Sensors</p> <p>This daughtercard uses COM_IO_5 for SENSOR2_RST signal.</p> <p>As described in section 10.2 Common I/O Bus Description it is important that attention is paid to pin sharing when using the COM_IO bus.</p> <p>In this case the SENSOR2_RST signal is pulled high by a 4.7K resistor (R5) on the MV0200 daughtercard. However as COM_IO_5 (GPIO_56) is shared with the function of BOOT3 during Myriad reset, this causes a problem.</p> <p>Specifically it is not possible to select a value for BOOT3 other than 1 when operating with MV0200 as the daughtercard resistor overrides the user Boot Config DIP switch selection.</p>
Limitation	MV0182 Feature reduction when operating with MV0200-R0
Solution	<p>This issue limits the range of boot modes possible on MV0182 when operating with an MV0200 daughtercard.</p> <p>Specifically the typical boot modes for MV0182 are:</p> <ul style="list-style-type: none"> 0x7 => SPIME 24 bit SPI Master Enhanced Boot 0xC => SPIM 24 bit SPI Master Boot 0xD => SPIS 24 bit SPI Slave Boot <p>Of these boot modes only 0xC and 0xD are possible, due to bit 3 being 1 in those instances.</p> <p>Boot mode 0x7 is not possible due to this design constraint and any attempt to use it will result in a failed boot as Myriad will see 0xF instead of 0x7</p> <p>Mode 0x7 is a faster boot mode than 0xC so the only real limitation here is one of reduced boot performance in SPI Master mode.</p>

NOTE: This compatibility issue is resolved for MV0182-R5 PCB revision and later. See section [1.9.6 “Workaround for MV0200 Compatibility Issue”](#) for further details.

12 Reference Documentation

This section details the supporting documentation provided with the MV0182 Development Boards.

All paths described are relative to the root of the extracted content from the movidius.org MV0182 documentation package.

As of the MV0182-R4 design there is a slight complication added to the release package which is worthy of some explanation. Because MV0182-R4 supports two different population variants (MA2100 vs MA2150) the Schematic variants feature of Altium designer was used to generate appropriate version specific variant information. This can be seen in the release package, where files have an additional suffix.

For example: BOM_MA2100-MV0182_R4M0E0(MA2100_NM).xls relates to the bill of populated components for the MA2100 variant of the design whereas BOM_MA2150-MV0182_R4M0E0 (MA2150_NM).xls relates to the components which would be populated if building boards with MA2150 parts.

Location ³	Description
MV0182_R3M0E0_Release\assembly	PDF Assembly Drawing ODB Machine Assembly Database Pick & Place Data
MV0182_R3M0E0_Release\BOM	Full Bill of Materials (XLS format) NOTE: (NM) variant is the subset of components which are mounted
MV0182_R3M0E0_Release\design	ZIP File containing all source design files in Altium Designer 10 Format
MV0182_R3M0E0_Release\gerber	Full PCB Gerber and NC_Drill files
MV0182_R3M0E0_Release\Layout	PDF version of Layout (all layers)
MV0182_R3M0E0_Release\mechanical	Documents outlining the mechanical specification for the board and including example mechanical specifications for camera daughtercards.
MV0182_R3M0E0_Release\Schematic	PDF Version of released schematic Note: In the MV0182-R4 release package there are 3 schematic PDF files supplied as follows: <ul style="list-style-type: none"> • MV0182_R4M0E0_Sch.pdf <ul style="list-style-type: none"> ◦ This schematic is PDF version of the master schematic which relates to both the MA2100 and MA2150 variants. However it does not highlight the population differences. For that level of detail please see the variant schematic PDFs. • MV0182_R4M0E0_Sch_MA2100_NM.PDF <ul style="list-style-type: none"> ◦ This schematic is a PDF version of the MA2100 population variant. It highlights the components

³ Note: For MV0182-RX Revision the documentation path starts with "MV0182_RXM0E0_Release"

Location	Description
	<p>which are not mounted for this variant.</p> <ul style="list-style-type: none">• MV0182_R4M0E0_Sch_MA2150_NM.PDF<ul style="list-style-type: none">◦ This schematic is a PDF version of the MA2150 population variant. It highlights the components which are not mounted for this variant.

Table 17: Reference Documentation