



MV0212 User Manual

v1.2 / November 2017

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Intel Movidius
2200 Mission College Blvd
M/S SC11-201
Santa Clara, CA 95054
<http://www.movidius.com/>

Revision History

Date	Version	Description
November 2017	1.2	Updated section 1.2 Key Top-Level Features . Added section 6.2 Connecting external USB Devices in host mode and limitations .

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1 Introduction

This document is the System Reference Manual for the MV0212 evaluation board. It provides detailed information on the overall design and usage of the MV0212 board. It is not intended to provide detailed documentation for the Myriad 2 processor or any other component used on the board. It is expected that the user refers to the appropriate documents for these devices to access further information.

This revision of the System Reference Manual specifically refers only to the MV0212-R0 PCB revision.

For specific details on the software SDK released with the MV0212 platform, see the separate "MDK_GettingStarted.pdf" document in the release pack.

NOTE: The MV0212-R0 design is derived from the Movidius MV0182-R5 PCB design and is intended to be directly compatible with any daughtercards which were designed for MV0182-R5. The design intent is that MV0212-R0 is functionally compatible with MV0182-R5 with the exception of the inclusion of the larger 512MB memory in the MA2450 SoC.

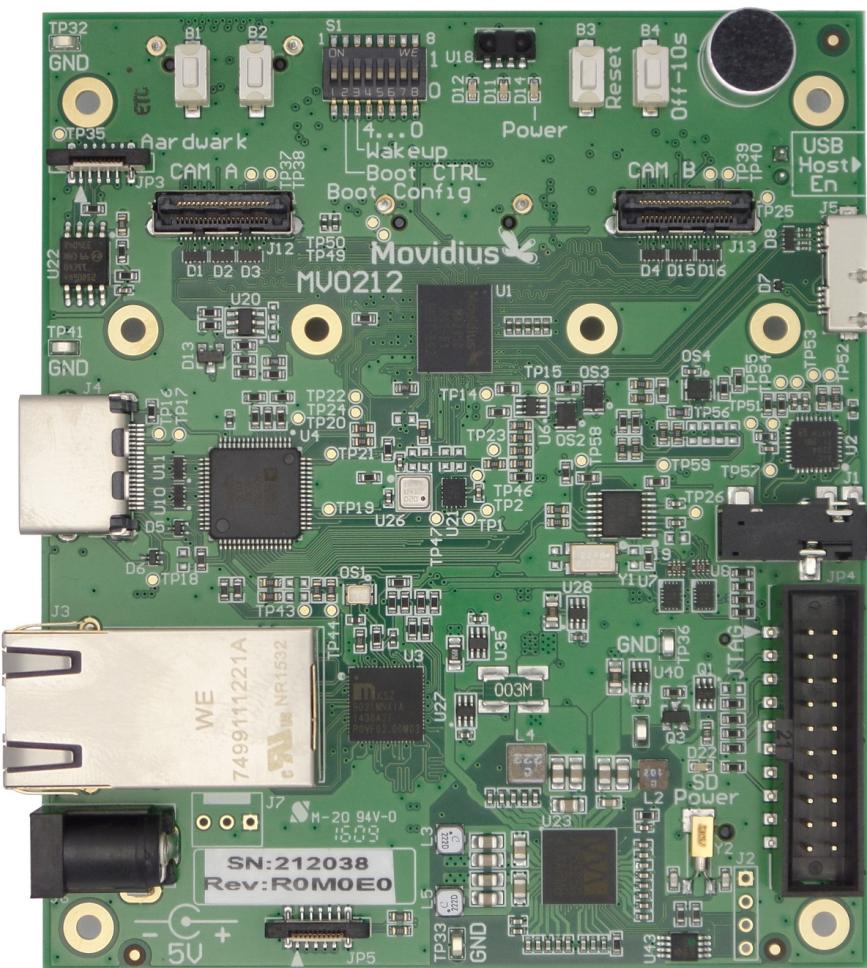
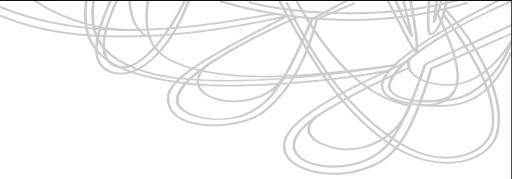


Figure 1: The MV0212 Development Board



1.1 MV0212 Board Specification

This section covers the specifications of the MV0212 board and provides a high level description of the major components and interfaces that make up the MV0212 board.

1.2 Key Top-Level Features

	Feature
Processor	MA2450 Multicore processor with stacked 512MB LPDDR2.
Boot Memory	8MB SPI Flash Memory (N25Q064A11ESE40G).
HDMI Video Output	ADV7513 HDMI Transmitter.
PC Connectivity	USB 2.0 Device Interface (Note: USB 3.0 Micro-AB Connector, but compatible with USB 2.0 Micro). Gigabit Ethernet Port (Micrel KSZ9031MNX PHY).
Storage	SD Card/SDIO Expansion slot.
User Interface	8 way DIP Switch for Boot Device Selection. 2 User Push Buttons. 2 User LEDs. Reset Button. Power Off Button.
System Debug	20 Pin 0.1" ARM compatible JTAG Debug Connector. 10 Pin FPC Aardvark (IIC/SPI) Debug Connector.
System Power	Wolfson WM8325 Power Management IC. 5V DC Power Supply Jack.
Expansion Headers	40 Pin LCD & AP Expansion Port with support for 4 lane MIPI DSI / CSI-TX. 40 Pin Camera_A Expansion Port with support for a single MIPI CSI-RX camera with up to 4 MIPI lanes. 40 Pin Camera_B Expansion Port with support for up to two MIPI CSI-RX cameras of 2 lanes each.
Sensors	Myriad 2 Power Consumption Monitoring Expansion header for connecting a custom power measurement daughter-card. BMI160 Inertial Measurement Unit. BMP_180 Pressure Sensor. Infrared Remote Control Sensor.
Audio	On board Microphone, Mono Audio input jack and Stereo Audio output jack.

Table 1: Key Top Level Features

1.3 Top-Level Block Diagram

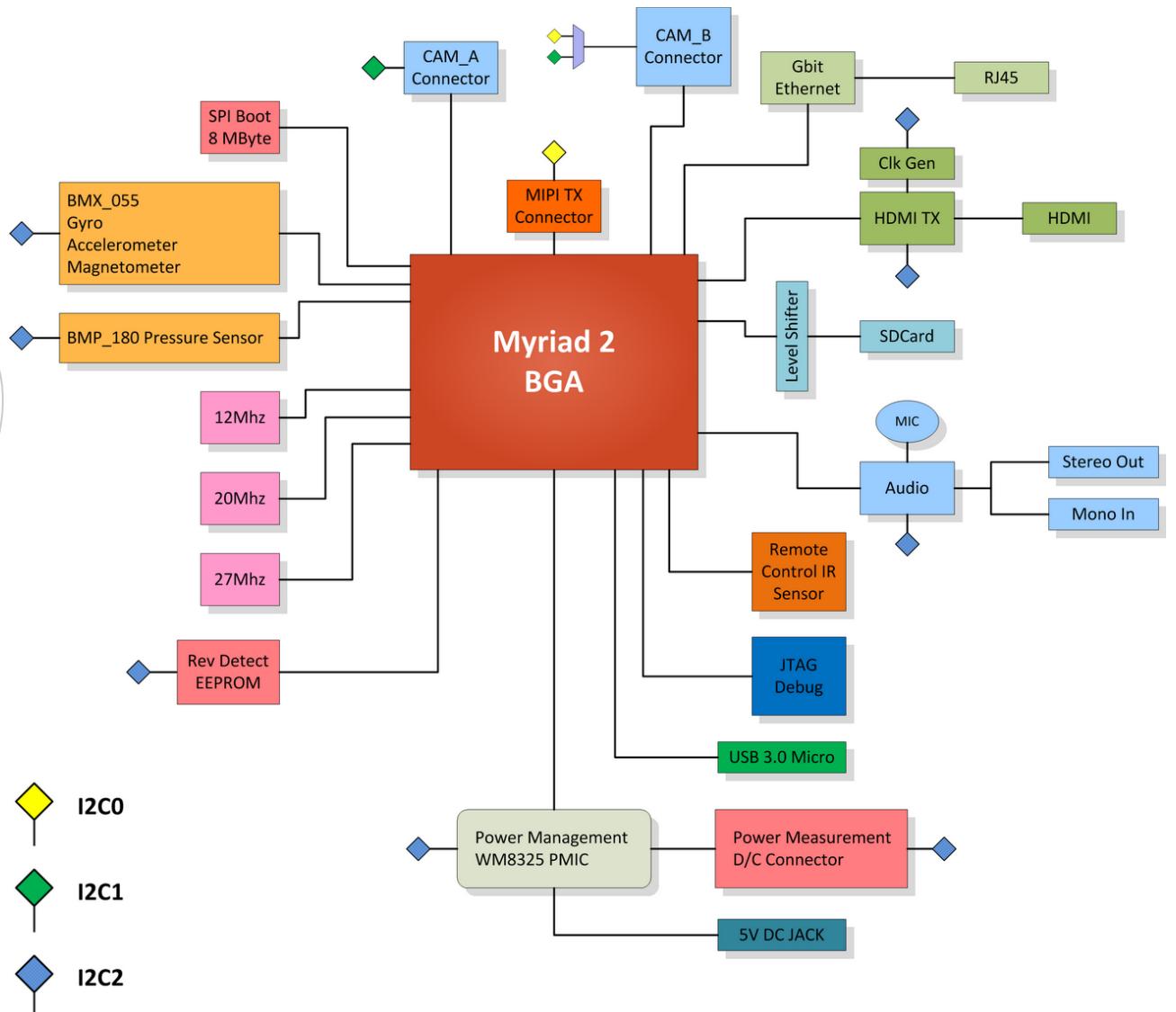


Figure 2: MV0212 System Block Diagram

1.4 PCB Overview

This section illustrates the location of the key system features on the PCB.

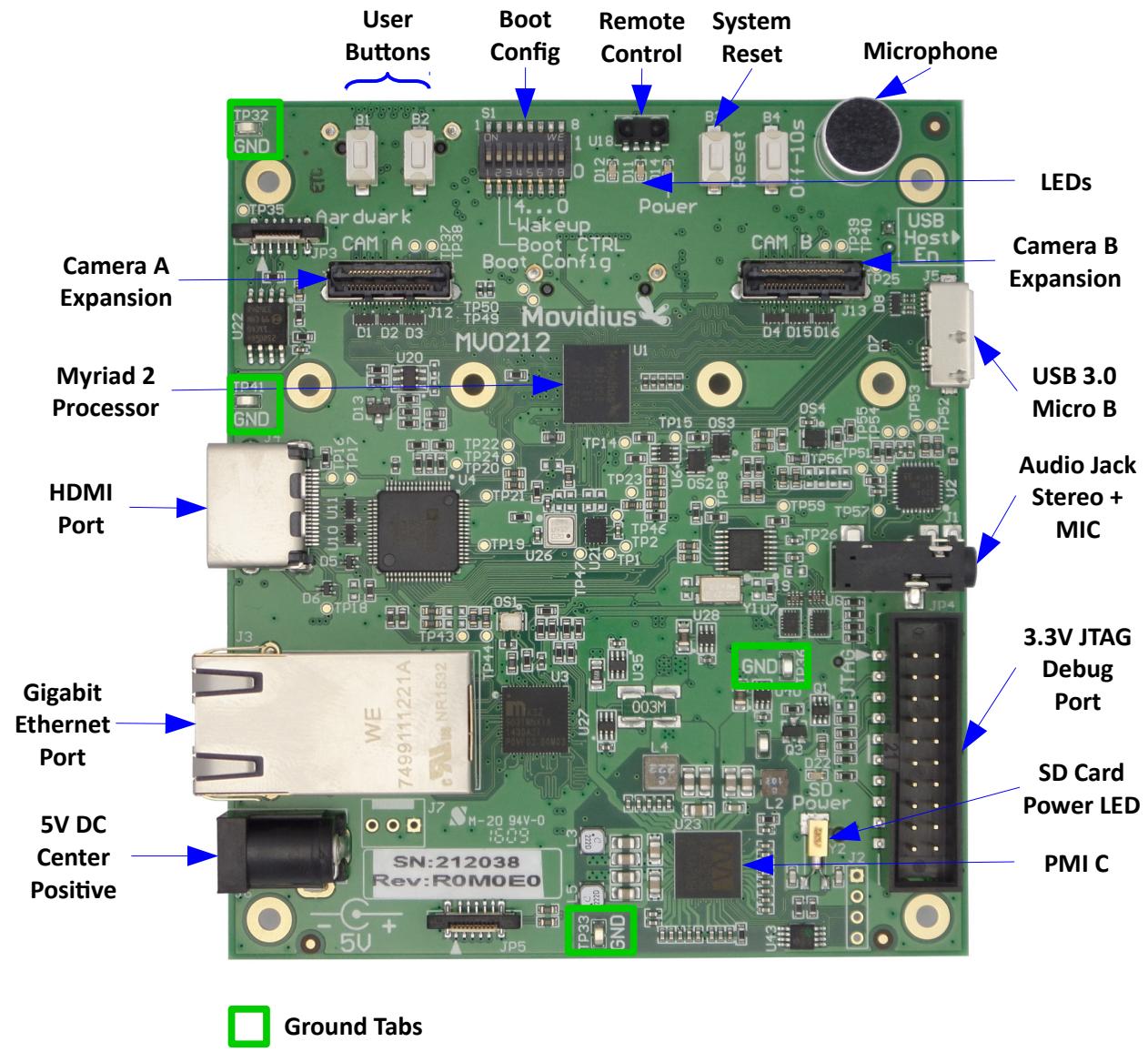


Figure 3: PCB Top Overview

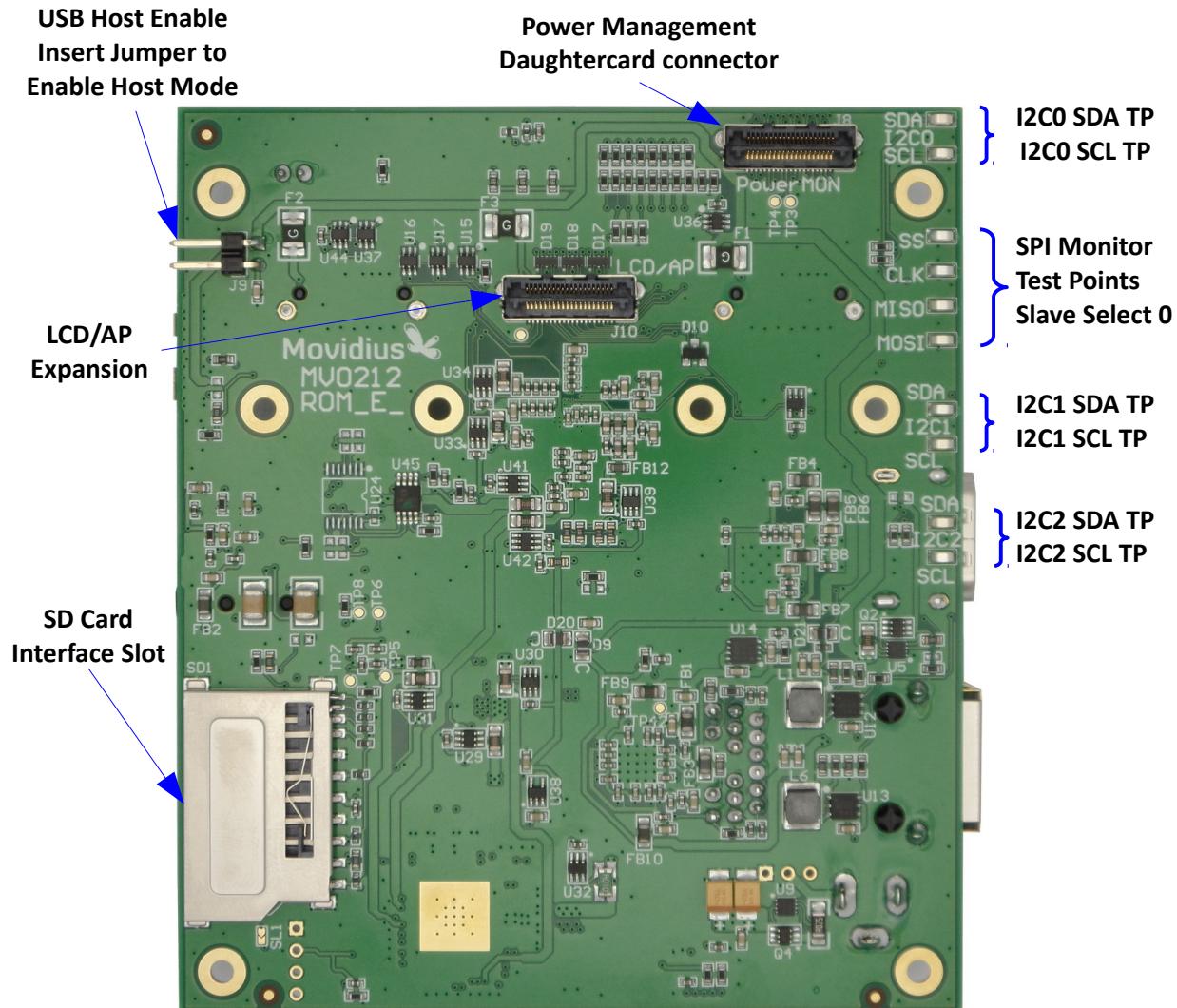


Figure 4: MV0212-R0 PCB Bottom Overview

1.5 Daughtercard Connections

The three daughtercard connections on the PCB use a common connector type. However, it is important to note that this does not imply that daughtercards are compatible between the different expansion ports.

Some specific camera daughtercards may be designed to be compatible between the CAM_A and CAM_B interfaces, but as a general rule daughtercards are designed specifically for the intended expansion port.

Users must take care to ensure that daughtercards are only attached to the intended expansion port. There are no physical interlocks in the design to prevent incorrect daughtercard attachments.

1.6 Movidius PCB Revision System

This section is intended to allow the user to correctly identify the MV0212 board revision and serial number. The Movidius board revision system is comprised of three components as follows:

Field	Description
RX	PCB Revision Number. Directly relates to the Printed Circuit Board. Any design change to the PCB will result in an increment of this field
MX	Mechanical Revision Number. This relates to a component change which changes the mechanical characteristics of the board. Example: Changing a pin header to a shrouded header would increment this field.
EX	Electrical Revision Number. This reflects any electrical modification to the design which does not involve a PCB change. Examples: Changing resistor values, or green wire modification of an existing design.

Table 2: PCB Revision Numbering System

All designs start at **ROM0E0** and increment fields as necessary from there.

The PCB silkscreen will contain the base revision for the PCB and supplemental labels are used thereafter to increase the MX or EX fields.

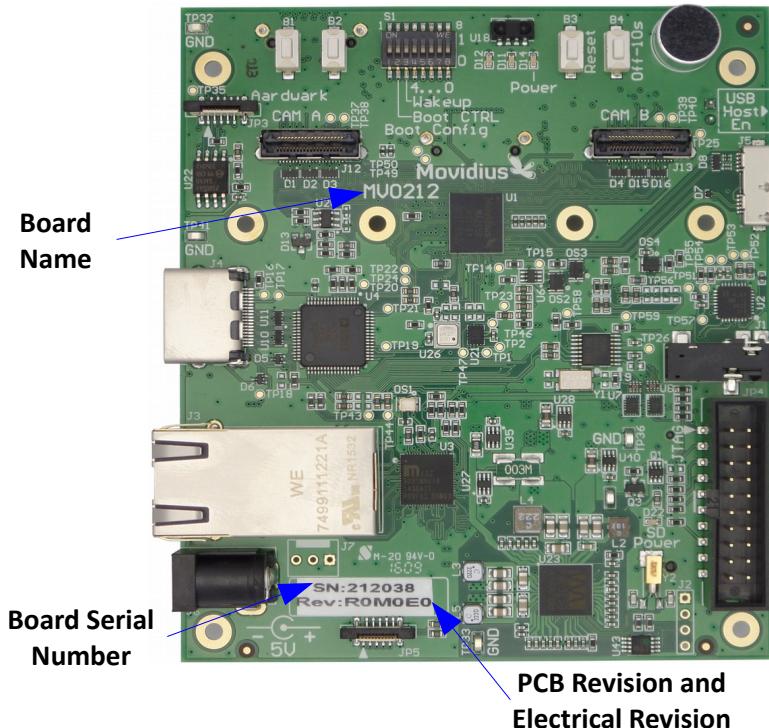


Figure 5: Identifying PCB Revision and Serial Number (MV0212-R0)

2 Getting Started Guide

This section explains how to connect up the development board and debug an application running on the board.

2.1 Equipment Required

The following pieces should have been supplied in the development kit:

- MV0212 Development Board + Mounting Metal Bracket.
- JTAG Ribbon Cable.
- Olimex Debugger Dongle.
- USB 2.0 Cable for Olimex.
- 5V Power Supply.
- Mounting Tripod.
- Plastic DIP Switch adjustment pen.

Optionally you may also have received the MV0200 and/or MV0201 camera daughtercards.

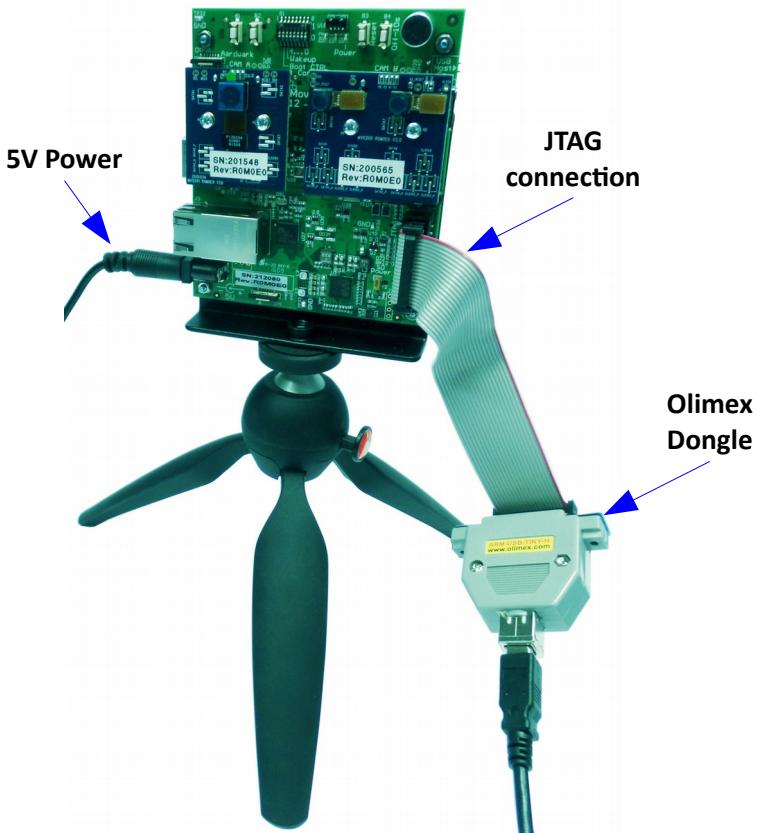


Figure 6: Illustration of Required Parts

2.2 Powering the Board

Once the board has been mounted on the included tripod and the JTAG connected as shown in [Figure 6](#), the

power supply can be applied.

The MV0212-R2 board automatically powers up.

Initially LED D14 will light to indicate standby power, followed by D11, D12 after approximately 1 second¹ which indicates that the PMIC has started correctly.

NOTE: D11, D12 are user configurable LEDs driven by the PMIC chip which default to illuminated.



Figure 7: LED State immediately after applying Power



Figure 8: LED State After PMIC has initialized to default ON state

To power cycle the board, the user should remove the DC power connector from J6 and then reconnect it.

NOTE: There is a soft-power-off button (B4) connected to the PMIC which allows for a controlled PMIC shutdown by holding this button for 10 seconds. After shutting down using this mechanism a board restart can only be achieved by removing and replacing the DC power connector from J6 as described above. This button is intended for users who need to develop custom applications using the PMIC controller IC.

2.3 Running your first application

See [MDK_GettingStarted.pdf](#) for details on setting up the software environment and running your first application.

¹ This assumes no user application is booted. An application booted from Flash can take control for D11, D12 and change the default on behaviour of the LEDs.

3 Boot Configuration and Switches

This section gives detailed information about the dip switch (8 channel) S1 and the four tactile switches B1, B2, B3, B4.

3.1 DIP Switch Connectivity

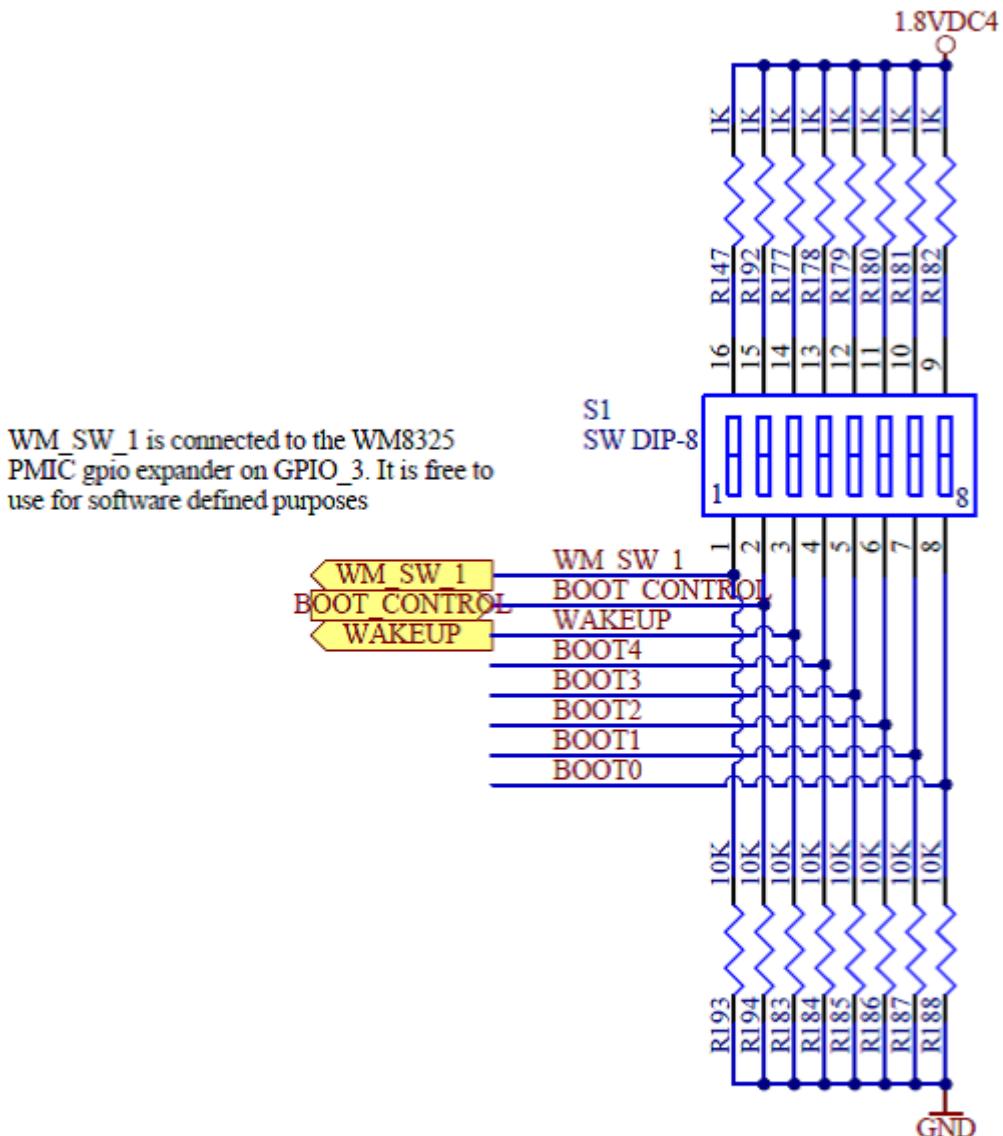


Figure 9: Schematic snippet showing DIP Switch Connections

DIP_SW_NUM	Name	Function	Alternate Function	Default State
1	WM_SW_1	Reserved, not accessible via software	None	OFF
2	BOOT_CONTROL	Select between FLASH and AP Boot	Dedicated	OFF
3	WAKEUP	Myriad WAKEUP PIN	Dedicated	OFF
4	BOOT4	Myriad GPIO_58 (Boot 4)	CLK_SEL (CDCEL925PW)	OFF
5	BOOT3	Myriad GPIO_56 (Boot 3)	COM_IO_5	ON
6	BOOT2	Myriad GPIO_53 (Boot 2)	COM_IO_2	ON
7	BOOT1	Myriad GPIO_52 (Boot 1)	COM_IO_1	OFF
8	BOOT0	Myriad GPIO_81 (Boot 0)	AUDIO_MCLK	OFF

Table 3: MV0212-R2 DIP Switch Description

The MV0212 DIP Switches are primarily used for boot mode configuration as follows:

- Switches 4 to 8 select the boot MODE using a 5 bit code BOOT4..0;
- Switch 3 configures the WAKEUP pin which should be low for normal boot operation;
- Switch 2 allows the user to select between SPI_FLASH boot using onboard flash memory when OFF (Default) or host driven boot from an external processor where Myriad should be configured in SPI Slave MODE;
- Switch 1 is reserved and is not accessible from the MA2450 processor

NOTE: The MV0212 board uses a very small low profile DIP switch to achieve a compact design. Due to the small size of the DIP switch, this part is inherently fragile and care is needed when modifying the DIP switch settings so as not to damage this part. The MV0212 board is supplied with a sharp plastic pen which is intended for modification of DIP switch settings. DIP switch settings should always be changed using this part to avoid damage to your system.

3.1.1 Boot Configuration GPIO Sharing

BOOT Configuration pins 4..0 are shared with alternate functions in the design as described above. For example BOOT0 is shared with the master clock needed for Audio operation. This works because the boot pins are only sampled on the rising edge of reset, after the device has come out of reset, it is then possible to reconfigure these pins for their alternate function. The actual function is isolated from the effects of the boot selection resistors via a 100K resistor in series.

As a general rule the following recommendations should be applied when sharing functionality with Boot pins:

- The shared alternate function should be an output from Myriad
 - The problem with pins that are inputs to Myriad is that they may be driven by the external device at the time of reset. In limited cases it may be possible to use input pins if this possibility can be precluded.
- For the boot modes to be supported it is important that the state of the shared pin at reset is valid for the connected external peripheral.

This is particularly relevant for the BOOT1, BOOT2 and BOOT3 pins. These pins have an alternate function on the COMMON_IO bus which is a set of pins shared with the AP/LCD and camera connectors. Their function is determined by the daughtercards they are connected to. As such this would normally create a constraint for daughtercard designers. The MV0212 design removes this restriction by using a mux on these pins. This mux ensures that the GPIOs are connected to the boot configuration only until the rising edge of reset. Once reset is high the boot configuration has already been latched and the mux then connects the GPIO to its "Alternate Function". This simplifies daughtercard design.

NOTE: During reset COM_IO_1, COM_IO_2, COM_IO_3 are floating so daughtercard designs should account for this.

3.1.2 MV0212 Supported Boot Modes

The MV0212 platform supports selection of the GPIO configured boot modes of the MA2450 SoC using DIP Switches 8,7,6,5,4 and 3. As the MA2450 part on the MV0212 board does not have eFuses configured the WAKEUP DIP Switch should always be in the "OFF" state to select GPIO configured boot mode.

Please see the Myriad2 Soc User Manual for full details on the supported boot modes.

The following table illustrates the subset of GPIO configured boot modes which are supported by the MV0212 board.

Boot Mode Number	Boot Mode Type	DIP[2] BOOT_CONTROL	DIP[3] WAKEUP	DIP[4..8]	Notes
0x2	USBD	OFF	OFF	OFF,OFF,OFF,ON,OFF	USB Device Boot
0x6	DEBUG_HALT ²	OFF	OFF	OFF,OFF,ON,ON,OFF	Doesn't boot from any interface
0x7	SPIME_24bit	OFF	OFF	OFF,OFF,ON,ON,ON	Onboard flash memory in fast boot mode
0xC	SPIM_2 4bit	OFF	OFF	OFF,ON,ON,OFF,OFF	Onboard flash memory in slower boot config
0xD	SPIS	OFF	OFF	OFF,ON,ON,OFF,ON	Boot from external AP connected to the SPI Slave interface using the LCD/AP connector

Table 4: MV0212 Boot configuration Options

² The DEBUG_HALT boot mode is mainly useful for troubleshooting. It does not configure the PLL, it just enables all clocks and then goes into an infinite loop.

3.1.3 Default DIP Switch Selection

The factory default setting for the BOOT Selection DIP Switch is shown below.

This setting selects Boot MODE 0xC which is SPIM 24 bit from the onboard 8 MB SPI Flash device.



Figure 10: Default Boot Mode Configuration

3.2 Push Button Switch Functions

There are 4 tactile push button switches on the MV0212 board as follows:

Button ID	Function	Connection
B1	User Defined push button under software control.	PMIC AUX GPIO1
B2	User Defined push button under software control.	PMIC AUX GPIO2
B3	System Reset	Myriad 2 Reset Control Pin
B4	PMIC Soft Power OFF button. Hold for 10 seconds to trigger system power off. (Note: This button cannot turn ON the system)	PMIC WM_ON signal

Table 5: Push Button Specification

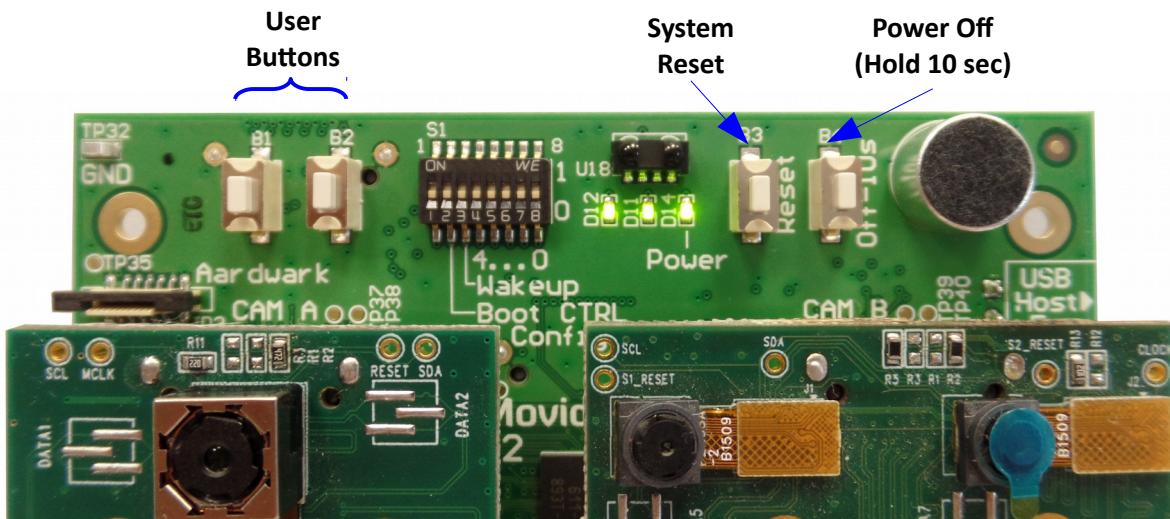


Figure 11: Location of the push button switches

4 System Clocks

4.1 Myriad Clock Sources

The Myriad 2 processor on the MV0212-R2 PCB is provided with the following clock sources:

Clock Name	Frequency	Description
OSC1	12 MHz	Primary System Clock for Myriad.
OSC2	27 MHz	Secondary System Clock for Myriad.
USB_REF_CLK	20 MHz	USB Auxiliary clock source.
RTC_CLK	32.768 KHz	Myriad RTC clock source.

4.2 External PLL

To allow for maximum flexibility and to account for the constrained availability of GPIOs on the MV0212 platform an external PLL peripheral is used.

The device used is the CDCE925 with a 27 MHz external oscillator source.

FUNCTIONAL BLOCK DIAGRAM for CDCE925, CDCE925

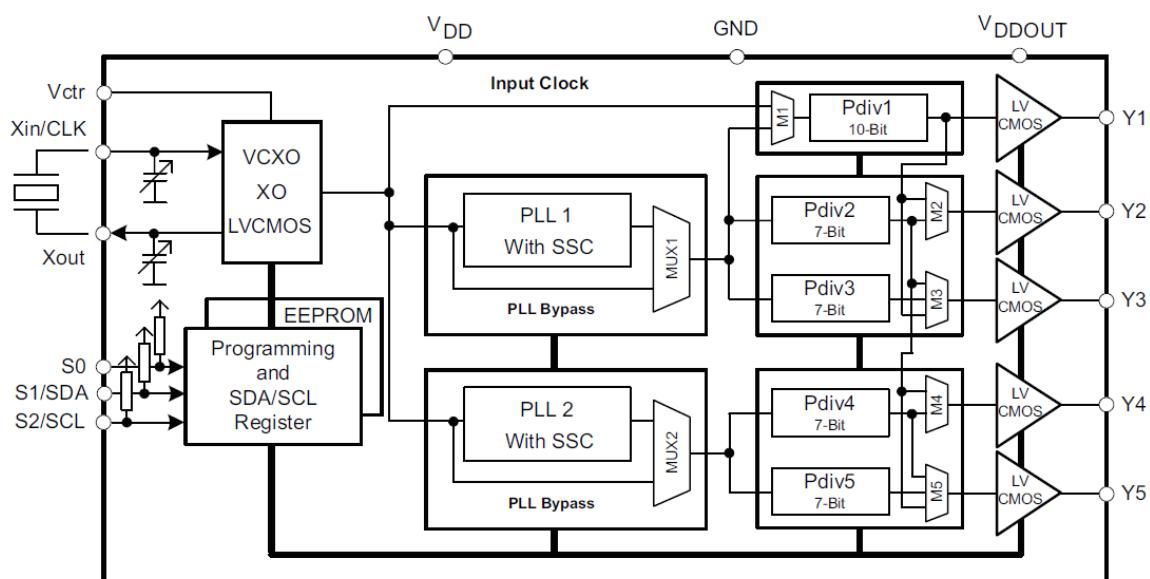


Figure 12: Block diagram of the CDCE925 Clock Generator

This device is configured via I2C to provide the following System Clock Sources:

PLL Output	PLL Num	Connection	Description
Y1	PLL1	HDMI_PCLK_GEN	Clock Source for HDMI-TX (ADV7513)
Y4	PLL2	CAM_A_CLK_GEN	Optional Clock source for Camera daughtercards on CAM_A interface
Y5	PLL2	CAM_B_CLK_GEN	Optional Clock source for Camera daughtercards on CAM_B interface

Table 6: Clock Generator Output Utilisation

5 Auxiliary GPIO Usage

The GPIO allocation on the MV0212 is optimized to support the maximum number of features on this development board. As such there are very few GPIOs remaining for general purpose usage.

To work around this limitation the design makes use of the Auxiliary GPIOs available on the WM8325 power management IC. These GPIOs are accessible via the I2C2 interface to the PMIC.

Some of the pins are used to control static signals such as the Ethernet reset, whereas others are assigned to the daughtercard interfaces for user expansion purposes. It is important to take this into consideration while designing daughtercards, as these I/O pins are most suited for static functions such as reset control. It is not advised to use these pins for functions where low latency operation is a requirement due to the overhead of the I2C communications needed to control them.

A special case is the Ethernet Phy IRQ signal. The intention here is that the PMIC supports a configuration where the GPIO can be configured as an IRQ. When the Ethernet_IRQ is asserted, the PMIC can be configured to signal this event to the Myriad processor using the WM_IRQ output of the PMIC. WM_IRQ is connected to GPIO_28 on myriad.

Furthermore the PMIC has 2 dedicated LED driver pins, these pins are used to directly control LED1 and LED2 on the board. As such, controlling these LEDs requires I2C communication with the PMIC controller.

The following table describes the function of the GPIOs allocated on the PMIC auxiliary interface:

GPIO	Function	Notes
1	WM_PB_1	Push Button
2	WM_PB_2	Push Button
3	WM_SW_1	DIP Switch #1
4	ETH_BOOT	Used to select between ethernet phy powerdown mode and GMII/MII mode
5	HDMI_PD	HDMI TX Power Down Control Signal
6	AP_IO_EXP1	General purpose IO#1 for use by LCD/AP Connector
7	BOOT_CONTROL	Switches between SPI Flash boot and AP SPI on SSO
8	Ethernet RST#	Ethernet PHY Reset control
9	Ethernet IRQ#	Ethernet Interrupt can be routed to WM_IRQ in SW
10	CAM_A IO EXP	General purpose IO for use by Camera A interface
11	CAM_B IO_EXP	General purpose IO for use by Camera B interface
12	AP_IO_EXP2	General purpose IO#2 for use by LCD/AP Connector
LED1	LED1 (D11 on PCB)	Dedicated PMIC LED1 control (Default on)
LED2	LED2 (D12 on PCB)	Dedicated PMIC LED2 control (Default on)

Table 7: PMIC Auxiliary I/O Allocation

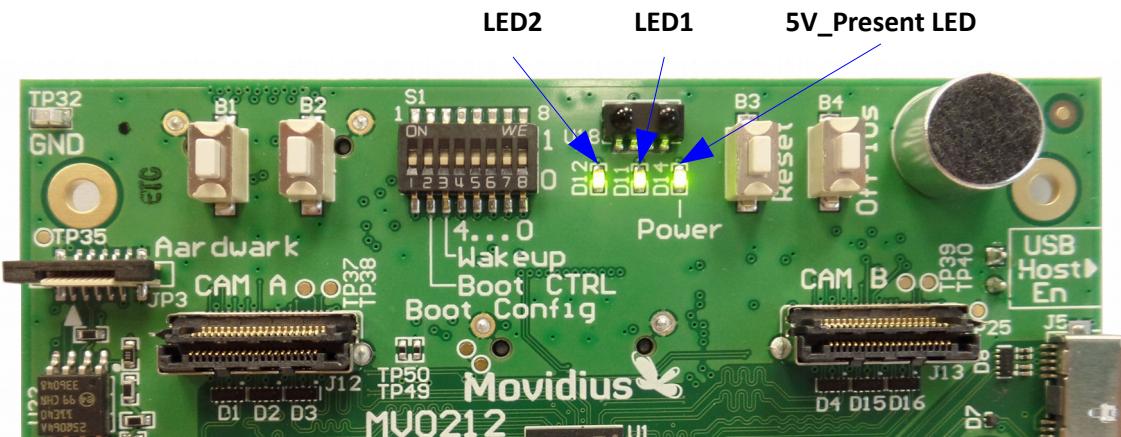


Figure 13: AUX LED Placement

6 USB Subsystem

MV0212 supports USB 3.0 operation and is backwards compatible with earlier USB specifications.

The board supports configuration as either a USB Device or a USB Host (subject to software support), however the user must take care to ensure that the jumper J9 is mounted only when operating in host mode. This jumper provides the 5V VBUS supply which would be needed by external devices in this case.

The USB connector is a USB 3.0 Micro-AB receptacle and as such it is compatible with either USB 3.0 micro B plugs (for normal device mode operation) or USB 3.0 micro-A plugs for operation as a USB 3.0 host.

NOTE: USB 3.0 micro-A plugs should only be used when configured for host operation.

6.1 USB Host Enable Jumper

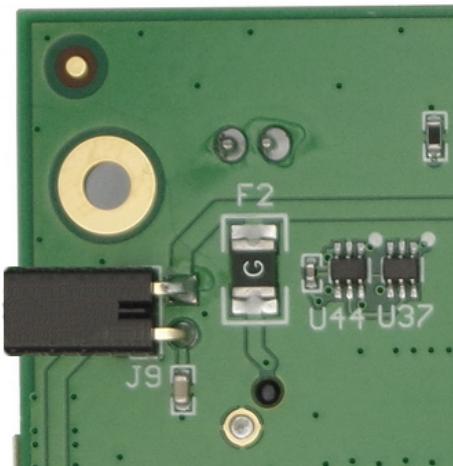


Figure 14: Jumper to Enable USB Host Mode

In order to enable host support Jumper J9 must be mounted to drive 5V out on VBUS as required by the USB host specification.

NOTE: This jumper must never be mounted when operating as a USB device.

6.2 Connecting external USB Devices in host mode and limitations

If the user wishes to configure the MV0212 board as a USB Host, there are a number of limitations that the user needs to consider when operating external USB devices with the MV0212 as a host board.

6.2.1 USB Connector limitations

The MV0212 motherboard provides a USB3.0 Type micro-B female connector at location J5. Unless the USB

device that the user wishes to connect to the board provides a micro-A male or micro-B male connector then a USB adapter cable will be needed.

The following cables have been found to work with external devices:

- PI Manufacturing PN: OTG-USB3-6 (more details at this [link](#)).
- Wurth PN: 692902100000 (more details at this [link](#)).

The latter cable is required for USB3.0 SS support as it provides a cross over between SS TX and RX pins.

6.2.2 USB VBUS limitations

When host mode is enabled (J9 populated), the board 5V input supply is connected directly to the USB external device. It has been found in some cases when an external USB device is connected to the board and host mode is enabled that the resulting inrush current due to the USB external device causes the over-current protection device on the board to activate. This in turn turns off the 5V input to the board and turns back on when the current drops below its trip threshold. This can cause the board to enter a continuous power cycling state that can only be stopped by removing the external USB device.

The suggested mechanism to avoid this if it occurs is to use an externally powered USB hub in order to supply power to the external USB rather than the MV0212 board itself. The hub can then be connected to the USB port J5 as normal.

7 LCD & AP Expansion Port

The LCD & AP Expansion port on the MV0212 development board is intended to facilitate either the connection of TFT LCD panels to the development board or facilitate the interfacing of MV0212 to an Applications Processor (AP) board via a MIPI interface. This section describes this interface and the features it supports.

7.1 LCD & AP Expansion Port Feature Overview

	Feature
Power	Fixed 5V supply
LCD I/F	Dual MIPI D-PHY supporting MIPI DSI / CSI-TX in 1, 2 or 4 lane configuration
GPIO Signals	IRQ from LCD or Applications Processor (AP_IRQ)
Control Bus	<p>2 Pin I2C Interface (MV0212 is Master)</p> <p>SPI Interface (MV0212 is Slave) with SSO, SS1</p> <p>Slave Select 0 is used to Boot Myriad 2 from AP and as control channel from AP to Myriad 2.</p> <hr/> <p>NOTE: Requires appropriate boot switch config.</p> <hr/> <p>Slave Select 1 is reserved for future use.</p>
Reset Control	MB_RESET pin can be pulled low by the AP to reset the MV0212 Board. This can be used to force the Myriad 2 to reboot with a different firmware image.
WAKEUP	The WAKEUP signal to Myriad 2 is normally pulled low by the boot configuration DIP switch to facilitate normal boot. However this signal may be overridden by an AP using this port to utilise its alternate function of waking Myriad from power down mode.
COM_IO	<p>There is a single connection to this connector from the shared COMMON_IO bus using COM_IO1. This can be used as an additional direct GPIO connection to Myriad from the AP, HOWEVER, as this pin is shared with both the CAM_A and CAM_B connectors it is crucial that any applications making use of this feature ensure that the usage of this pin does not conflict with camera daughtercard functionality.</p> <p>As a general rule the use of the COM_IO should be avoided on daughtercard designs unless absolutely necessary. This maximises the flexibility of the system to mix and match different camera and AP expansion daughter-cards.</p>
AP_IO_EXP1/2	These are two general purpose Auxiliary I/O's which are available for use by the AP/LCD interface. They are driven by the PMIC auxiliary I/O function and control of these pins via software requires I2C communication from Myriad to the PMIC. As such they are most useful for functions such as static I/O configuration.

Table 8: LCD Expansion Port Feature Overview

7.2 LCD/AP Expansion Port J10 Pinout

Pin	Signal	Connection	Description	Direction
1	GND	GND	Common Ground	N/A
3	MIPI_PHY0_CLK_N	MIPI_C4_N	MIPI PHY4 Clock Pair	FROM_MV0212
5	MIPI_PHY0_CLK_P	MIPI_C4_P	MIPI PHY4 Clock Pair	FROM_MV0212
7	GND	GND	Common Ground	N/A
9	MIPI_PHY0_D0_N	MIPI_D8_N	MIPI PHY4 Data Pair 0	FROM_MV0212
11	MIPI_PHY0_D0_P	MIPI_D8_P	MIPI PHY4 Data Pair 0	FROM_MV0212
13	GND	GND	Common Ground	N/A
15	MIPI_PHY0_D1_N	MIPI_D9_N	MIPI PHY4 Data Pair 1	FROM_MV0212
17	MIPI_PHY0_D1_P	MIPI_D9_P	MIPI PHY4 Data Pair 1	FROM_MV0212
19	GND	GND	Common Ground	N/A
21	MIPI_PHY1_CLK_N	MIPI_C5_N	MIPI PHY5 Clock Pair	FROM_MV0212
23	MIPI_PHY1_CLK_P	MIPI_C5_P	MIPI PHY5 Clock Pair	FROM_MV0212
25	GND	GND	Common Ground	N/A
27	MIPI_PHY1_D0_N	MIPI_D10_N	MIPI PHY5 Data Pair 0	FROM_MV0212
29	MIPI_PHY1_D0_P	MIPI_D10_P	MIPI PHY5 Data Pair 0	FROM_MV0212
31	GND	GND	Common Ground	N/A
33	MIPI_PHY1_D1_N	MIPI_D11_N	MIPI PHY5 Data Pair 1	FROM_MV0212
35	MIPI_PHY1_D1_P	MIPI_D11_P	MIPI PHY5 Data Pair 1	FROM_MV0212
37	GND	GND	Common Ground	N/A
39	VDD_5V	VDD_5V	5V Power to Daughtercard, Max 0.5A total	FROM_MV0212
2	COM_IO1	GPIO_52	Common general purpose I/O; Shared with CAM_A, CAM_B	BI_DIR (if safe to share)
4	GND	GND	Common Ground	N/A
6	SPI_SCLK	SPI0_SCLK	SPI clock input	TO_MV0212
8	GND	GND	Common Ground	N/A
10	SPI_MISO	SPI0_MISO	SPI MISO	FROM_MV0212
12	GND	GND	Common Ground	N/A
14	SPI莫斯	SPI0莫斯	SPI MOSI	TO_MV0212
16	GND	GND	Common Ground	N/A
18	SPI_SSO	SPI0_SS_0_AP	SPI Slave Select 0 (For boot or AP Uplink communications)	TO_MV0212
20	I2C_SCL	I2C0_SCL	I2C0 Control bus to AP (shared with CAMB)	FROM_MV0212
22	I2C_SDA	I2C0_SDA	I2C0 Control bus to AP (shared with CAMB)	FROM_MV0212
24	GND	GND	Common Ground	N/A
26	MB_RESET	EXT_RST	Reset Input from AP (Active Low)	TO_MV0212
28	AP_IRQ	GPIO_22	IRQ from AP to Myriad	TO_MV0212
30	SPI_SS1	SPI0_SS_1	SPI Slave Select 1 (Reserved for future use)	TO_MV0212
32	MB_WAKEUP	WAKEUP	AP Control of WAKEUP Signal	N/A
34	AP_IO_EXP_1	WM8325_GPIO_6	General purpose I/O from PMIC	FROM_MV0212
36	AP_IO_EXP_2	WM8325_GPIO_12	General purpose I/O from PMIC	FROM_MV0212
38	RESERVED	TP45	Reserved for Future Use	N/A
40	VDD_5V	VDD_5V	5V Power to Daughtercard, Max 0.5A total	FROM_MV0212

Table 9: LCD Expansion Port Pinout

NOTE: All digital logic signal levels are based on 1.8V I/O logic unless otherwise specified.

8 Camera Expansion Port

The Camera Expansion port on the MV0212 development board is intended to facilitate the connection of either single or dual MIPI camera modules to the development board. This section describes this interface and the features it supports.

NOTE: All digital logic signal levels are based on 1.8V I/O logic unless otherwise specified.

8.1 Camera Expansion Port Feature Overview

	Feature
Power	Fixed 5V supply
MIPI I/F	The CAM A interface supports a single MIPI CSI camera in either 1, 2 or 4 lane configuration.
	The CAM B interface supports up to two MIPI CSI cameras each with either 1 or 2 MIPI lane support.
GPIO Signals	Each Camera interface has a two dedicated Myriad GPIOs, one of which has support for GPIO_PWM output mode; CAM_A_GPIO0 -> GPIO_59 CAM_A_PWM -> GPIO_27 CAM_B_GPIO0 -> GPIO_15 (Note: Also optionally UART_TX) CAM_B_PWM -> GPIO_33 (Note: Also optionally UART_RX)
Control Bus	2 Pin I2C Interface (MV0212 is Master)
	CAM_A uses I2C1 (dedicated)
	CAM_B uses I2C0 (Shared only with LCD/AP I2C interface)
Clock Source	Each Camera Interface has a dedicated clock source from the MV0212 CDCEL925 external PLL (CAM_A_CLK_GEN, CAM_B_CLK_GEN). Typically this clock source is used to provide a master clock to camera sensors.
COM_IO	Each camera interface shares 5 common GPIOs as part of the COM_IO bus. The shared nature of these GPIOs is a compromise between the shortage of free GPIOs on the overall design and the need for maximum flexibility on Camera and AP daughtercards. Please see section 9.2 for important notes on the use of these pins.
CAM_A_IO_EXP CAM_B_IO_EXP	These are two dedicated general purpose Auxiliary I/O's which are available for use by the camera interface. They are driven by the PMIC auxiliary I/O function and control of these pins via software requires I2C communication from Myriad to the PMIC. As such they are most useful for functions such as control of static signals (e.g. reset)

Table 10: Camera Expansion Port Feature Overview

8.2 Camera A Expansion Port (J12) Pinout

Pin	Signal Name	Connection	Description	Direction
1	GND	GND	Common Ground	N/A
3	MIPI_PHY0_CLK_N	MIPI_CO_N	PHY0 Clock Pair	TO_MV0212
5	MIPI_PHY0_CLK_P	MIPI_CO_P	PHY0 Clock Pair	TO_MV0212
7	GND	GND	Common Ground	N/A
9	MIPI_PHY0_D0_N	MIPI_DO_N	PHY0 Data0 Pair	TO_MV0212
11	MIPI_PHY0_D0_P	MIPI_DO_P	PHY0 Data0 Pair	TO_MV0212
13	GND	GND	Common Ground	N/A
15	MIPI_PHY0_D1_N	MIPI_D1_N	PHY0 Data1 Pair	TO_MV0212
17	MIPI_PHY0_D1_P	MIPI_D1_P	PHY0 Data1 Pair	TO_MV0212
19	GND	GND	Common Ground	N/A
21	RESERVED 3		NOT CONNECTED	N/C
23	RESERVED 4		NOT CONNECTED	N/C
25	GND	GND	Common Ground	N/A
27	MIPI_PHY1_D0_N	MIPI_D2_N	PHY1 Data0 Pair	TO_MV0212
29	MIPI_PHY1_D0_P	MIPI_D2_P	PHY1 Data0 Pair	TO_MV0212
31	GND	GND	Common Ground	N/A
33	MIPI_PHY1_D1_N	MIPI_D3_N	PHY1 Data1 Pair	TO_MV0212
35	MIPI_PHY1_D1_P	MIPI_D3_P	PHY1 Data1 Pair	TO_MV0212
37	GND	GND	Common Ground	N/A
39	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0212
2	CAM_COM_IO1	GPIO_52	General purpose I/O; Shared with CAM_B, AP, BOOT1	FROM_MV0212 (if safe to share)
4	GND	GND	Common Ground	N/A
6	CAM_COM_IO2	GPIO_53	General purpose I/O; Shared with CAM_B, BOOT2	FROM_MV0212 (if safe to share)
8	GND	GND	Common Ground	N/A
10	CAM_COM_IO3	GPIO_54	General purpose I/O; Shared with CAM_B, AP	BI_DIR (if safe to share)
12	GND	GND	Common Ground	N/A
14	CAM_COM_IO4	GPIO_55	General purpose I/O; Shared with CAM_B, PWR_MON	BI_DIR (if safe to share)
16	GND	GND	Common Ground	N/A
18	CAM_COM_IO5	GPIO_56	General purpose I/O; Shared with CAM_B, BOOT3	FROM_MV0212 (if safe to share)
20	I2C_SCL	I2C1_SCL	I2C Control Bus for Camera	FROM_MV0212
22	I2C_SDA	I2C1_SDA	I2C Control Bus for Camera	FROM_MV0212
24	GND	GND	Common Ground	N/A
26	CAM_CLK_GEN	CDCEL925PW_Y4	Clock Source for camera daughterboard, configured via i2c	FROM_MV0212
28	CAM_GPIO	GPIO_59	Dedicated daughterboard GPIO	BI_DIR
30	CAM_PWM	GPIO_27	Dedicated daughterboard GPIO+PWM	BI_DIR
32	RESERVED5	N/C	Reserved for future use	N/A
34	CAM_IO_EXP_1	WM8325_GPIO_10	Dedicated AuxiGPIO, I2C config	FROM_MV0212
36	RESERVED1	TP37	Reserved for future use	N/A
38	RESERVED2	TP38	Reserved for future use	N/A
40	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0212

Table 11: Camera Expansion Port Pinout

8.3 Camera B Expansion Port (J13) Pinout

Pin	Signal Name	Connection	Description	Direction
1	GND	GND	Common Ground	N/A
3	MIPI_PHY0_CLK_N	MIPI_C2_N	PHY2 Clock Pair	TO_MV0212
5	MIPI_PHY0_CLK_P	MIPI_C2_P	PHY2 Clock Pair	TO_MV0212
7	GND	GND	Common Ground	N/A
9	MIPI_PHY0_D0_N	MIPI_D4_N	PHY2 Data0 Pair	TO_MV0212
11	MIPI_PHY0_D0_P	MIPI_D4_P	PHY2 Data0 Pair	TO_MV0212
13	GND	GND	Common Ground	N/A
15	MIPI_PHY0_D1_N	MIPI_D5_N	PHY2 Data1 Pair	TO_MV0212
17	MIPI_PHY0_D1_P	MIPI_D5_P	PHY2 Data1 Pair	TO_MV0212
19	GND	GND	Common Ground	N/A
21	MIPI_PHY1_CLK_N	MIPI_C3_N	PHY3 Clock Pair	TO_MV0212
23	MIPI_PHY1_CLK_P	MIPI_C3_P	PHY3 Clock Pair	TO_MV0212
25	GND	GND	Common Ground	N/A
27	MIPI_PHY1_D0_N	MIPI_D6_N	PHY3 Data0 Pair	TO_MV0212
29	MIPI_PHY1_D0_P	MIPI_D6_P	PHY3 Data0 Pair	TO_MV0212
31	GND	GND	Common Ground	N/A
33	MIPI_PHY1_D1_N	MIPI_D7_N	PHY3 Data1 Pair	TO_MV0212
35	MIPI_PHY1_D1_P	MIPI_D7_P	PHY3 Data1 Pair	TO_MV0212
37	GND	GND	Common Ground	N/A
39	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0212
2	CAM_COM_IO1	GPIO_52	General purpose I/O; Shared with CAM_A, AP, BOOT1	FROM_MV0212 (if safe to share)
4	GND	GND	Common Ground	N/A
6	CAM_COM_IO2	GPIO_53	General purpose I/O; Shared with CAM_A, BOOT2	FROM_MV0212 (if safe to share)
8	GND	GND	Common Ground	N/A
10	CAM_COM_IO3	GPIO_54	General purpose I/O; Shared with CAM_A, AP	BI_DIR (if safe to share)
12	GND	GND	Common Ground	N/A
14	CAM_COM_IO4	GPIO_55	General purpose I/O; Shared with CAM_A, PWR_MON	BI_DIR (if safe to share)
16	GND	GND	Common Ground	N/A
18	CAM_COM_IO5	GPIO_56	General purpose I/O; Shared with CAM_A, BOOT3	FROM_MV0212 (if safe to share)
20	I2C_SCL	I2C0_SCL	I2C Control Bus for Camera	FROM_MV0212
22	I2C_SDA	I2C0_SDA	I2C Control Bus for Camera	FROM_MV0212
24	GND	GND	Common Ground	N/A
26	CAM_CLK_GEN	CDCEL925PW_Y5	Clock Source for camera daughterboard, configured via i2c	FROM_MV0212
28	CAM_GPIO	GPIO_15	Dedicated Camera daughterboard GPIO	BI_DIR
30	CAM_PWM	GPIO_33	Dedicated Camera daughterboard GPIO with PWM Support	BI_DIR
32	RESERVED3	TP39	Reserved for future use	N/A
34	CAM_IO_EXP_1	WM8325_GPIO_11	Dedicated Auxiliary GPIO, configured via I2C	FROM_MV0212
36	RESERVED1	TP39	Reserved for future use	N/A
38	RESERVED2	TP40	Reserved for future use	N/A
40	VDD_5V	VDD_5V	5V Power to D/c, Max 0.5A total	FROM_MV0212

Table 12: Camera Expansion Port Pinout

9 Daughtercard Design Considerations

9.1 AP Uplink and Camera Interface MIPI connections Diagram

The following diagram illustrates at block level how the Camera and AP uplink connections are made to Myriad 2. The diagram illustrates how the following use case would be achieved using the MV0212:

- Daughtercard with 4 lane MIPI camera connected to the CAM_A Interface
- Daughtercard with dual 2 lane MIPI cameras connected to the CAM_B Interface.
- Daughtercard which provides uplink to an Applications processor using a 4 lane MIPI configuration

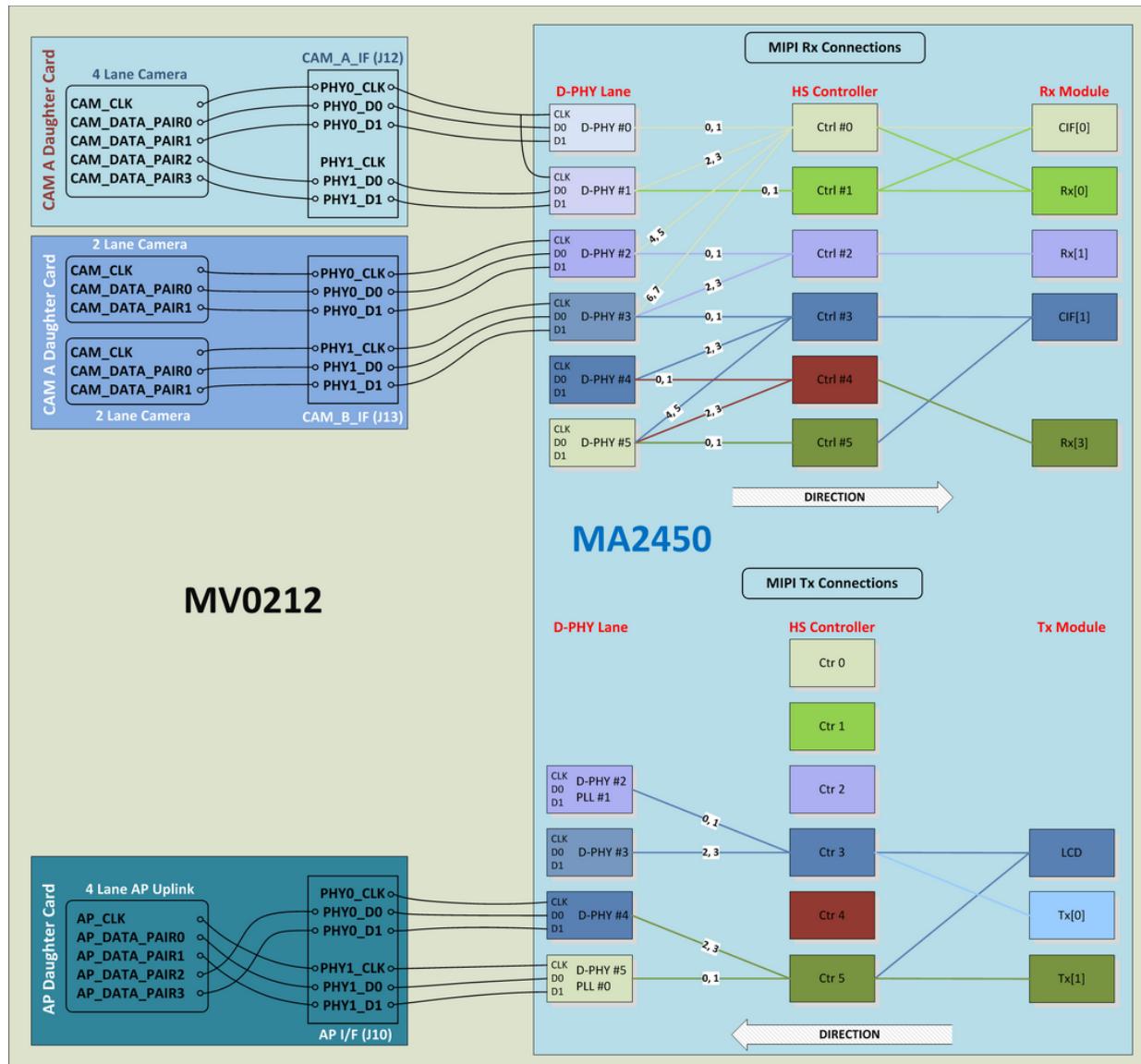


Figure 15: MV0212 MIPI Connections Example

Some Important points to note:

- The MIPI TX for D-PHY4,5 has reversed numbering 0,1 then 2,3 (see [Figure 15](#) above)
 - As such the AP Uplink Pair 0,1 are connected to D-PHY5 and Pairs 2,3 are connected to DPHY4
 - The clock source must come from D-PHY#5 as it is the only connected D-PHY containing a PLL
- It is not possible to build an AP daughtercard that supports a dual 2 lane MIPI output
 - This is because D-PHY4 does not contain an independent means of generating a clock
- The 4 lane MIPI-RX use case illustrated on the CAM_A interface shows a connection between DPHY-0 CLK and DPHY-1 CLK. This is needed to support 4 lane MIPI operation. This connection is made on the MV0212 motherboard directly under the Myriad 2 BGA balls as directed in the Myriad 2 platform datasheet.

9.2 Common I/O Bus Description

The MV0212 design maximizes the use of system GPIOs to support as many features as possible on this development platform.

This design goal means that there are very few GPIOs remaining for allocation to the various expansion interfaces (CAM_A, CAM_B, AP/LCD, POWER_MON). In order to maximize the flexibility of the expansion interface while working within the constraints of limited GPIOs, the decision was made to share 5 GPIOs between the 3 expansion headers.

This has the benefit of allowing certain expansion cards to use a maximum number of GPIOs when needed, but does so at the cost of introducing potential incompatibilities between different daughtercard configurations.

The general advice is that daughtercard designers should avoid the use of these common IO pins unless absolutely necessary for the application. For example it is better to use CAM_A_IO_EXP as a camera sensor reset control than use COM_IO1 for this purpose. Daughtercards which do not use any of the shared resources can safely be combined in any combination, however if the shared resources have been used then the user must take care to avoid any resource conflicts.

In addition to the constraints placed on these I/O's due to sharing across the expansion ports, further constraints result from the fact the 3 of the pins also double as boot pins. Please see section [3.1.1](#) for details of the specific constraints this imposes.

The following table provides a breakdown of the functions of the COM_IO bus and illustrates which pins are shared on each interface.

Signal	GPIO	CAM_A	CAM_B	AP_LCD	PWR_MON	Function A	Function B	Function C
COM_IO_1	gpio_52	2	2	2	-	BOOT1	GPIO_OUT	cpr_io_clk_3
COM_IO_2	gpio_53	6	6	-	-	BOOT2	GPIO_OUT	-
COM_IO_3	gpio_54	10	10	-	-	-	GPIO_IN_OUT	-
COM_IO_4	gpio_55	14	14	-	30	-	GPIO_IN_OUT	-
COM_IO_5	gpio_56	18	18	-	-	BOOT3	GPIO_OUT	-

Table 13: Common IO Function Sharing Breakdown

9.3 Mating Connector Descriptions

The MV0212 is designed with a view to having daughtercards which are mounted using a direct PCB to PCB

mounting strategy. To achieve the correct PCB Mating height Movidius recommends the use of the following connector type for MV0212 daughtercard designs:

Manufacturer	Part Number	Distributor	Part Number
Samtec	LSHM-120-06.0-L-DV	Farnell	2433941

Table 14: Recommended Daughtercard Connector Specification

For diagnostic or debug purposes Samtec also produce a cable that is compatible with this connector type.

Manufacturer	Part Number	Distributor	Part Number
Samtec	HLCR-20-09.80-BD-TD-2	Samtec Direct	N/A

Table 15: Recommended Daughter card Connector Specification

9.4 Connector Pin Numbering Convention

The MV0212 design uses a common connector for each daughtercard interface.

This connector is a hermaphroditic connector and as such it is important that a common convention is adopted to ensure the correct connection of daughtercard signals.

The following convention has been adopted by Movidius for the MV0212 design:

- In order to keep the schematic symbol the same for both motherboards and daughtercards Movidius opted to use different footprints on motherboard and daughtercard PCBs.
- To keep things easy for external daughtercard designers, the official pinout (as described in the Samtec datasheet) is used for all daughtercard layouts.
- As such only the Movidius MV0212 motherboard uses this non-standard footprint.
- To ensure compatibility daughtercard designers should only need to apply the following two steps:
 1. Use the same schematic symbol for daughtercard designs as in the MV0212 Schematics
 2. Follow the default layout footprint guidelines as documented by Samtec.
- The pin numbering will then match that of the schematic symbol, e.g. MIPI_PHY0_CLK_N goes to pin 3 for camera daughtercard designs.

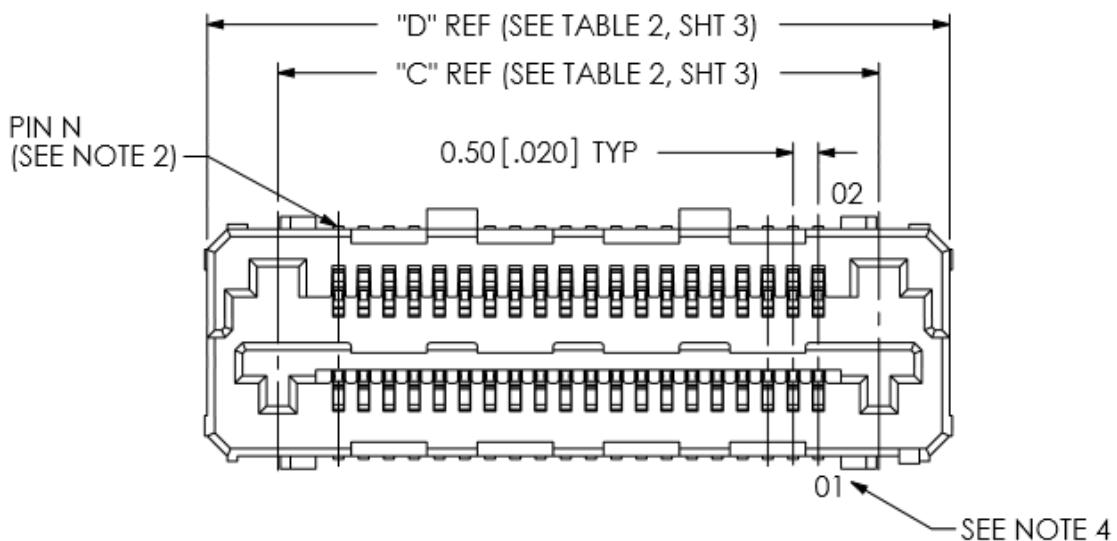


Figure 16: Example Samtec Footprint Recommendation

9.5 Daughtercard Mechanical Specification

This section provides mechanical details of the PCB hole placement and connector positions.

This mechanical specification is fully backwards compatible with MV0182.

Please see section 11 for details of other aspects of the mechanical specification.

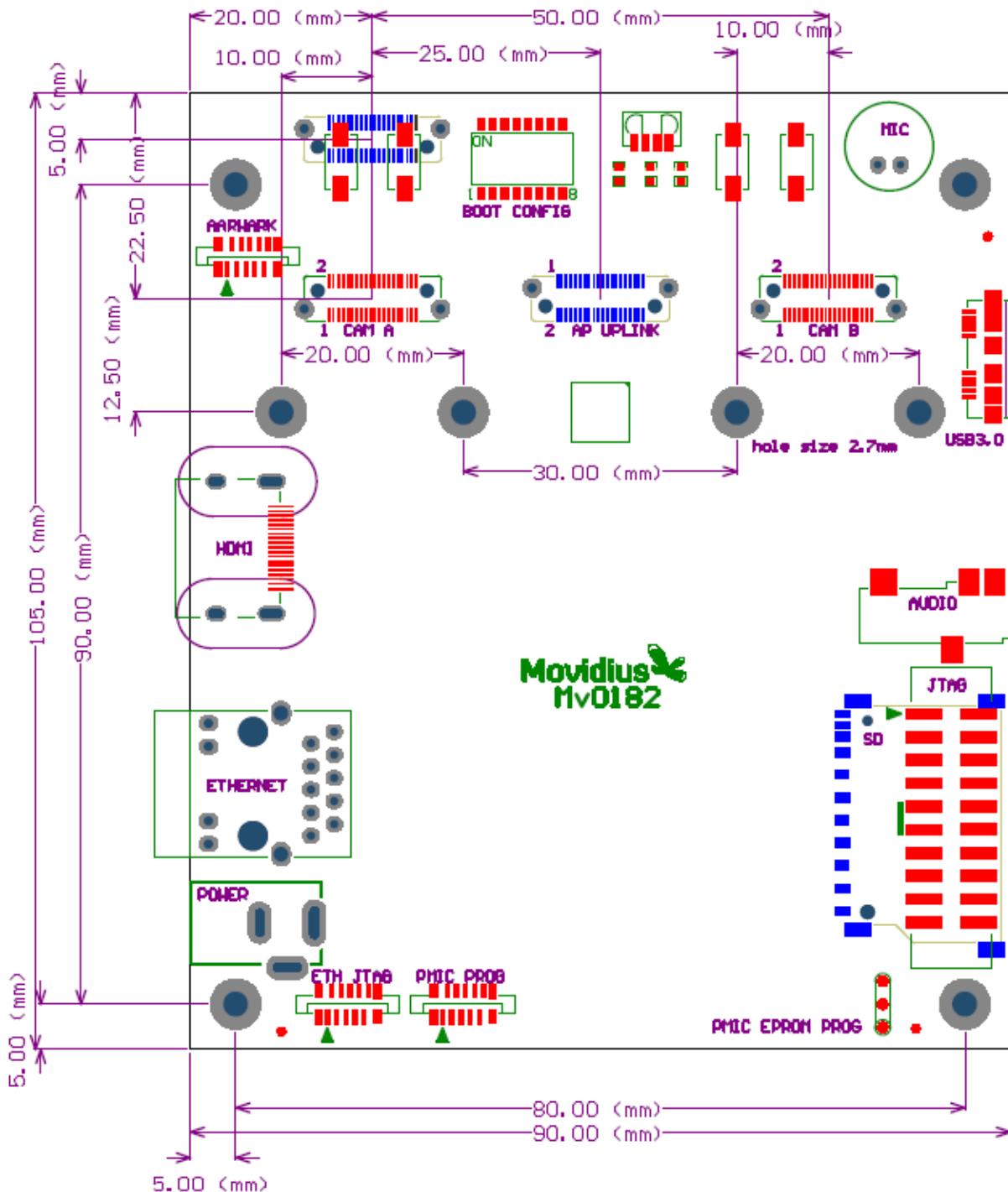


Figure 17: MV0212 Board Mechanical Specification

10 Known Limitations MV0212

This section details the known issues with the MV0212 design. It documents the severity of each issue any known workarounds if applicable. If issues have been resolved in subsequent PCB revisions this is noted in the solution field.

The scope of this document is limited to the hardware features of this board. It makes no reference to any software or driver limitations, as any such issues are documented as part of the general MDK software deliverable package.

10.1 Design Errata

10.1.1 MV0212-R1-1

Name	Misleading text on Schematic page 10
Severity	Low
Description	<p>Page 10 of the schematic has the following text: “if RZ52 is mounted then BMI160 will use I2C - unmount for SPI”</p> <p>This text is found beside U21 BMI160. It incorrectly implies that it is possible to operate U21 from SPI rather than I2C. This is not correct as there are no SPI connections to this IC.</p>
Limitation	No functional limitation. This is purely a cosmetic issue.
Solution	This text will be removed in the event of any subsequent respin of this board.

11 Reference Documentation

This section details the supporting documentation provided with the MV0212 Development Boards.

All paths described are relative to the root of the extracted content from the movidius.org MV0212 documentation package.

Location	Description
MV0212_R0M0E0_Release\assembly	PDF Assembly Drawing. ODB Machine Assembly Database. Pick & Place Data.
MV0212_R0M0E0_Release\BOM	Full Bill of Materials (XLS format). NOTE: (NM) variant is the subset of components which are mounted
MV0212_R0M0E0_Release\design	ZIP File containing all source design files in Altium Designer 10 Format.
MV0212_R0M0E0_Release\gerber	Full PCB Gerber and NC_Drill files.
MV0212_R0M0E0_Release\Layout	PDF version of Layout (all layers).
MV0212_R0M0E0_Release\mechanical	Documents outlining the mechanical specification for the board and including example mechanical specifications for camera daughtercards.
MV0212_R0M0E0_Release\Schematic	PDF Version of the released schematics. NOTE: (NM) variant is the schematic showing which subset of components which are mounted.
MV0212_R0M0E0_Release\Pmic_eeprom	Contents of the Power management IC EEPROM (U43) configuration in Intel Hex format.

Table 16: Reference Documentation