

SWITCHED CAPACITOR STEP UP SINGLE PHASE 5 LEVEL INVERTER FOR PV APPLICATION

PROJECT REPORT

Submitted by

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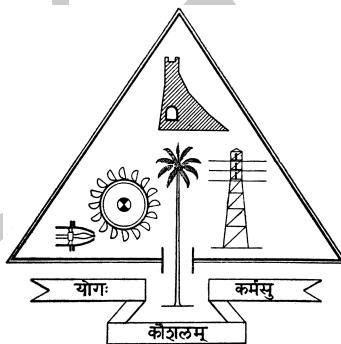
The APJ Abdul Kalam Technological University
in partial fulfillment of the requirements for the award of the degree

of

Bachelor of Technology

in

Electrical and Electronics Engineering



**Department of Electrical Engineering
Government Engineering College, Thrissur**

JUNE - 2023

DECLARATION

We undersigned hereby declare that the project report (“Switched Capacitor Step Up Single Phase 5 Level Inverter for PV application”), submitted for partial fulfillment of the requirements for the award of degree of Bachelor of Technology of the APJ Abdul Kalam Technological University, Kerala is a bonafide work done by us under supervision of T.G. SANISH KUMAR, Associate Professor, Government Engineering College, Thrissur. This submission represents our ideas in our own words and where ideas or words of others have been included; we have adequately and accurately cited and referenced the original sources. We also declare that we have adhered to ethics of academic honesty and integrity and have not misrepresented or fabricated any data or idea or fact or source in our submission. We understand that any violation of the above will be a cause for disciplinary action by the institute and/or the University and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been obtained. This report has not been previously formed the basis for the award of any degree, diploma or similar title of any other University.

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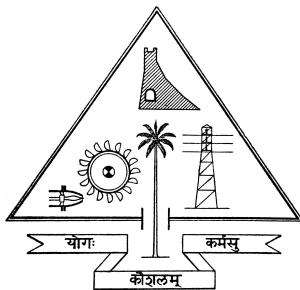
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CERTIFICATE

This is to certify that the Project Report titled "**SWITCHED CAPACITOR STEP UP SINGLE PHASE 5 LEVEL INVERTER FOR PV APPLICATION**" is a bonafide record of the work carried out by **ADHEEB SHIBU VATTASSERIL (TCR19EE008)**, **BASTIN BABU C (TCR19EE034)**, **CHARLES GEORGE (TCR19EE037)**, **ANOOP K.C (TCR19EE025)** to the APJ Abdul Kalam Technological University in partial fulfillment of the requirements for the award of the Degree of Bachelor of Technology (Electrical and Electronics Engineering) is a bonafide record of the project work carried out by them under my guidance and supervision. This report in any form has not been submitted to any other University or Institute for any purpose.

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ACKNOWLEDGEMENT

During the course of my project work several persons collaborated directly and indirectly with me. Without their support it would be impossible for me to finish my work. That is why I wish to dedicate this section to recognize their support.

I want to start expressing my thanks to my project guide **T.G Sanish Kumar**, Associate Professor Dept. of Electrical Engineering, because of his valuable advice and guidance towards this work. I received motivation; encouragement and hold up from his during the course of work.

I am thankful to **Dr. E.A Jasmin**, Head of the Department, and our Principal **Dr Satish K P**, for their sole co-operation.

I am grateful to express my thanks to all the faculty members of our department for their support. I articulate my gratitude to all my associates and colleagues for their support and help for this work.

Last, but not the least I wish to express my gratitude to God Almighty for His abundant blessings without which this effort would not have been successful.

ABSTRACT

Multilevel inverters are power electrical devices that can use several lower level DC voltages as inputs to produce the desired output. Because they can create a smoother stepped output waveform, multilevel inverters are becoming more and more preferred than traditional two level inverters. Additionally, the output from multilevel inverters has fewer harmonic distortions and dv/dt. Typically, diode clamped, flying capacitor, or cascaded H-bridge topologies are used in multilevel inverters. These topologies include drawbacks such as a huge number of components, high size, expense, and complexity of control. The purpose of this project is to utilise a switched capacitance (SC) structure to get around the drawbacks of the current topologies. This project work involves the simulation and hardware implementation of switched Capacitor Step Up Single Phase 5 Level Inverter for PV application.

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Chapter 1

INTRODUCTION

1.1 General Background

Researchers have recently begun to pay greater attention to multilevel inverters (MIs) because of benefits like improved waveform quality, reduced EM noise, and less device stress. For applications like electric motor drivers, uninterruptible power supply, and distributed generation systems, MIs are used to couple a DC source to an AC bus. In current usage are the following topologies:

- 1)Neutral-point clamped (Diode clamped).
- 2)Flying capacitor.
- 3)Cascaded H-bridge (CHB).

1.2 Objective

For low-power applications, the system size and cost are the main concerns. Problems in multilevel inverters (MIs) employing current topologies are the following:-

- 1)Large number of components(switches, power supplies, capacitors, and diodes).
- 2)Large size and high cost.
- 3)Complex control.

A new MI topology that employs a Switched Capacitor(SC) structure in cascade with an H-bridge offers a solution to the issue. The goal of this new system is to produce a SC-MI that has the following qualities:

- 1)Fewer components(switches, sources and capacitors).
- 2)Smaller and less expensive.
- 3)Less complex control.
- 4)Requires only one power DC source.
- 5)Boost operation without magnetic elements.

1.3 Scope

Multi-level inverters have a bright future. Future electronic devices that might be made completely of ICs and other microprocessors would need to meet extremely high criteria of power quality that might not be feasibly envisioned with the inverter topologies currently in use. The current MI topologies are also expensive, difficult to regulate, and big. However, the switched capacitance architecture is inexpensive and simple to regulate while utilising fewer switches. Multi-level inverters may replace single-level inverters as the dominant inverter technology in the expanding electronic industry with more research and development.

1.4 Requirements

Software Requirements

- MATLAB (Simulation)
- Latex (Documentation)

Chapter 2

LITERATURE SURVEY

The Multilevel inverter is a novel concept emerging as a promising advancement in the field of inverters since they provide features like fewer components, smaller and less expensive system, less complex control, etc. The existing researches have implemented multilevel inverters using techniques like cascaded H-bridge, diode clamped, flying capacitor structure, etc. Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating.

Balancing among dc link and clamping capacitors exists in both neutral point clamped and flying capacitor inverters. Diode clamped or neutral clamped has the difficulty of increase in the number of clamping diodes as the level increases. Similarly, in flying capacitor the number of capacitors increases and system becomes bulkier. Among these inverter topologies cascaded inverter achieves greater reliability and simplicity.

A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The most attractive features of a multilevel inverter are as follows:

- 1) They can generate output voltages with extremely low distortion and lower dv/dt.
- 2) They draw input current with very low distortion.
- 3) They generate smaller common-mode (CM) voltage.
- 4) They can operate with a lower switching frequency.

Multilevel inverters have an arrangement of power switching devices and capacitor voltage sources. Multilevel inverters are suitable for high-voltage applications because of their ability to synthesize output voltage waveforms with a better harmonic spectrum and attain higher voltages with a limited maximum device rating.

There are three main types of multilevel inverters: diode-clamped (neutral-clamped), capacitor-clamped (flying capacitors), and cascaded H-bridge inverter.

2.1 Diode Clamped Structure

The diode-clamped inverter is also known as the neutral-point clamped inverter (NPC) which was introduced by Nabae et al (1981). The diode-clamped inverter consists of two pairs of series switches (upper and lower) in parallel with four series capacitors. Clamping diodes are used to connect neutral point at the middle point of capacitors to the respective points between the switches. For a five level inverter three neutral points are available. The upper and lower pair of switches are complimentary in nature. Thus any four switches will be in ON state at any point of time. Since the upper part of switches operate for long duration of time, switches with different current ratings are used. All five levels of output can be generated by turning switches ON & OFF appropriately.

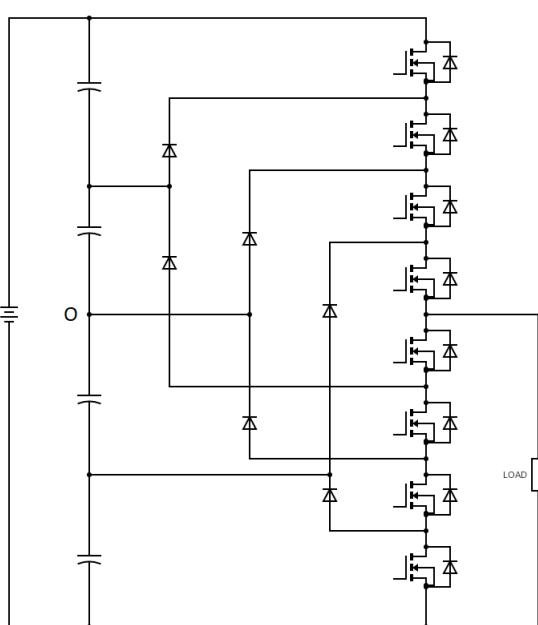


Figure 2.1: Five Level Diode Clamped Multi Level Inverter

The middle point of the two capacitors can be defined as the “neutral point”. The NPC uses a single dc bus that is subdivided into a number of voltage levels by a series string of capacitors. For a five-level diode-clamped inverter if the point O is taken as the ground reference, the output voltage has five states $0, +1V_{dc}, +2V_{dc}, -1V_{dc}$ and $-2V_{dc}$. The voltage levels across the given load are : $0, +1V_{dc}, +2V_{dc}, +3V_{dc}$ and $+4V_{dc}$. Three phases are necessary to generate a three-phase voltage.

The disadvantages of this system are,

- (1) Different voltage ratings for clamping diodes are required.
- (2) Real power flow is difficult because of the capacitors imbalance.
- (3) Need high voltage rating diodes to block the reverse voltages.
- (4) The number of switches, capacitors, and diodes required in the circuit increases with the increase in the number of output voltage levels.

Generalizing the diode clamped inverter for "m" levels:

$$\text{number of clamping points} = m-2$$

$$\text{number of diodes} = (m-1)(m-2)$$

$$\text{number of capacitors} = m-1$$

$$\text{number of switches} = 2(m-1)$$

2.2 Flying Capacitor Inverter

Capacitor-clamped multilevel inverter topologies are relatively new compared to the diode-clamped or the cascaded H-bridge cell inverter topologies. Redundancy in the switching states is available by using flying capacitors instead of clamping diodes. This redundancy can be used to regulate the capacitor voltages and obtain the same desired level of voltage at the output. Figure 2.2 shows a single-phase five-level capacitor-clamped multilevel inverter topology. The voltage across the capacitors is considered to be half of DC source voltage V_{dc} . The output voltage consists of five different voltage levels, $0, +1/2V_{dc}, -1/2V_{dc}, +V_{dc}, -V_{dc}$. Similar to the other multilevel inverter topologies, capacitor clamped multilevel inverter also has complementary pairs of switches. The number of switching states for the capacitor-clamped multilevel inverter topology is higher than that of the diode-clamped inverter. The number of voltage levels at the output can be increased by adding a pair of complementary switches and a capacitor. An output voltage can be produced by using different combinations of switches. The topology allows

increased flexibility in how the majority of the voltage levels may be chosen. In addition, the switches may be chosen to charge or discharge the clamped capacitors, which balance the capacitor voltage.

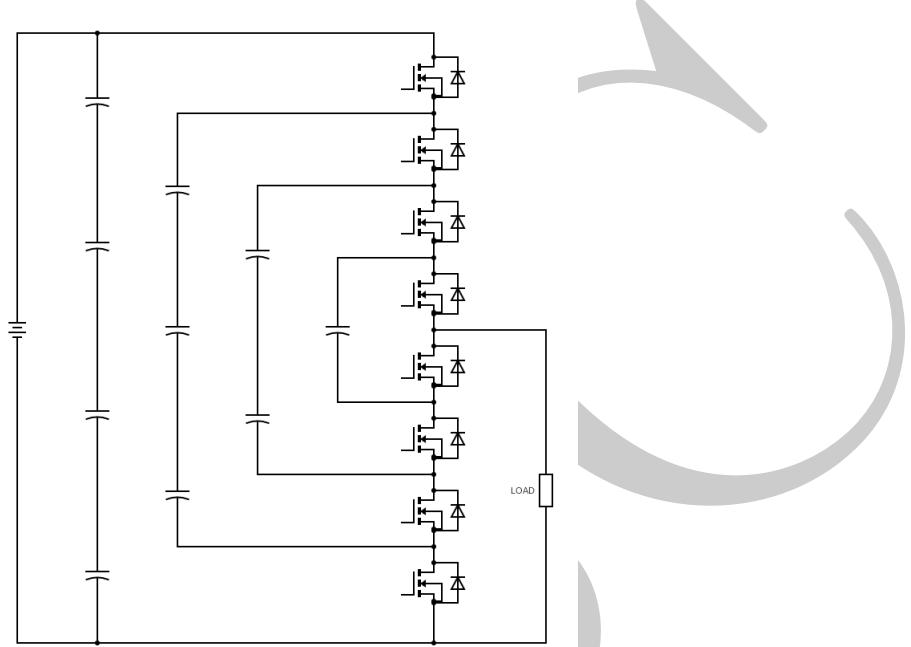


Figure 2.2: Flying Capacitor Multilevel Inverter

The disadvantages are,

- (1) Large numbers of capacitors are bulky and more expensive than the clamping diodes used in the diode-clamped multilevel inverter.
- (2) Complex control is required to maintain the capacitor's voltage balance.
- (3) Switching utilization and efficiency are poor for real power transmission.

Generalizing the flying capacitor inverter for "m" levels:

$$\text{number of flying capacitors} = \frac{(m-1)(m-2)}{2}$$

$$\text{number of main capacitors} = m-1$$

$$\text{number of switches} = 2(m-1)$$

2.3 Cascaded H-Bridge Inverter

The cascaded H-bridge inverter has drawn tremendous interest due to the greater demand of medium-voltage high-power inverters. The cascaded inverter uses series strings of single-phase full-bridge inverters

to construct multilevel phase legs with separate dc sources. The output of each H-bridge can have three discrete levels, results in a staircase waveform that is nearly sinusoidal even without filtering. A single H-bridge is a three-level inverter. Each single-phase full-bridge inverter generates three voltages at the output: $+V_{dc}$, 0 and $-V_{dc}$. The four switches S_1 , S_2 , S_3 and S_4 are controlled to generate three discrete outputs out V with levels $+V_{dc}$, 0 and $-V_{dc}$. When S_1 and S_4 are on, the output is V_{dc} ; when S_2 and S_3 are on, the output is $-V_{dc}$. Here two single H-Bridges are connected series to get five different voltage levels. Different combinations of single level H-Bridge can produce voltages of $+2V_{dc}$, $+1V_{dc}$, 0, $-V_{dc}$ and $-2V_{dc}$

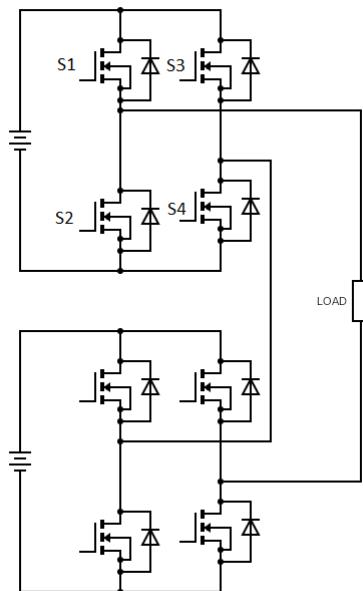


Figure 2.3: Cascaded H-Bridge Inverter

The disadvantage for cascaded multilevel H-bridge inverter is the following:

- (1) Needs separate DC sources.
- (2) Needs large number of switches.

Generalizing the H-Bridge inverter for "m" levels:

$$\text{Number of switches} = 2(m-1)$$

$$\text{Number OF DC Sources} = (m-1)/2$$

This project presents a multilevel inverter based on switched capacitance structure which can generate a greater number of voltage levels with optimum number of components.

Chapter 3

SWITCHED CAPACITOR FIVE LEVEL INVERTER

This chapter discusses the working of a switched capacitor based five level inverter with reduced switch count and a single DC source. It also explains the phase disposition PWM technique used to generate the switching signals for the inverter.

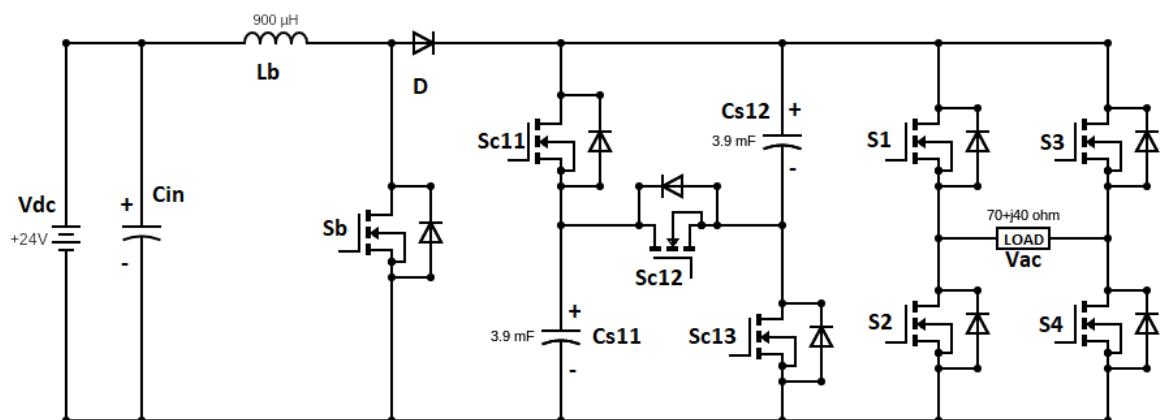


Figure 3.1: Switched Capacitor 5-level inverter circuit

The proposed inverter consists of a single DC source, single SC cells connected in parallel with the H-bridge circuit and a load. The SC cell in combination with the boost circuit provides the required input for the H- bridge inverter circuit. The DC-DC converter boosts the input DC voltage to a higher level. This is necessary because the switched capacitor network and the inverter stage require a higher voltage

to operate effectively. The switched capacitor network synthesizes a 5 level AC voltage from the boosted DC voltage, and the inverter stage converts this 5 level AC voltage into a single phase AC output. Considerations include the switching frequency, the switching losses, and the efficiency of the inverter. The switching of the elements are driven by the gate drive circuits developed by PWM technique. A control logic is implemented to generate the switching signals. A comparison of the number of components used in realising a 5 level inverter using switched capacitor structure and other conventional topologies are summarised in the table below.

Topology	Capacitor	Diode	Switch	DC Source
Switched Capacitor MLI	3	1	7	1
Flying Capacitor MLI	10	0	8	1
Cascaded H-Bridge MLI	0	0	8	2

Table 3.1: Comparison of the number of components in a 5 level inverter

3.1 Design

SPECIFICATION	VALUE
Input Voltage (V_{dc})	24V
Boost circuit output (V_{in})	72V
Input Current (I_{dc})	4.2A
Output Current (I_{in})	1.2A
Switching frequency(f_{SW})	20KHz
Modulation Index(M)	.95
Current Ripple(ΔI)	0.21A
Voltage Ripple(ΔV)	0.72A
Capacitor Discharging Value(Q_N)	0.2C

Table 3.2: Design specification

3.1.1 Boost Circuit

The boost converter is a DC-to-DC converter designed to perform the step-up conversion of applied DC input. In the Boost converter, the supplied fixed DC input is boosted (or increased) to adjustable DC output voltage i.e. output voltage of the boost converter is always greater than the input voltage. So, a Boost converter is also called a step-up converter or step-up chopper. The inductance, capacitance and duty cycle can be determined as:

- **Boost Inductance:**

$$L_b = \frac{V_{dc}(V_{ip} - V_{dc})}{f_{sw} \times \Delta I \times \Delta V_{ip}} = 4mH \quad (3.1)$$

- **Boost Capacitance:**

$$C_b = \frac{I_{ip}(V_{ip} - V_{dc})}{f_{sw} \times \Delta V \times \Delta V_{ip}} = 2mH \quad (3.2)$$

- **Duty Cycle:**

$$D_b = 1 - \frac{V_{dc}}{V_{in}} = 0.66 \quad (3.3)$$

3.1.2 Capacitor Cell

The switched-capacitor C_{sn} can be calculated by:

$$C_{SN2} \geq \frac{Q_N}{\Delta V_{in} V_{in}} \geq 3.9mf \quad (3.4)$$

which is dependent on the total capacitor discharging value (Q_N) and the permissible voltage ripple across the applied input voltage (δV_{in}) of the system. The selection criteria mentioned here are for voltage source type inverters that only need filter inductor at the output to provide filtering for the output waveform.

3.2 Switched Capacitor Structure

Capacitor C_1 is charged while connected in parallel with the input source through Sc_{11} . Capacitor C_2 is charged while connected in parallel with the input source through Sc_{12} . C_1 is thus charged to V_{in} and C_2 is also charged to V_{in} . The five levels of voltage are obtained by the combination of Switched capacitor cell and H bridge inverter. Two Levels of voltage (in addition to a zero level) are therefore obtained by the following combinations:-

MODE	OUTPUT VOLTAGE	STATE
1	$+V_{in}$	Source and C_1 in parallel.
2	$+2V_{in}$	C_1 and C_2 in series through Sc_{12} , then parallel with source.
3	$0V$	Any combination of Switched capacitor cell.

Table 3.3: Output voltage states

In mode 1(to obtain $+V_{in}$), the capacitors C_1 and C_2 are connected in parallel by switching on Sc_{11} & Sc_{13} such that it provides $+V_{in}$ to the H-Bridge.In mode 2(to obtain $+2V_{in}$), the capacitors C_1 and

C_2 is in series connected through switch $Sc12$ thus providing $+2V_{in}$ to h-Bridge.

3.3 Modes of Operation

Mode 1: The voltage across capacitors C_1 & C_2 is same as boost output voltage V_{in} . Since they are connected parallel by closing switches $Sc11$ & $Sc13$ the H-Bridge has V_{in} as input. This voltage is carried to the load by switches $S1$ & $S4$. Hence, the total voltage that is produced across the load is V_{in} .

Mode 2: The voltage across capacitors C_1 & C_2 is same as boost output voltage V_{in} . Since they are connected series by closing switch $Sc12$ the H-Bridge has $2V_{in}$ as input. This voltage is carried to the load by switches $S1$ & $S4$. Hence, the total voltage that is produced across the load is $2V_{in}$.

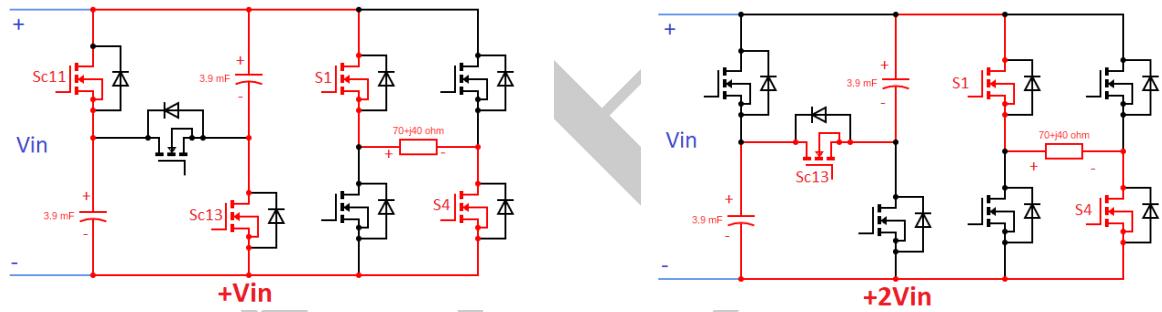


Figure 3.2: Positive Modes of Operation

Mode 3: The voltage across capacitors C_1 & C_2 is same as boost output voltage V_{in} . Since they are connected parallel by closing switches $Sc11$ & $Sc13$ the H-Bridge has V_{in} as input. This voltage is carried to the load by switches $S3$ & $S2$. Hence, the total voltage that is produced across the load is $-V_{in}$.

Mode 4: The voltage across capacitors C_1 & C_2 is same as boost output voltage V_{in} . Since they are connected series by closing switch $Sc12$ the H-Bridge has $2V_{in}$ as input. This voltage is carried to the load by switches $S3$ & $S2$. Hence, the total voltage that is produced across the load is $-2V_{in}$.

Mode 5: In this mode, voltage across the load is zero. This is achieved by either closing switches $S1$ & $S3$ or $S2$ & $S4$.

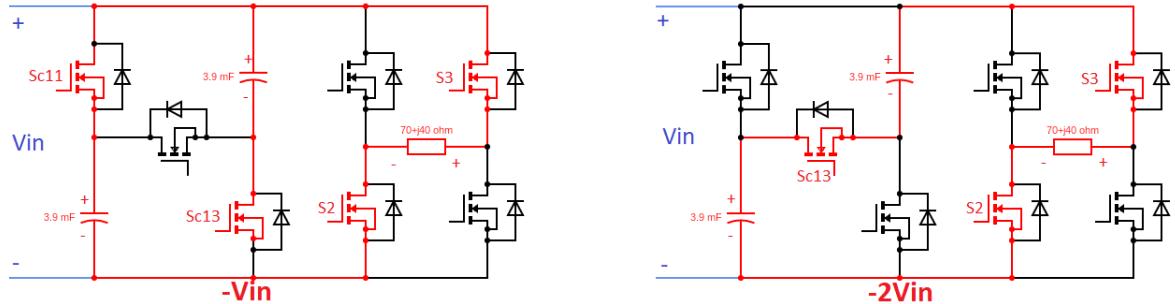


Figure 3.3: Negative Modes of Operation

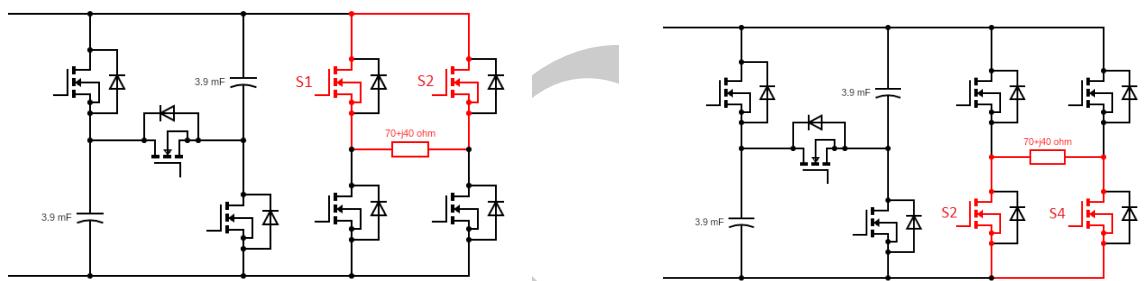


Figure 3.4: 0V Mode of Operation

Therefore there are 5 different voltage levels ($2 * 2 + 1$) available at the output of the inverter. The switching states are controlled by Level-shifted Phase PWM.

3.4 Switching States

MODE	OUTPUT VOLTAGE	STATE
1	V_{in}	Source and C_1 and C_2 in parallel.
2	$2V_{in}$	C_1 and C_2 in series.

Table 3.4: Output voltage of Capacitor cell states

In the positive half cycle S_4 is fully turned on whereas S_3 is fully turned OFF and switches S_1 and S_2 are toggled alternatively. Similarly, in the positive half cycle S_3 is fully turned on whereas S_4 is fully turned OFF and switches S_1 and S_2 are toggled alternatively. To achieve zero voltage output s_1 and s_3 or s_2 and s_4 are turned on simultaneously.

MODE	VOLTAGE STATE	SC11	SC12	SC13	S1	S2	S3	S4
1	0	ON/OFF	ON/OFF	ON/OFF	ON	OFF	ON	OFF
2	0	ON/OFF	ON/OFF	ON/OFF	OFF	ON	OFF	ON
3	$+V_{IN}$	ON	OFF	ON	ON	OFF	OFF	ON
4	$+2 V_{IN}$	OFF	ON	OFF	ON	OFF	OFF	ON
5	$-V_{IN}$	ON	OFF	ON	OFF	ON	ON	OFF
6	$-2 V_{IN}$	OFF	ON	OFF	OFF	ON	ON	OFF

Table 3.5: Switching State of switched capacitor pair

3.5 Level Shifted PWM

This technique can be efficiently applied for Diode Clamped, Cascaded Multilevel, Switched Capacitor and Capacitor Cell Inverters. The main classification of carrier based PWM techniques are Level shifted carrier PWM and Phase disposition PWM. Most of the carrier based PWM techniques have been derived from the classical carrier disposition strategies. The phases of carrier signals are rearranged to produce three main disposition techniques known as PD, POD and APOD. The level shifted method arrange N-1 carrier wave-forms of same amplitude and frequency stacked to fully occupy the linear modulation range of the inverter. The reference or modulating wave is positioned at the centre of the carrier set, and continuously compared with the carriers. Whenever the magnitude of reference wave is greater than a carrier wave, positive going switching pulse is obtained. When the reference goes above all the carriers maximum output is obtained. As the reference falls below each carrier the corresponding levels in the inverter output gets reduced.

Switching scheme used in this inverter is level shifted pulse width modulation. Four level-shifted triangular carrier signals are modulated using a single sine wave. All triangular waves are in phase. The amplitude of the sine wave is 2 units. Each triangular wave is level-shifted by 1 unit corresponding to each output level.

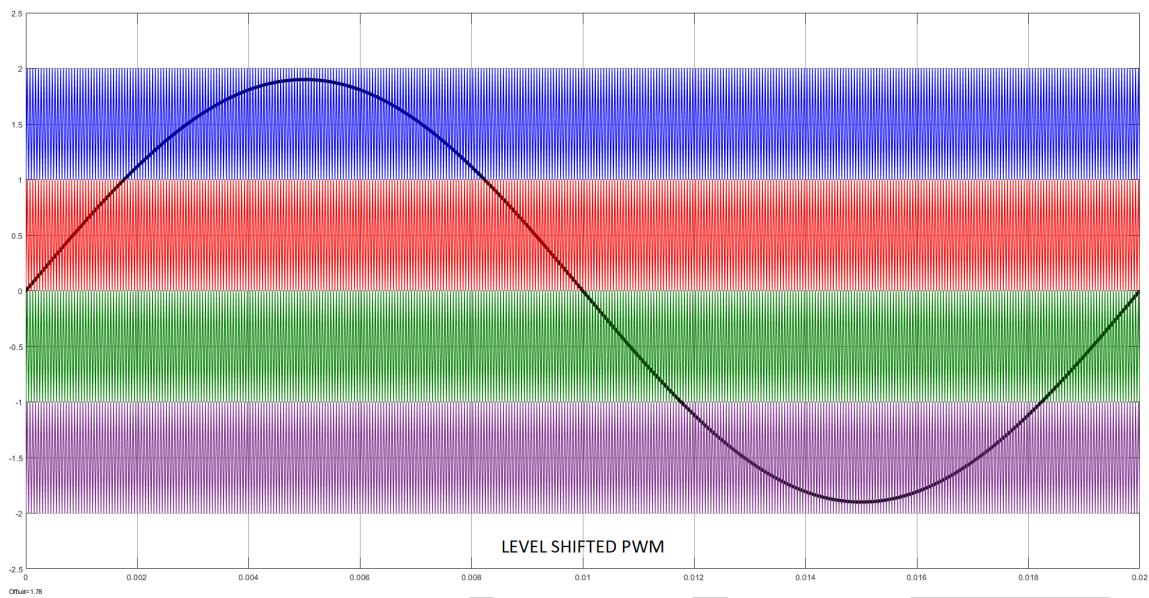


Figure 3.5: Level Shifted Sine PWM Scheme

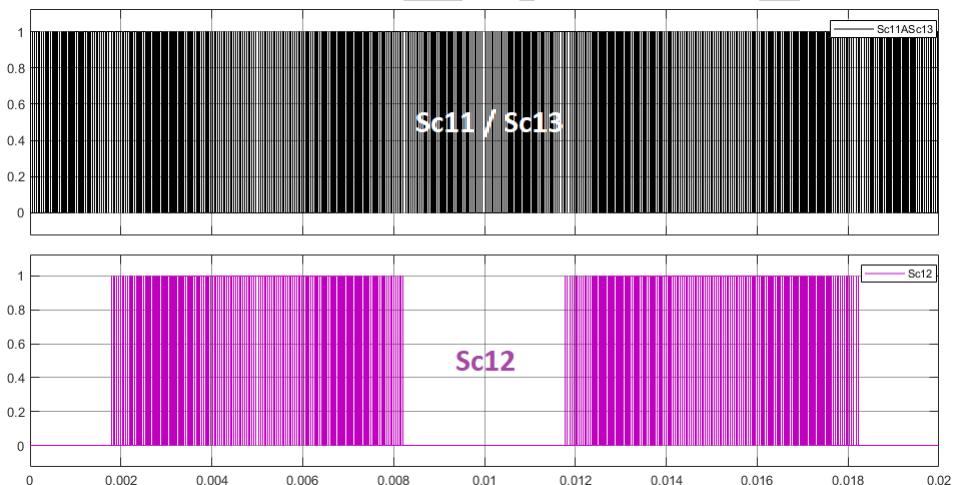


Figure 3.6: Capacitor Cell Switching

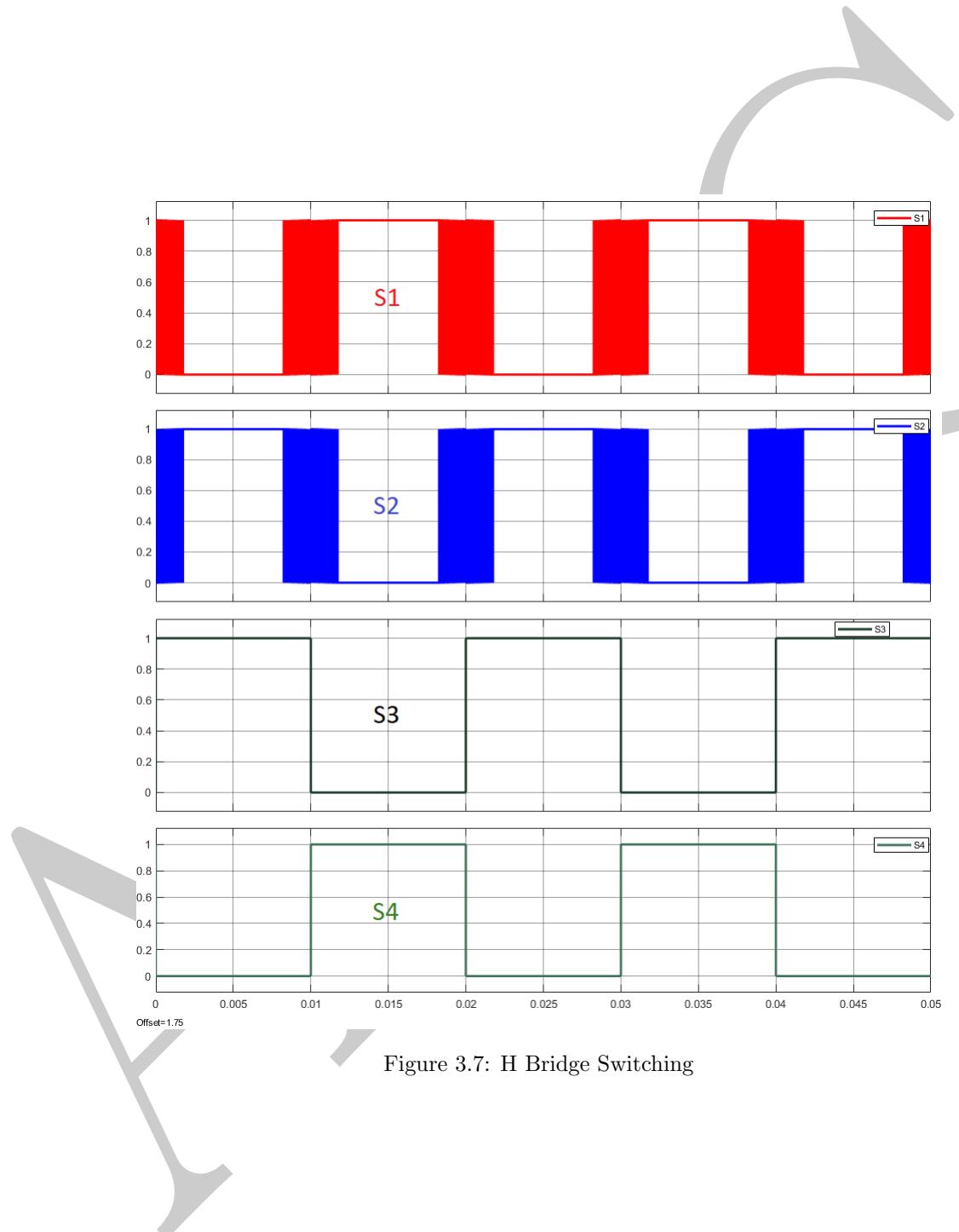


Figure 3.7: H Bridge Switching

Chapter 4

SIMULATION RESULTS

This chapter discusses about the simulation model of the five level inverter based on switched capacitor structure. Further the analysis of the simulink model is also given.

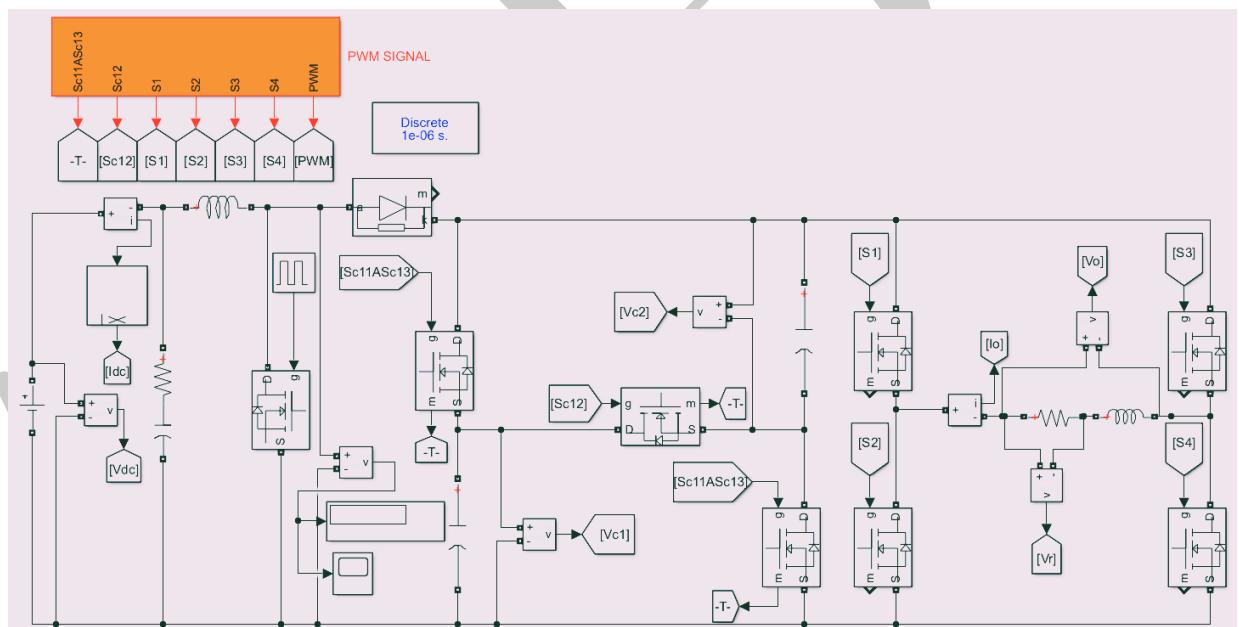


Figure 4.1: Simulink Circuit

The simulation of the FIVE-LEVEL INVERTER was done using the simulink tool in matlab. Operation of the inverter was verified with R and R-L load. Gating pulses are derived using Level Shifted PWM technique. The switching delay and gate delay are neglected. The design consideration are given in the table below.

PARAMETER	VALUE
Input Voltage (V_{dc})	24V
Boost circuit output (V_{out})	72V
Output Voltage (V_{rms})	100V
Power Rating(P_{output})	100W
Carrier frequency	20KHz
Line Frequency(f)	50Hz
DC-Link Capacitor ($C1C2$)	4mF,150V
Load Resistor	70ohm
Load inductance	129 mH
Boost Inductor(L_B)	4mH

Table 4.1: Simulation specification

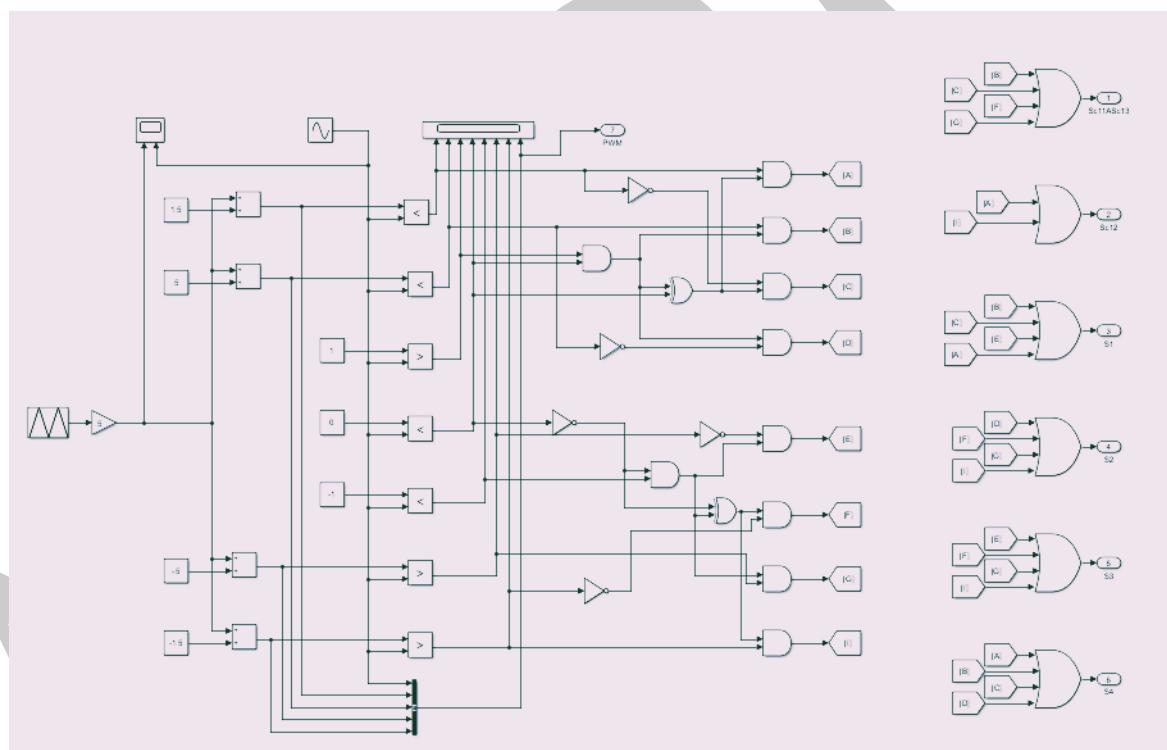


Figure 4.2: Level Shifted Sine PWM Logic Implementation

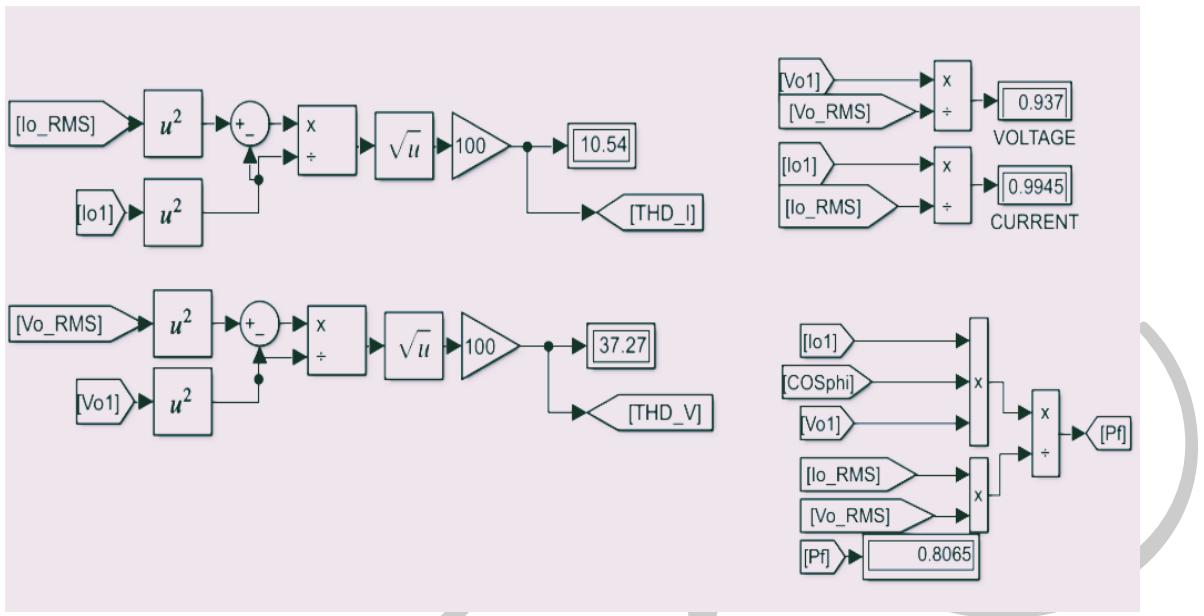


Figure 4.3: Measurement Block

4.1 Result

The output of the simulink simulation is shown in the following figures. Figure 5.16 shows the output voltage, capacitor voltage and current. Figure ?? shows the analysis after measurement of various inverter parameters. The peak voltage output of the inverter is 144V. The RMS value of output voltage is 99.96V. The RMS value of output current is 1.164A. The capacitor voltage is nearly constant with negligible ripple. The model is found to meet the expected design power output of 100Watts.

4.1.1 Total Harmonic Distortion(THD)

The output voltage waveform for a load of resistance 70 ohm and inductance of 129mH is shown in figure 5.16. It's THD of ouput voltage is found to be 33.28% and THD of output current is found to be 3.4%.

4.1.2 Efficiency

Efficiency of the switched capacitor five-level inverter for a load of resistance 70 ohm and inductance of

129mH is found to be 92.43% for a power output of 100W.

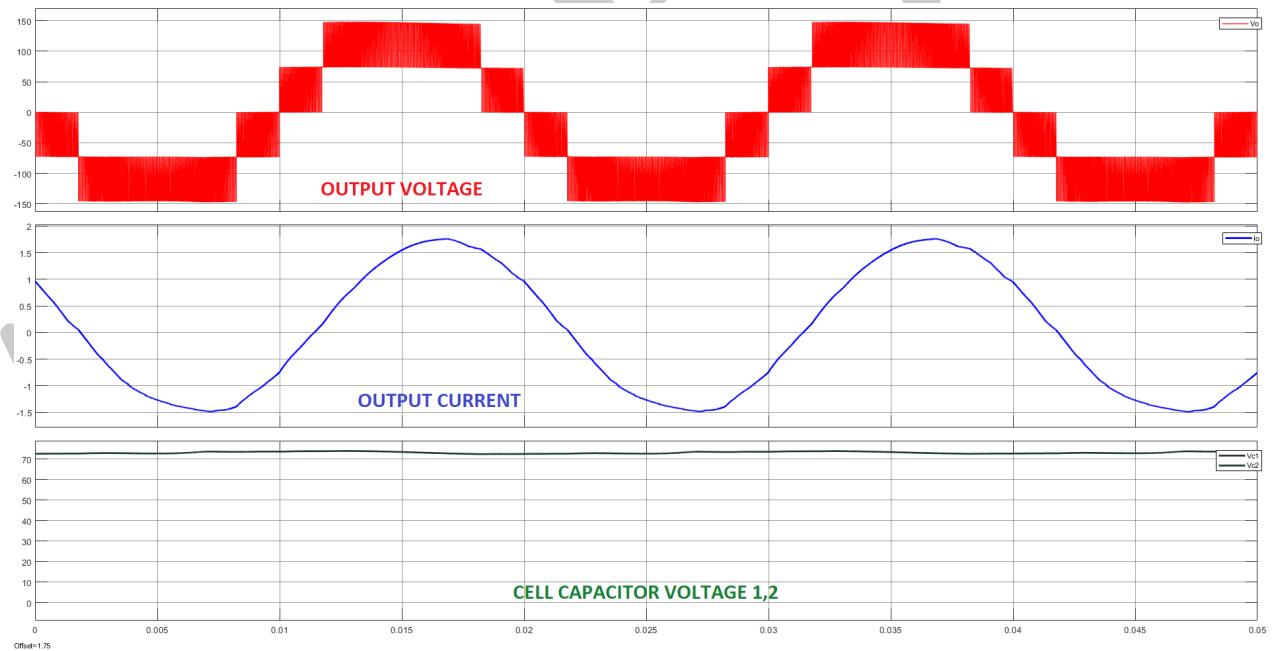
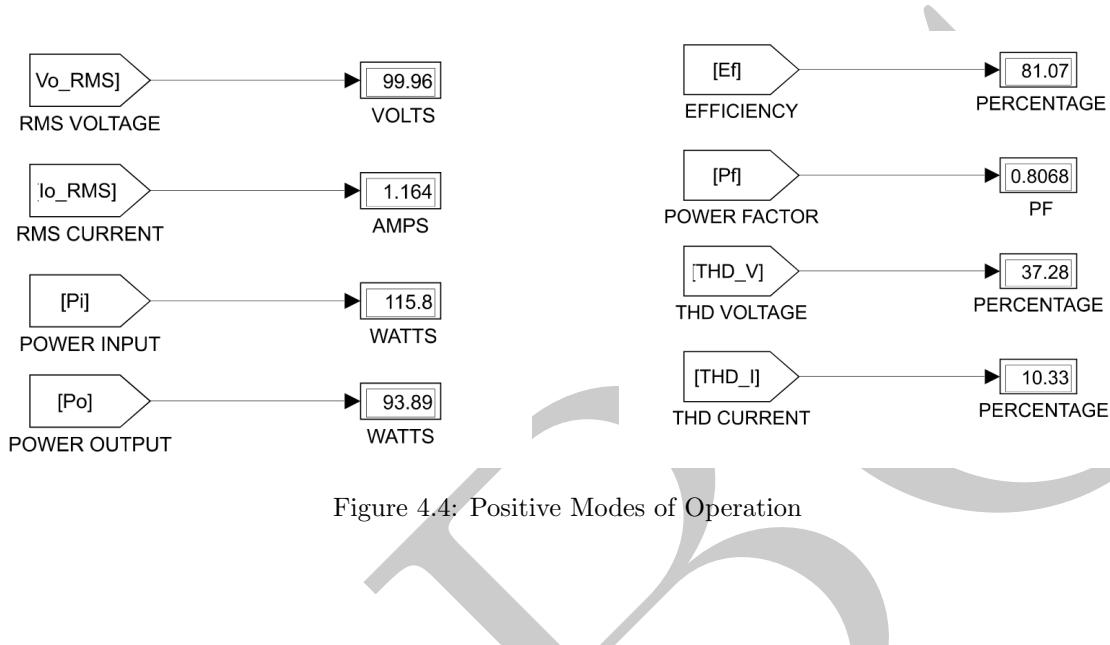


Figure 4.5: Simulink Output

Chapter 5

HARDWARE REQUIREMENTS

5.1 Component Selection

COMPONENTS	RATING	NOS
dsPIC30F2020		1
LM7815T		7
MUR460		10
IRF540		4
TLP250(F)		4
IRFP460C		8
CAPACITOR	220 μ F	14
CAPACITOR	1000 μ F	9
CAPACITOR	0.1 μ F	12
RESISTOR	1K Ohm	18
RESISTOR	270 Ohm	9
RESISTOR	720 Ohm	1
RESISTOR	560 Ohm	9

Table 5.1: Components for the Inverter

5.1.1 dsPIC30F2020

The dsPIC30F2020 microcontroller is a 16-bit digital signal controller with powerful capabilities for PWM (Pulse-Width Modulation) applications. It offers a range of features and specifications that make it well-suited for precise control of PWM signals.

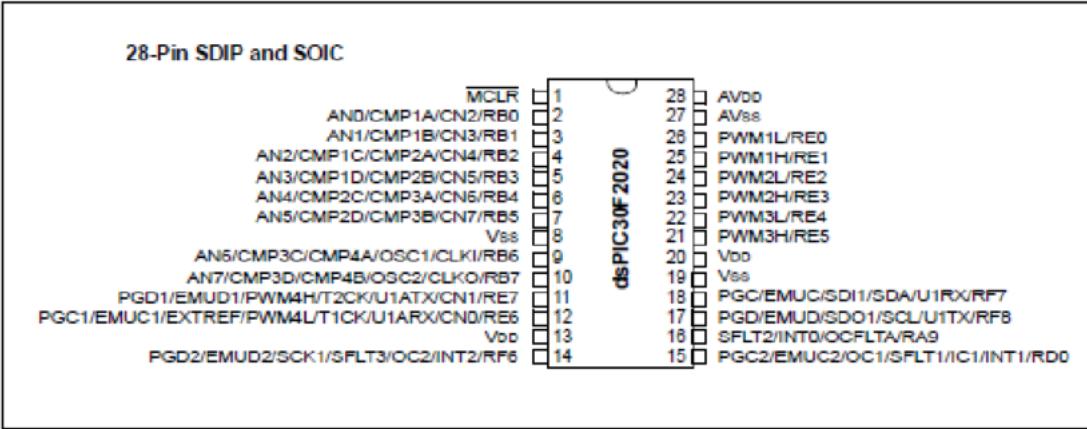


Figure 5.1: Pin Diagram of dsPIC30F2020

Here's a note highlighting its specifications with a focus on PWM applications:

1. **Architecture:** The dsPIC30F2020 is based on a high-performance modified Harvard architecture, which combines the benefits of both Harvard and Von Neumann architectures. This architecture allows for efficient execution of complex algorithms and real-time signal processing required in PWM applications.
2. **PWM Modules:** The dsPIC30F2020 has four independent PWM modules, each capable of generating up to two PWM outputs. These modules provide flexibility in generating multiple PWM signals simultaneously and offer features such as dead-time control, fault protection, and synchronization options.
3. **PWM Resolution:** The PWM modules in the dsPIC30F2020 support a resolution of up to 10 bits. This high resolution allows for precise control of the duty cycle and enables smooth and accurate generation of analog-like signals.
4. **PWM Frequency:** The dsPIC30F2020 supports a wide range of PWM frequencies, allowing for the selection of an appropriate frequency based on the specific application requirements. The PWM frequency can be adjusted to suit the desired switching speed and noise considerations.
5. **Duty Cycle Control:** The dsPIC30F2020 provides precise control over the duty cycle of the PWM signals. The duty cycle determines the ON time of the PWM output signal within each period and can be dynamically adjusted to control the average power or analog-like value delivered to the connected devices.
6. **Output Drive Strength:** The PWM outputs of the dsPIC30F2020 can drive external devices directly. The output drive strength ensures that the PWM signals can effectively control power MOSFETs, motor drivers, or other components without the need for additional buffer circuits.

7. Programming Environment: The dsPIC30F2020 is programmed using Microchip's MPLAB development environment, which provides a comprehensive set of tools for PWM configuration, code development, debugging, and simulation. This facilitates efficient development and testing of PWM applications.

Overall, the dsPIC30F2020 microcontroller offers a robust set of specifications specifically designed for PWM applications. Its multiple PWM modules, high resolution, flexible frequency range, precise duty cycle control, and suitable output drive strength make it an excellent choice for applications such as motor control, power electronics, lighting systems, and other applications that require precise control of PWM signals.

The implementation of this circuit requires a switching signal of 20kHz and 4 independent PWM modules as per design. Based on this dsPIC30F2020 can provide these required features with 4 independent PWM modules.

5.2 Inductor and Transformer Design

5.2.1 Inductor

Inductor design involve the process of determining the necessary parameters and specifications for the construction of these electromagnetic components.

- Determine the required inductance value: The inductance value is determined based on the desired performance of the circuit or system.
- Select the core material: The core material depends on factors such as frequency, current levels, and size constraints. Common core materials include ferrite, powdered iron, and laminated cores.
- Calculate the number of turns: The number of turns of wire around the core is calculated using the desired inductance value and the core's magnetic properties.
- Determine wire gauge: The wire gauge is chosen based on the desired current-carrying capacity and the physical constraints of the design.
- Consider parasitic effects: Parasitic effects such as resistance, capacitance, and core losses should be taken into account during the design process.

PARAMETER	BOOST INDUCTOR
Core	EE65/32/26
Conductor thickness	SWG16
number of turns	123

Table 5.2: Inductor Parameters

5.2.2 Transformer

Transformer design involve the process of determining the necessary parameters and specifications for the construction of these electromagnetic components.

- Determine the required turns ratio: The turns ratio is determined by the desired voltage conversion ratio between the primary and secondary windings.
- Calculate the core size and material: The core size and material are chosen based on factors like power handling capability, frequency range, and desired efficiency. Common core materials include laminated iron, ferrite, and powdered iron.
- Calculate the number of turns for primary and secondary windings: The number of turns for each winding is determined using the turns ratio and the desired voltage transformation.
- Determine wire gauge: The wire gauge is selected based on current-carrying capacity and the physical constraints of the design.
- Consider parasitic effects: Similar to inductors, parasitic effects such as resistance, capacitance, and core losses should be considered during transformer design.

PARAMETER	POWER SUPPLY TRANSFORMER
Core	EE42/21/15
Primary Conductor thickness	24SWG
Number of turns primary	33 turns
Secondary Conductor thickness	26SWG
number of turns secondary	28

Table 5.3: Transformer Parameters

5.3 PCB Realisation

A PCB (Printed Circuit Board) is a crucial component in electronic devices. It provides a platform for connecting and supporting electronic components, facilitating the flow of electrical signals and power. The primary purpose of designing a PCB is to create a reliable, compact, and efficient circuit layout. The need for PCB design arises from the following reasons:

- Component Integration: PCBs allow for the integration of various electronic components into a compact form, reducing the size of the overall device.
- Signal Integrity: PCBs enable proper routing and impedance control, ensuring reliable transmission of signals and minimizing noise interference.
- Electrical Connectivity: PCBs provide a means to establish electrical connections between different components, ensuring accurate and efficient flow of current and data.
- Mechanical Support: PCBs offer physical support to electronic components, ensuring their stability and protecting them from external factors such as vibrations and shocks.
- Manufacturing Efficiency: PCBs streamline the manufacturing process by allowing for automated assembly and soldering, reducing production costs and increasing consistency.

When designing a PCB, several criteria should be considered:

- Component Placement: Proper placement of components on the PCB ensures optimal signal flow, efficient routing, and effective heat dissipation.
- Signal Integrity: To maintain signal integrity, careful consideration should be given to trace routing, minimizing signal crosstalk, and adhering to impedance requirements.
- Power Distribution: The PCB design should include appropriate power and ground plane layers to ensure stable power distribution and minimize voltage drops.
- Thermal Management: Adequate consideration should be given to thermal dissipation, using techniques such as heat sinks, thermal vias, and proper component placement to prevent overheating.
- Design for Manufacturability (DFM): PCB designs should adhere to DFM guidelines to ensure ease of manufacturing, efficient assembly, and cost-effectiveness.

- Design for Testing (DFT): Incorporating test points and access for test probes simplifies the testing and debugging process during manufacturing and maintenance.
- EMI/EMC Considerations: Designing for electromagnetic compatibility helps minimize electromagnetic interference (EMI) and ensures compliance with regulatory standards.
- Size and Form Factor: The PCB design should consider the available space constraints and the intended application to achieve the desired compactness and compatibility.

The project PCB consists of three individual circuits: the dsPIC circuit, the gate power supply circuit, and the main circuit board, which serves as a 5-level inverter. Each circuit is designed with specific considerations, following the criteria mentioned earlier. The dsPIC circuit is responsible for generating signals that control the 5-level inverter. It is designed with a focus on signal integrity, proper component placement, and thermal management. Signal routing and impedance control are carefully implemented to ensure accurate and reliable signal transmission. The component placement is optimized to facilitate efficient signal flow between the dsPIC circuit and the main circuit board of the 5-level inverter. Thermal management techniques are also incorporated to dissipate heat effectively and maintain the stability of the dsPIC component.

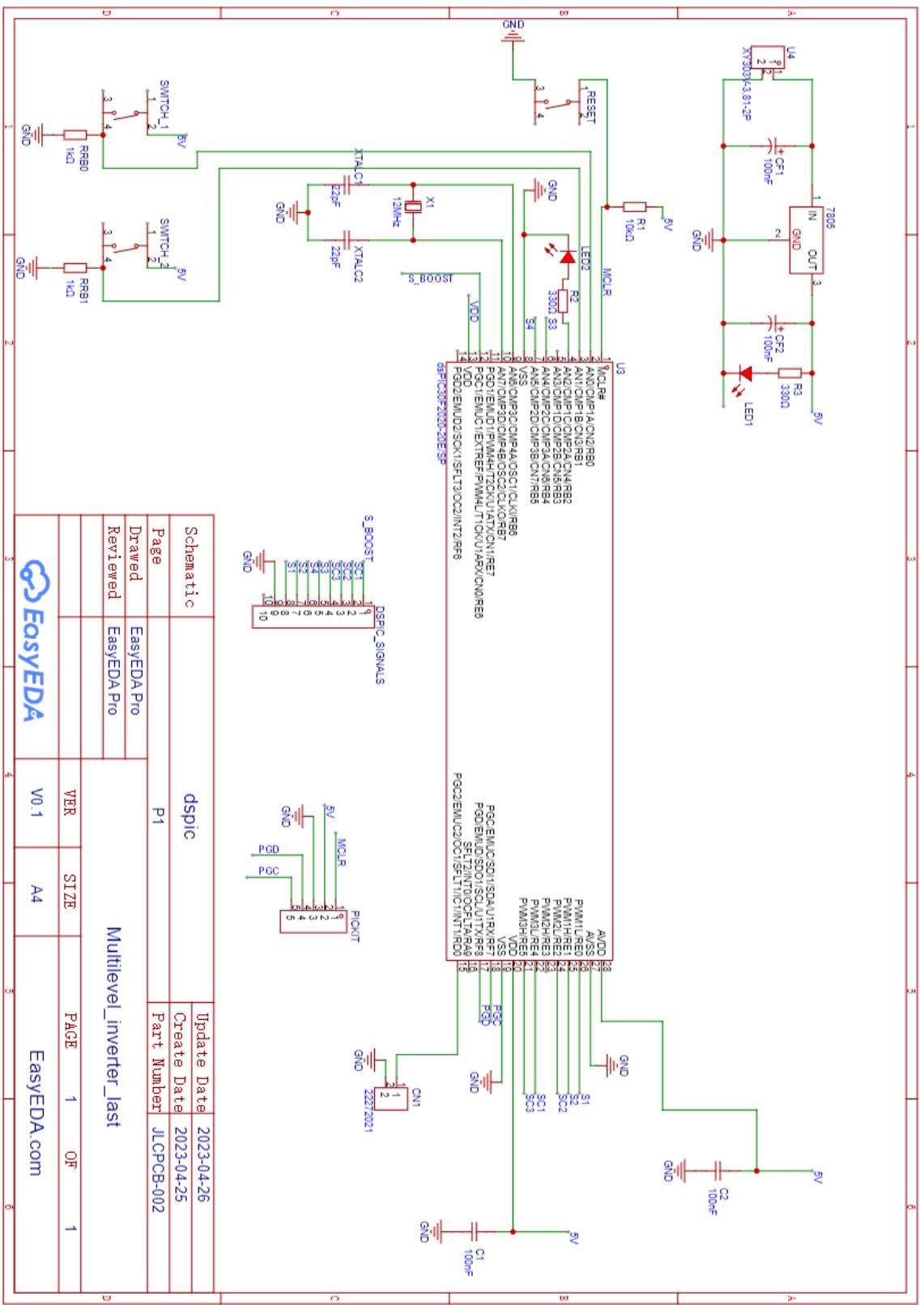


Figure 5.2: dsPIC circuit schematic diagram

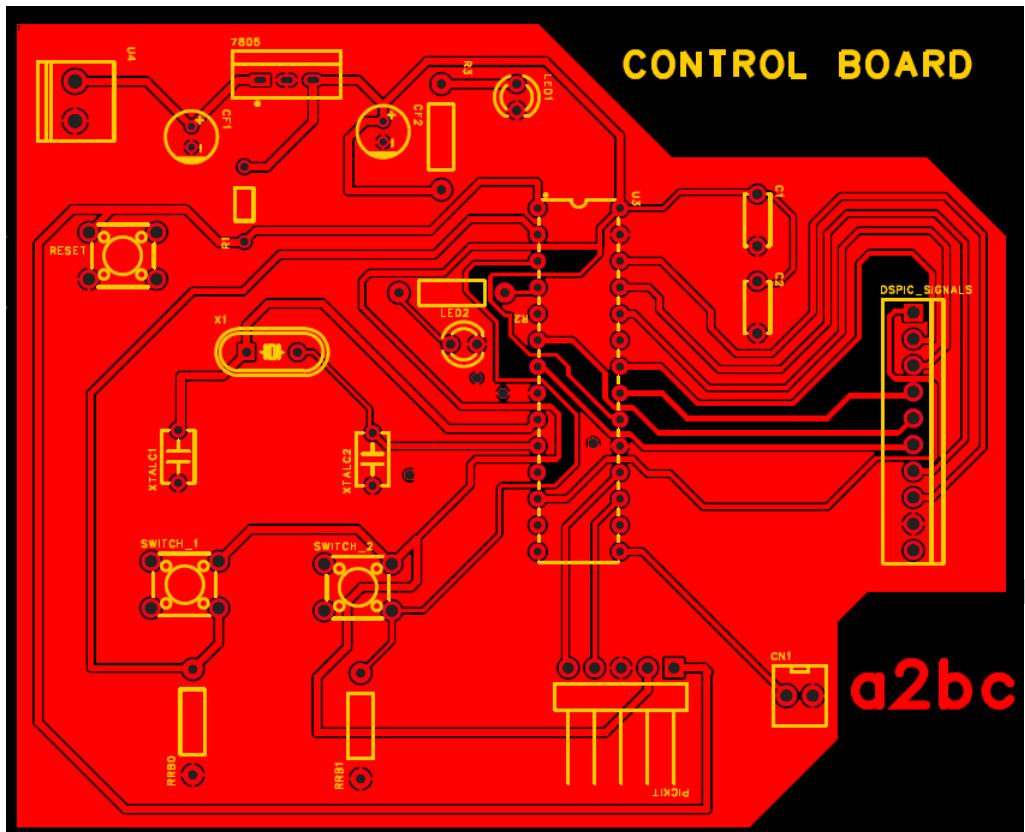


Figure 5.3: dsPIC pcb layout

The gate power supply circuit is designed to provide a stable power source to the 5-level inverter on the main circuit board. It ensures proper power distribution throughout the PCB, minimizing voltage drops and ensuring consistent power delivery. Adequate power and ground planes are included to support the high-power requirements of the inverter. Thermal management considerations are also taken into account to optimize power supply operation and maintain the overall reliability of the gate power supply circuit.

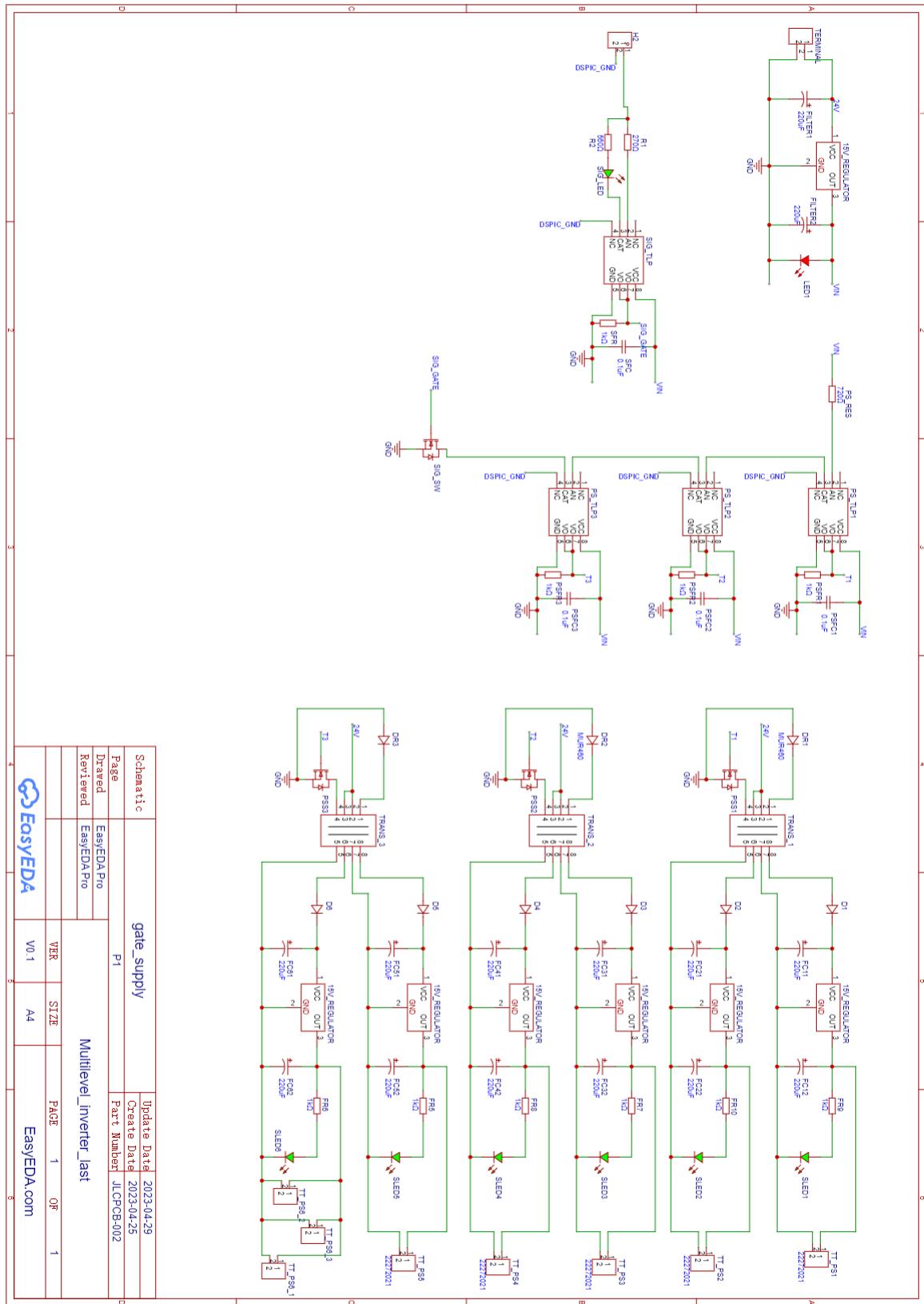


Figure 5.4: Gate power supply circuit schematic diagram

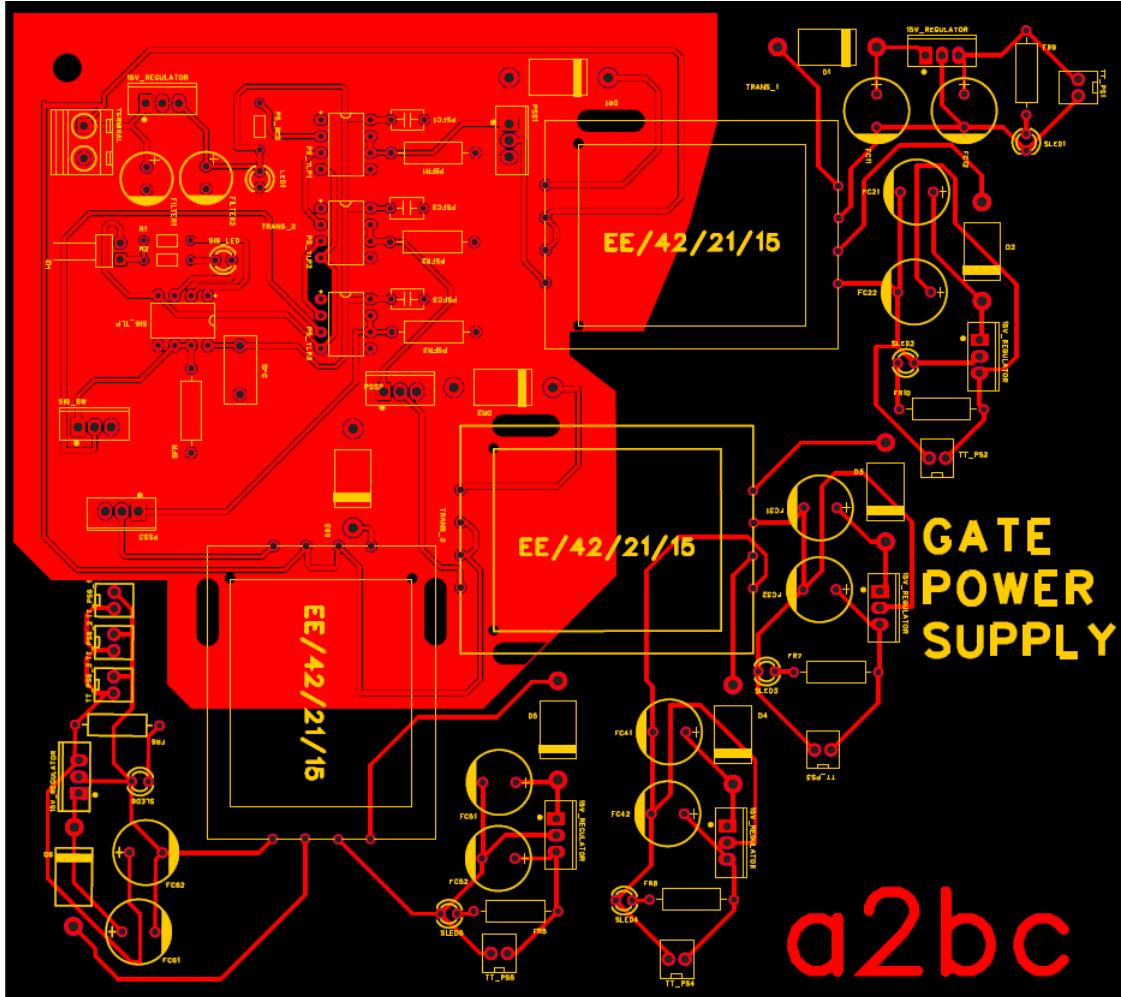


Figure 5.5: Gate power supply pcb layout

The main circuit board serves as the central hub, connecting the individual circuits and functioning as the 5-level inverter. It takes power supply from the gate power circuit and receives control signals from the dsPIC circuit. The design of the main circuit board prioritizes component integration, signal integrity, and mechanical support. Component placement is optimized to facilitate efficient signal flow and power distribution within the 5-level inverter. The layout adheres to design for manufacturability (DFM) guidelines, enabling ease of assembly and cost-effectiveness during production. Proper thermal management techniques are employed to prevent overheating and maintain the overall reliability of the main circuit board.

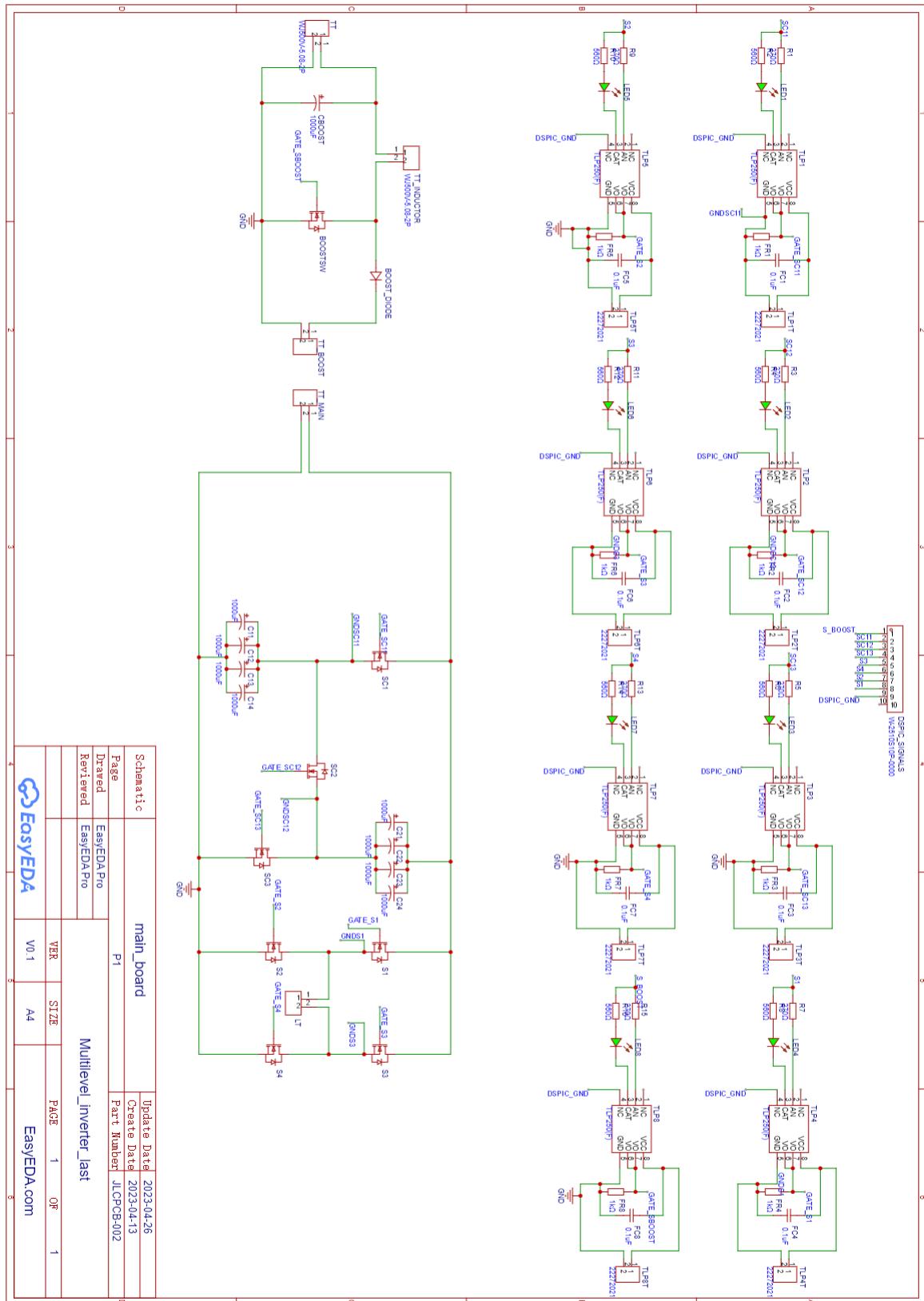


Figure 5.6: Inverter circuit schematic diagram

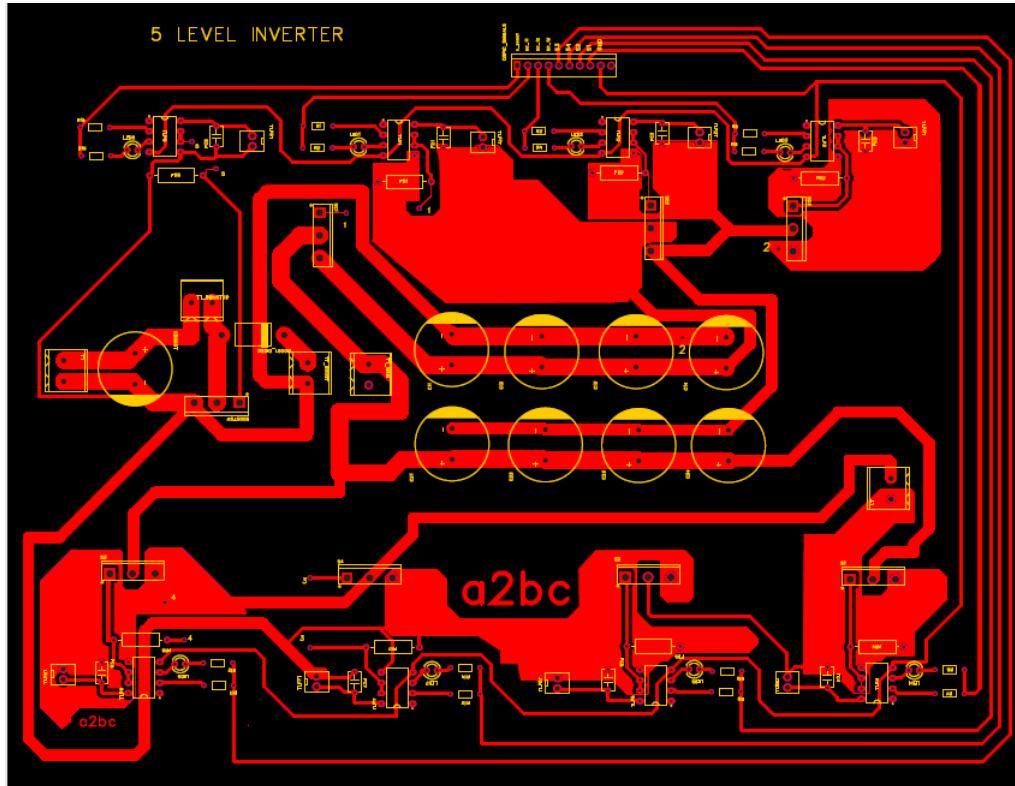


Figure 5.7: Inverter circuit pcb layout

By dividing the project into these individual circuits and designing them with the aforementioned criteria in mind, the PCB layout achieves an efficient, reliable, and compact solution. The integration of the dsPIC circuit, gate power supply circuit, and the main circuit board as a 5-level inverter ensures the proper functioning of the power supply and signal generation, resulting in the desired performance of the electronic device.

5.4 Hardware Results

5.4.1 Haedware Setup

The three circuit boards, including the dsPIC circuit, the gate power supply circuit, and the 5 level inverter circuit board (capacitor bank, H-bridge, and boost converter), are interconnected and operated using a voltage/current supply.

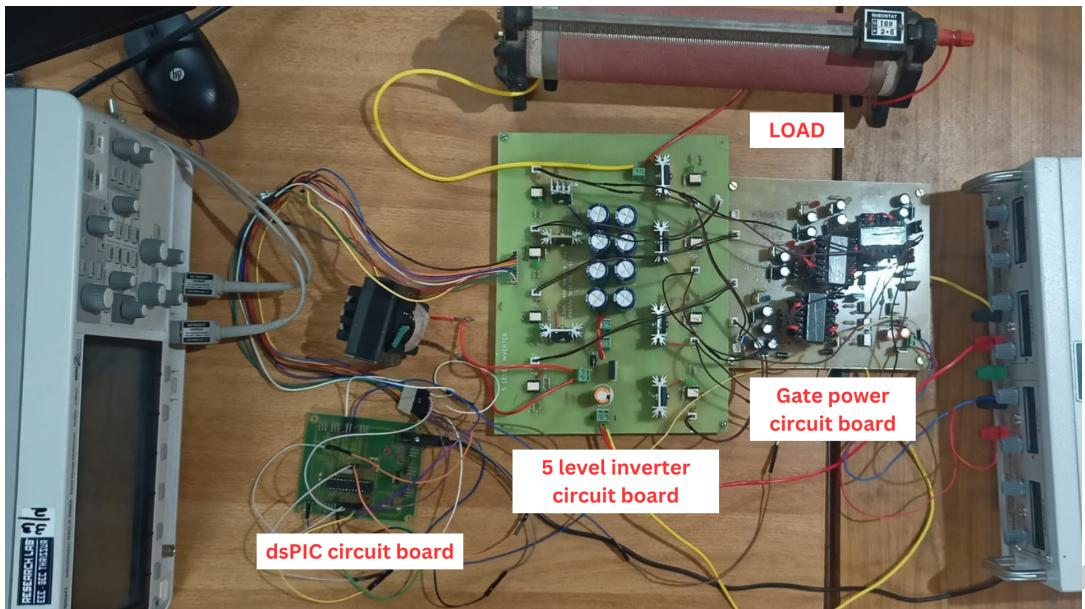


Figure 5.8: Hardware setup of 5 level inverter

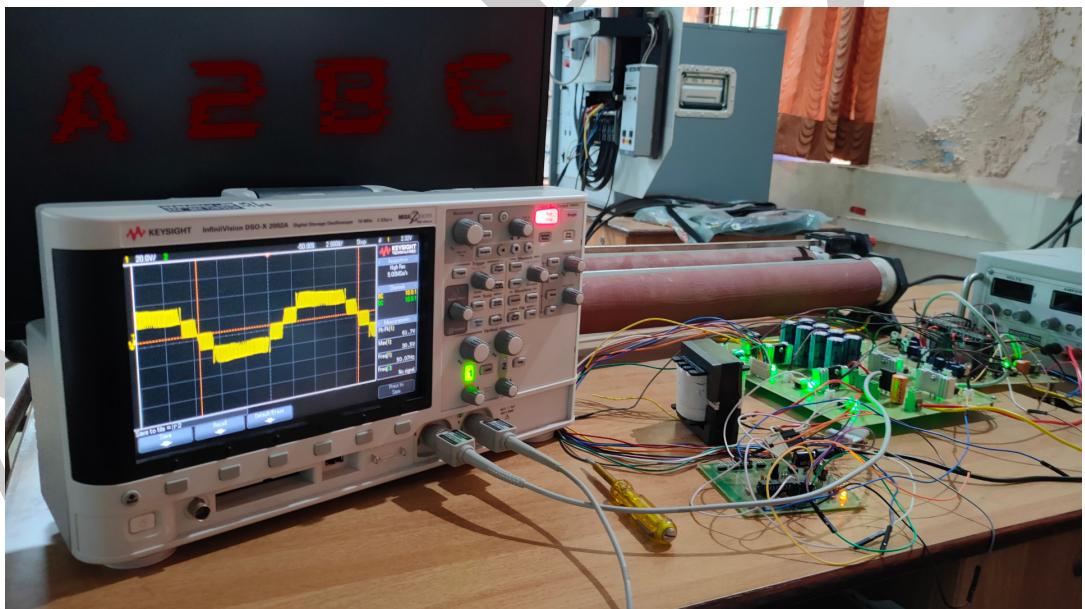


Figure 5.9: Hardware setup of 5 level inverter

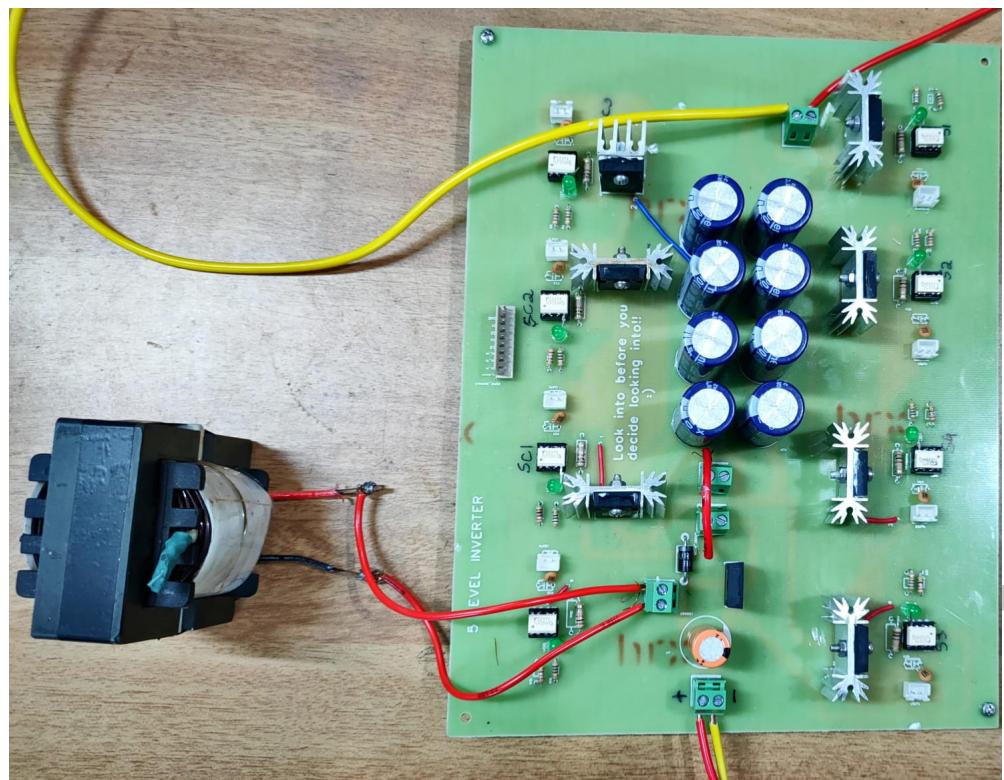


Figure 5.10: Inverter circuit board

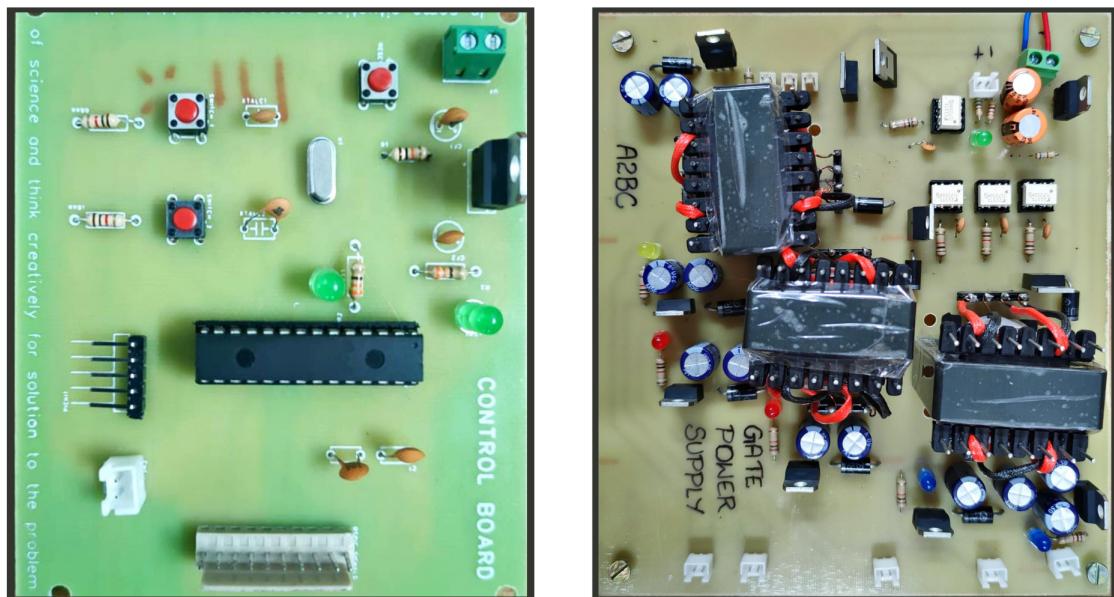


Figure 5.11: dsPIC Circuit and Gate Power Board

5.4.2 Switching Signals

The signals generated by the dsPIC circuit can be observed and analyzed using a Digital Storage Oscilloscope (DSO). The signals from the dsPIC circuit are utilized to control the operation of the switches in the capacitor bank, H-bridge, and boost converter. These switches play a crucial role in the operation of these 5 level inverter circuit circuits.

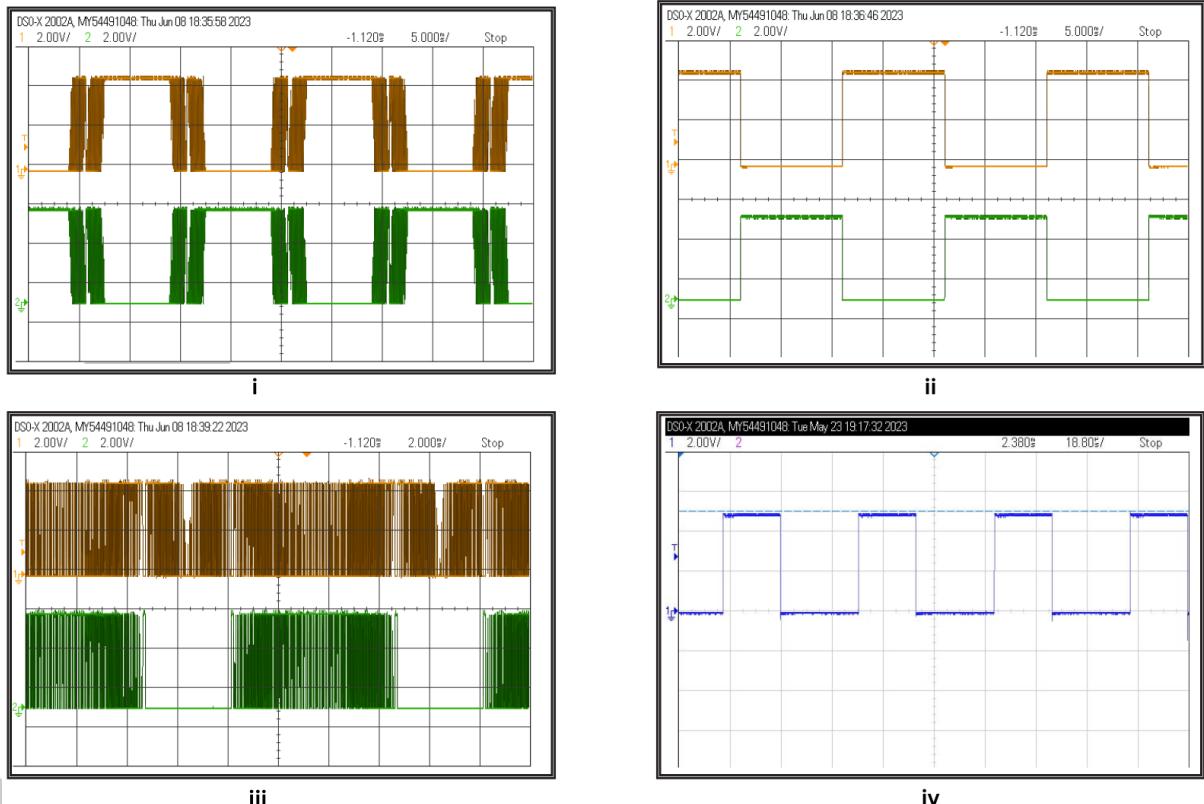


Figure 5.12: Switching Signals for Capacitor Bank, H Bridge and Boost switches
i. Brown shows the switching signal for switch S1 and green the signal for S2 in H-bridge
ii. Brown shows the switching signal for switch SC1, SC3 and green the signal for SC2 in Capacitor bank
iii. Brown shows the switching signal for switch S3 and green the signal for S4 in H-bridge
iv. the switching signal for boost circuit

5.4.3 Output Waveworms

The output current and voltage from the 5-level inverter, as well as the output from the gate power circuit, are observed and analyzed using a Digital Storage Oscilloscope (DSO). The DSO is connected to the respective output terminals of the inverter and gate power circuit using appropriate probes or cables.

GATE POWER

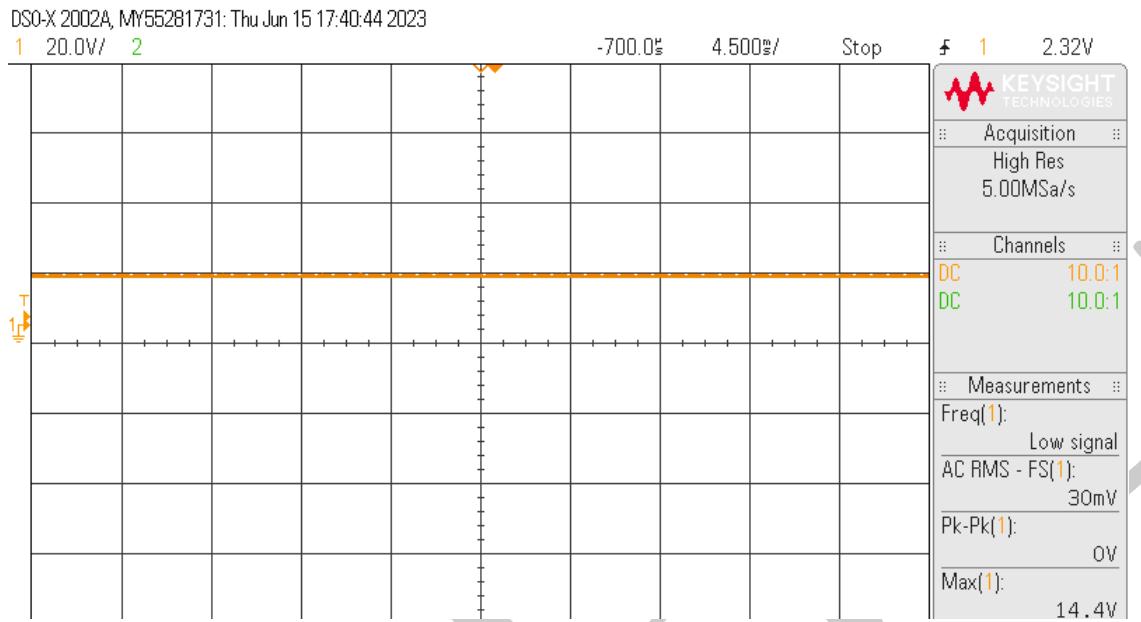


Figure 5.13: Gate Power Output Voltage Waveform

R LOAD

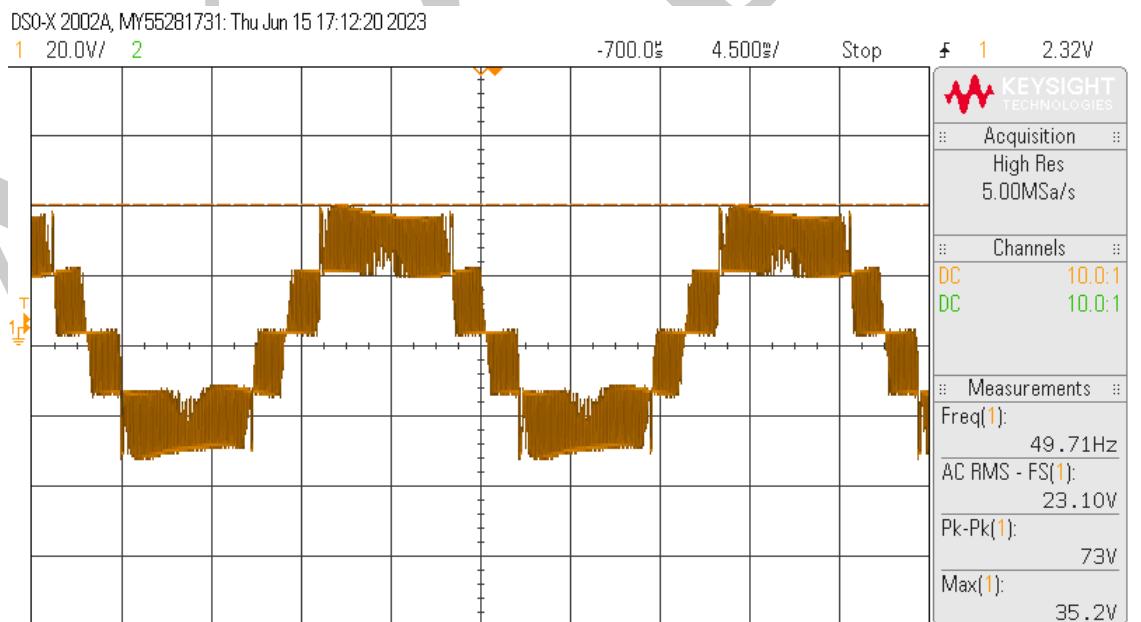


Figure 5.14: Inverter Output Voltage Waveform with R Load

RL LOAD

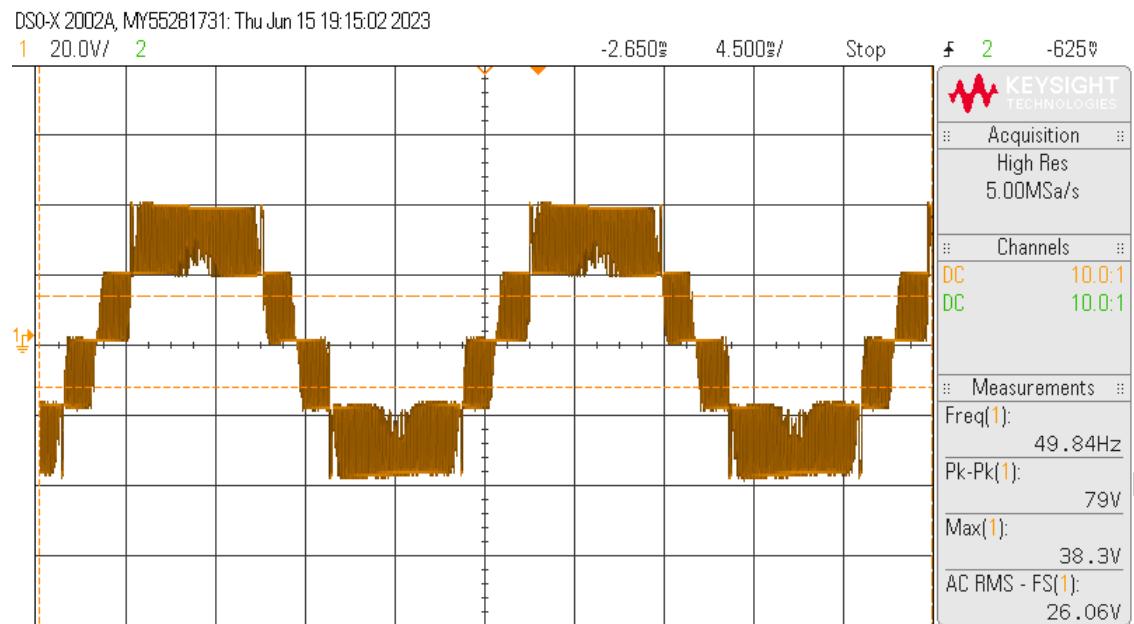


Figure 5.15: Inverter Output Voltage Waveform with RL Load

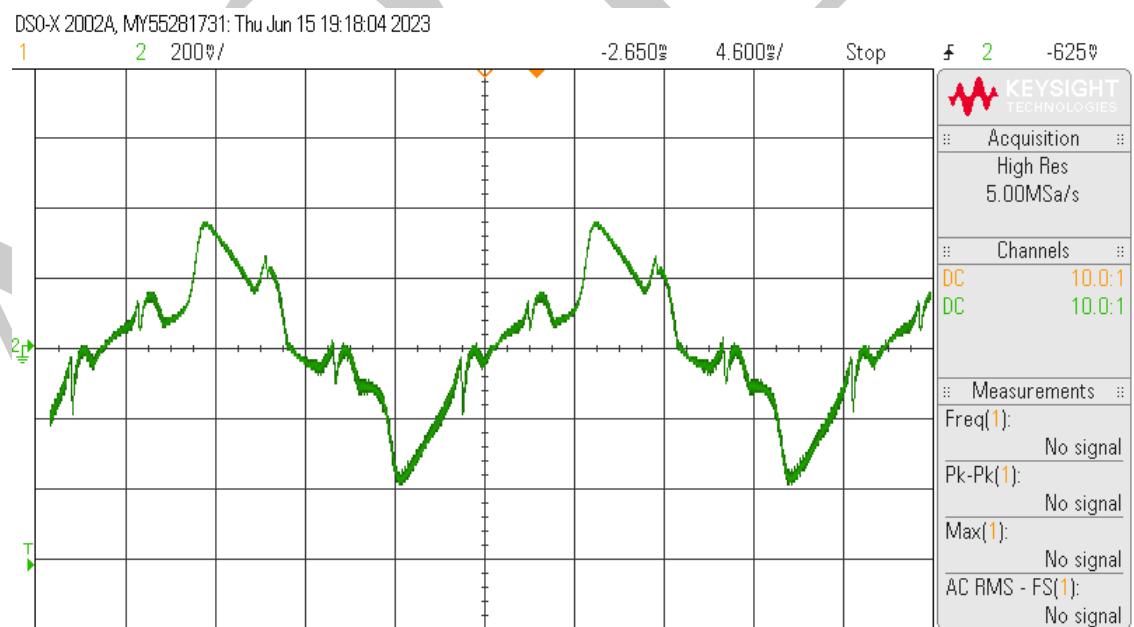
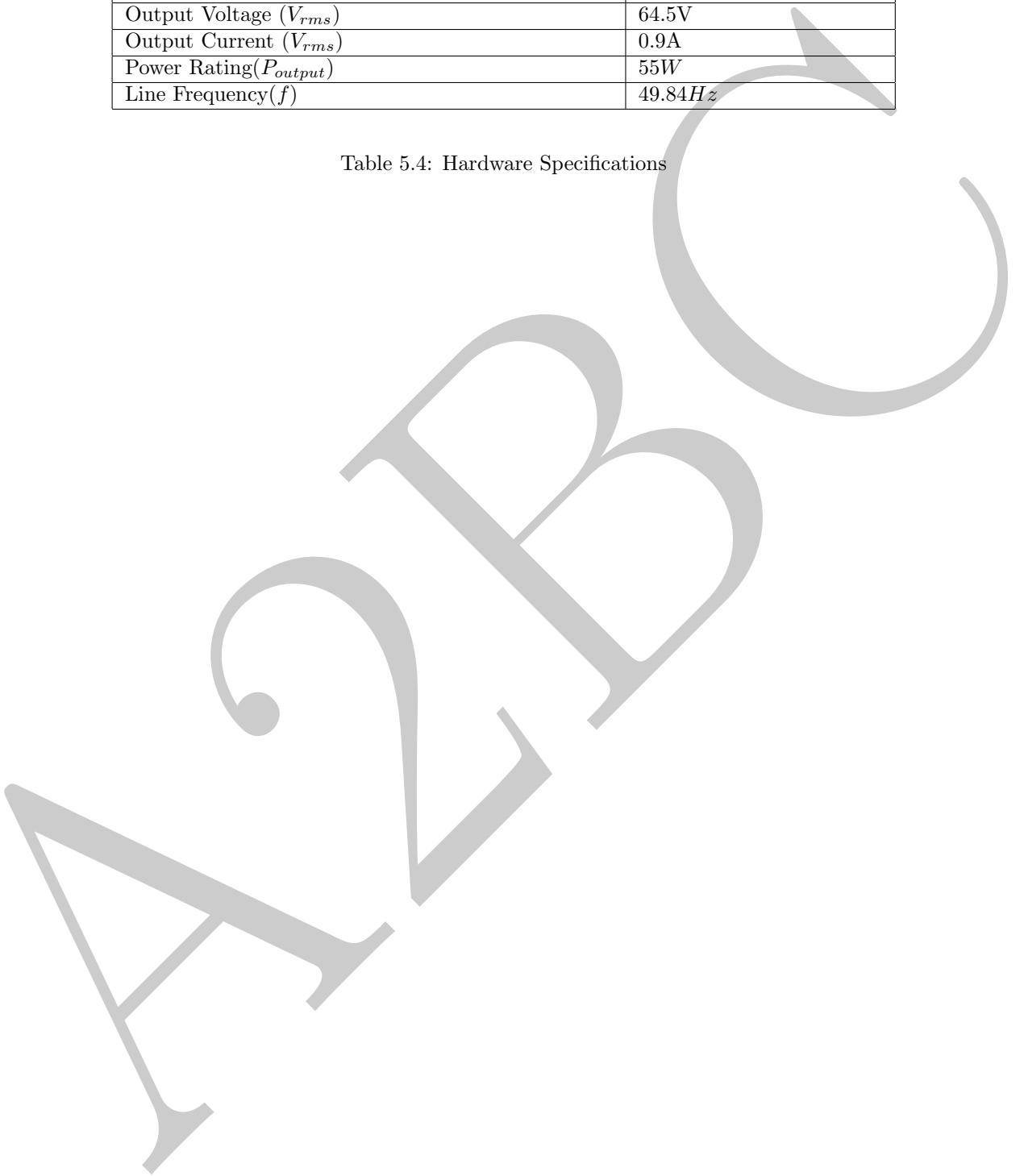


Figure 5.16: Inverter Output Current Waveform with RL Load

HARDWARE PARAMETER	VALUE
Input Voltage (V_{dc})	24V
Input Current (V_{dc})	2.6A
Output Voltage (V_{rms})	64.5V
Output Current (V_{rms})	0.9A
Power Rating(P_{output})	55W
Line Frequency(f)	49.84Hz

Table 5.4: Hardware Specifications

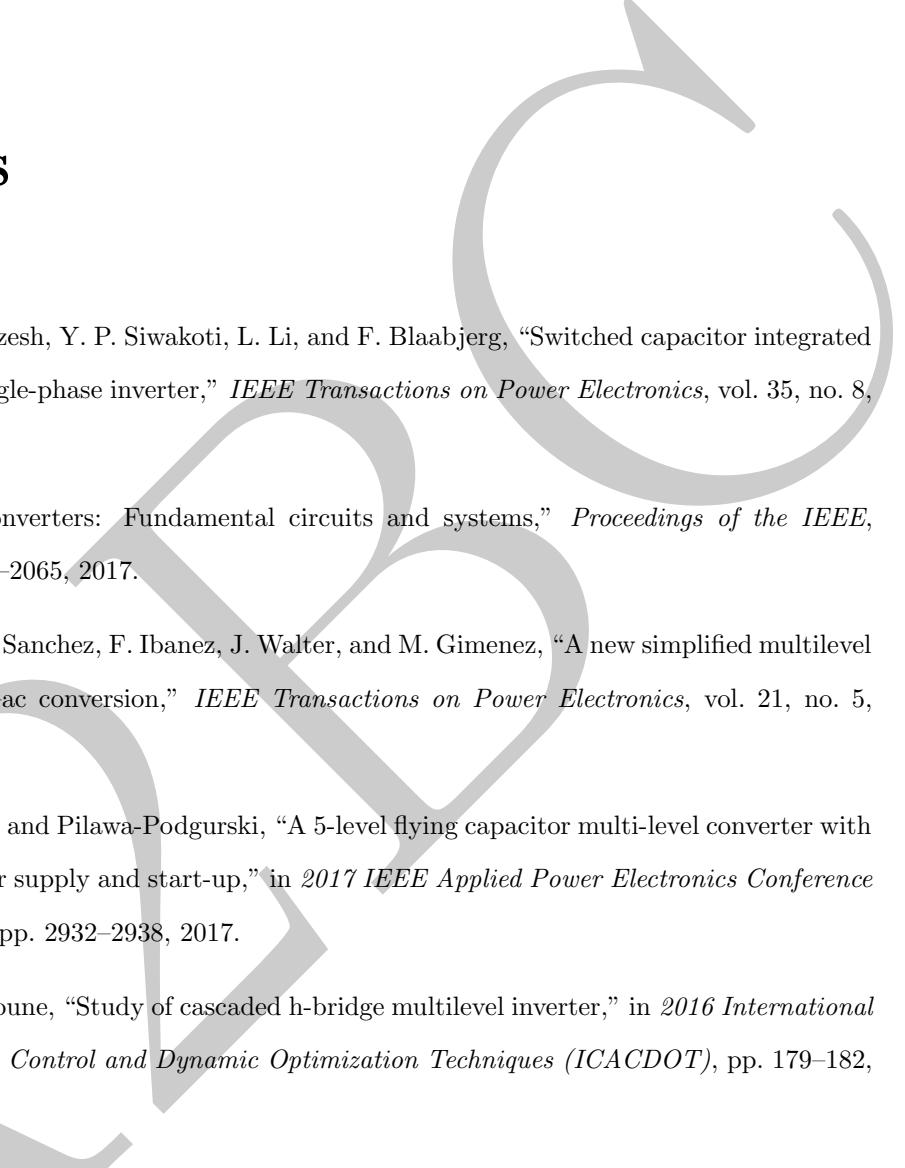


Chapter 6

CONCLUSION

In this study, literature survey of Multilevel Inverter has been done. Comparative study of different existing topologies were done to chose most suitable topology that satisfies required objectives. Proposed Multilevel Inverter uses boost circuit switched capacitor cell and H bridge to meet required output. Circuit was designed for output power of 100W in MATLAB. Output RMS Voltage and RMS Current were found to be 99.96V and 1.164A respectively. Level shifted PWM method was used to produce control signals with switching frequency of 20 kHz. Also circuit was simulated in simulink to obtain results. Total Harmonic Distortion in load voltage and current were found to be 33.28% and 3.4%. Overall Efficiency of proposed multilevel inverter was found to be 92.43%. The circuit was also realised in hardware we obtained the above mentioned results.

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