REVISION QUESTIONS

1. (i) What is a **multiplexer**?
   (ii) Draw a well labeled diagram of a 4 to 1 multiplexer.

2. (a) List the main differences between Serial Networks and Combinatorial Networks
   (b) What is a flip-flop?

3 (a) Give the main differences between a J-K flip flop and an R-S flip-flop.
   (b) Given the following Clock (**C**) and Data (**D**) inputs, find the corresponding Q outputs assuming that Q begins in a state of 0.

C	0	1	0	1	1	1	0	1	1
D	1	1	0	1	1	0	1	1	0

4. (a) (i) What are multivibrators?
   (ii) Explain the different multivibrators found in sequential circuits.
   (b) Draw a symbol, truth (defining) table and a logic diagram for the T flip- flop.
   (c) Assume that the following sequence of clock inputs occurs for the T flip-flop and draw a corresponding timing diagram to show the corresponding Q outputs.

C	0	1	1	0	0	0	1	1	1	0

   Assume that Q starts in state of 1.
   (d) Define the following
   (i) Asynchronous Transfer. (ii) Serial Transfer
   (iii) Propagation time

5. (i) Draw a will labeled diagram of an R-S flip-flop and give the corresponding defining table.
   (ii) Sketch the timing diagram for all inputs and outputs of an R-S flip-flop given that initially R = S = C = 0 and the following sequence of events occurs:
   R = 1; C = 1; R = 0; S = 1; C = 0;S = 0; C = 1; R = 1; R = 0; S = 1; S = 0; C = 0

6. With help of a diagram explain how the binary adder works.

7. (a) (i) What is a register?
(ii) Draw a simple diagram to represent a four bit register using D flip-flops.

(b) An 8 bit register is loaded as shown below. Determine its contents when given a

0	1	1	0	1	1	1	0

(i) Left shift
(ii) A left rotation

8. (a) Draw a symbol and logic diagram for the JK flip-flop.

(b) Assume that the following are the C and D inputs of a D flip-flop, give the corresponding Q outputs.

D	0	1	1	1	1	0	0	1
C	1	0	1	0	0	0	0	1

(c) Draw a timing diagram that shows the D C inputs and the corresponding Q and Q outputs of a D flip-flop assuming that initially D=C=0 and the following sequence of events occurs.
C=1, D=1, D=0, D=1, C=0, D=0, D=1, C=1, D=0
D=1, C=0, D=0, C=1, D=1, C=0, D=0, D=1

(d) Give the corresponding Q output assuming that the above sequence occurs for the
(i) Positive edge triggered flip-flop
(ii) Negative edge triggered flip-flops.

(e) Define the following terms when used in sequential data communication
(i) Handshaking
(ii) Switching time

9 (a) (i) Draw a Logic Diagram and Truth table of a J-K flip-flop
(iii) Assume the following D and Q inputs for the D flip-flop and derive the corresponding Q outputs

D	0	1	0	1	1	0	1	0	1
C	0	1	1	0	0	1	1	0	1

(iv) Assume a positively edged D flip-flop and show the corresponding Q outputs on a timing diagram

10. (a) (i) Draw a Symbol, Defining Table and a Logic Diagram of a T Flip-Flop

(ii) Assume the following are the T successive inputs to a T flip-flop and give the corresponding Q outputs. Assume that initially the Q output is in a state of 0.

0 0 1 1 0 1 0 0 1 1 1 0 1 0 0 1 1

(b) Use a diagram to explain how a Combinatorial Adder differs from a Serial Adder

(c) Explain briefly using an example the difference between ROMs and PLA's.

(d) Explain briefly how an Adder can be modified to produce a Subtractor

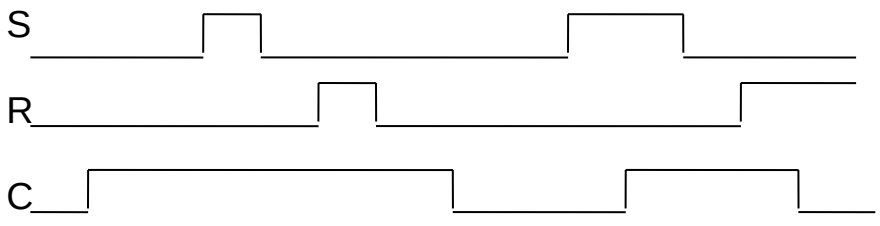
11. (a) Define the following

(i) An Edge Triggered flip-flop
(ii) A Leading Edge
(iii) A Trailing Edge

(b) Draw a symbol, a Truth Table and a Logical Diagram of the R-S Flip- Flop

(c) Given the following S, R, and C transitions of the R-S flip flop, draw the corresponding Q outputs assuming:

(i) A Latch (An ordinary flip-flop)
(ii) A positively edged flip-flop
(iii) A negatively edged flip-flop



(d) (i) Why are Binary Counters constructed from T or J-K flip-flops?

(ii) How can a J-K flip-flop be modified to produce a T flip-flop?

12. (a) Give the main differences between a J-K flip flop and an R-S flip-flop.

(b) Given the following Clock (**C**) and Data (**D**) inputs, find the corresponding Q outputs assuming that Q begins in a state of 0.

C	0	1	0	1	1	1	0	1	1
D	1	1	0	1	1	0	1	1	0.

13. (a) (i) What are multivibrators

(ii) Explain the different multivibrators found in sequential circuits.

(b) Draw a symbol, truth (defining) table and a logic diagram for the T flip-flop.

(b) Assume that the following sequence of clock inputs occurs for the T flip-flop and draw a corresponding timing diagram to show the corresponding Q outputs.

C	0	1	1	0	0	0	1	1	1	0

Assume that Q starts in state of 1.

(c) Define the following

(i) Asynchronous Transfer. (ii) Serial Transfer

(iii) Propagation time.

14. (a) Explain briefly how an encoder works

(b) Write short notes about the following

(i) Wire Ored gates

(ii) Tristate gates

(iii) Delays

(iv) Races

15. (a) Explain briefly how a sequential adder works

(b) Explain how a decade counter works

(c) What is the difference between a **Full Adder** and a **Half Adder**?

(d) Use a Truth Table to help you explain how a Full Adder is constructed

(e) Use an example to help you explain what is meant by a **period** when dealing with timing diagrams.

List and explain the aids you need in order to construct Sequential Diagrams

16. (a) (i) Draw diagrams of two combinatorial circuits that are equivalent:

(ii) Use a truth table to show that the two diagrams you have drawn above are equivalent.

(b) Assume the following J, C, K, inputs of a J-K flip-flop and draw the corresponding diagram showing these inputs and the outputs corresponding to the given inputs. Assume initially that the output Q is in a state of 0.

J	1	0	0	1	1	1	1	1
C	1	1	0	0	1	1	0	0
K	1	0	1	1	1	1	1	0

(c) Assume the following inputs for the D flip-flop

D	0	1	1	0	1	1	1	0
C	0	0	1	1	1	0	1	0

Draw a timing diagram for these inputs and the Q outputs assuming:

(i) An ordinary Flip-flop

(ii) A positively edged flip-flop

(iii) A negatively edged flip-flop

17. (a) Why are some registers called shift registers and where are they used?

(b) Assume an 8 bit register has the following contents

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1	0	1	0	1	1	1	0

(i) What will its contents be after **shifting** it 3 times to the left?

(ii) What will its contents be after **rotating** it 3 times to the left?

(c) An ASCII character Z = 5A is to be transmitted using serial asynchronous transfer. Draw its timing diagram assuming that a character is transmitted with a start bit, a parity bit and two stop bits.

(d) Explain the features of the different methods used in data transmission. Give the advantages and disadvantages of these methods.

(i) Define a Delay and explain briefly how Delay Circuits are constructed.

18. (a) Use a diagram to help you explain briefly how Serial Input can be converted into parallel output

(b) What are the advantages of Serial transfer as compared to parallel transfer?

(c) A three character word YOU is to be transmitted.

(i) Show how it should be transmitted on a timing diagram assuming serial transfer with a start bit, a parity bit and a stop bit.

(ii) How would it appear if parallel transfer is used?

(d) Explain briefly how a master-Slave J-K flip-flop works.