MAKERERE UNIVERSITY

SCHOOL OF COMPUTING & INFORMATICS TECHNOLOGY

END OF SEMESTER I EXAMINATION 2017/2018

PROGRAMME: BCS and BSSE

YEAR OF STUDY: BCS I and BSSE II

COURSE NAME: COMPUTER ORGANISATION AND ARCHITECTURE

COURSE CODE: CSC 1104

DATE: 14th DECEMBER 2017 **TIME: 04:00 p.m. – 7:00 p.m.**

EXAMINATION INSTRUCTIONS

1. **ATTEMPT ALL QUESTIONS IN SECTION A (40 MARKS)**
2. **ATTEMPT THREE (03) QUESTIONS IN SECTION B (60 MARKS)**
3. **DO NOT OPEN THIS EXAM UNTIL YOU ARE TOLD TO DO SO**
4. **ALL ROUGH WORK SHOULD BE IN YOUR ANSWER BOOKLET**

SECTION A [40 Marks]

(a) (i) Differentiate Computer Organization from Computer Architecture **(2 Marks)**

(ii) List any two attributes of Computer Architecture. **(2 Marks)**

(b) Given a Binary number 10110011.11011_2 find its equivalent in

(i) Octal (Base 8) **(2 Marks)**

(ii) Hexadecimal (Base 16) **(2 Marks)**

(iii) Decimal (Base 10) **(2 Marks)**

(c) Estimate the biggest base ten number that can be expressed in 64 bits assuming that the bits are expressed as:

(i) An Ordinary Binary number **(2 marks)**

(ii) A Sign Magnitude Number **(2 marks)**

(d) Name and draw Logic Gates with the following characteristics:

(i) It outputs 1's if all the inputs are the same **(2 marks)**

(ii) It outputs 1's if all the inputs are 0's. **(2 marks)**

(e) Use examples to help you explain the following:

(i) A Literal **(1 mark)**

(ii) A Miniterm **(1 mark)**

(iii) A Maxiterm **(1 mark)**

(f) (i) What is a Demultiplexer? **(1 mark)**

(ii) Draw a logic diagram for a 1-3 Demultiplexer **(2 marks)**

(iii) How many control lines would you need to design a 1-7 Demultiplexer? **(1 mark)**

(g) Some Error Detection schemes use Parity Bits.

(i) What is a Parity Bit? **(1 mark)**

(ii) Differentiate Even Parity from Odd Parity **(2 marks)**

(h) (i) Use a diagram to help you explain what you understand by **a period**. **(2 marks)**

(ii) A Sine Curve makes 120 periods in two seconds. What is its frequency? **(2 marks)**

(i) Assume that an 8bit register is loaded with a Hexadecimal number DC_{16}, what are its new contents after the following operations assuming that the carry bit is 1?

(i) RLC (ii) RAR **(1 mark each)**

(j) (i) Find the corresponding postfix expression for the infix expression

$$\frac{(p*q)(a+b)}{c} + \frac{(a*b)(p-q)}{d}$$ **(3 marks)**

(ii) Derive the infix expression for the postfix expression below:

a b* c d + * p q * a f - * - r / **(3 marks)**

SECTION B [60 Marks]

Question 1:

(a) Consider a Decimal Number -125_{10} and write its equivalent as:

(i) An ordinary Binary Number **(1 mark)**

(ii) An 8 bit Sign magnitude number **(1 mark)**

(iii) An 8 bit Two's Complement Number **(1 mark)**

(iv) A Typical 32 bit Floating Point Number **(2 marks)**

(v) A Double Precision IEEE Floating Point Number **(2 marks)**

(b) Use an example to help you explain how you would detect a Numeric Overflow when working with Two's Complement Numbers. **(2 marks)**

(c) The two numbers A = C2D80000 and B = 41100000 are Single Precision IEEE Floating Point numbers, find

(i) A + B **(3 marks)**

(ii) A * B **(3 marks)**

(iii) A /B **(3 marks)**

(d) Add the two numbers +5678 and -2489 as Packed BCD numbers **(2 marks)**

Question 2:

(a) (i) Use a Truth Table to prove whether $\bar{A}+\bar{B}+\bar{C}$ is equivalent to $\overline{A+B+C}$ **(3 marks)**

(ii) Use Boolean Algebra to help you simplify the following expression:

$\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + ABC$ **(3 marks)**

(b) A Karnaugh Map is described by an expression $F(A,B,C,D) = \sum(0,5,7,8,10,12)$

(i) Draw a Truth Table corresponding to the above expression. **(3 marks)**

(ii) Generate the corresponding Sum of Products expression **(3 marks)**

(iii) Simplify the expression using the Karnaugh Map method **(3 marks)**

(iv) Simplify the same expression again using the Karnaugh Map method assuming that there are also some Don't Care cases described by an expression $d(A,B,C,D) = \sum(1,2,13,14,15)$ **(3 marks)**

(v) Draw a Logical Diagram corresponding to the simplified expression from part (iv) above. **(2 marks)**

Question 3:

(a) Explain briefly how a Half Adder differs from a Full Adder **(2 marks)**

(b) (i) Starting from a Truth Table, derive an expression for a 1-2 Demultiplexer and hence draw a corresponding Logical Diagram. **(6 marks)**

(ii) How many control lines would you need to draw a 6-1 Multiplexer? (**1 mark**)

(c) (i) What is a Decoder? **(1 mark)**

(ii) Draw a Truth Table for a decoder with three inputs and six outputs. **(3 marks)**

(iii) Draw a Logical diagram corresponding to the table in part (ii) above. **(3 marks)**

(d) Use an example to help you explain the difference between a ROM circuit and a Programmed Logic Array. **(4 marks)**

Question 4:

(a) Draw a symbol, a defining table and a well labelled diagram for a J-K flip flop. **(6 marks)**

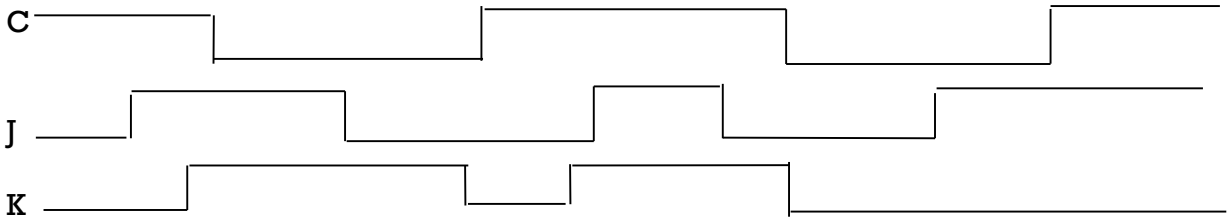
(b) The Timing diagrams below show inputs for the J-K flip-flop. Give corresponding Q outputs assuming that it is:

(i) An Ordinary Flip-flop (a latch) **(2 marks)**

(ii) A positively edge triggered flip-flop **(2 marks)**

(iii) A negatively edge triggered flip-flop **(2 marks)**

Assume in all cases that the initial state of Q is 0



(c) (i) How does a normal J-K flip flop differ from a Master-Slave J-K flip-flop? **(2 marks)**

(ii) How would you modify a J-K flip flop to get a T flip flop? **(2 marks)**

(d) (i) Explain briefly advantages of Parallel Data Transmission over Serial Transmission. **(2 marks)**

(ii) An ASCII character 71 is to be transmitted in serial using 8 data bits, one start and one stop bit. Show how this can be represented on a timing diagram. **(2 marks)**

Question 5:

(a) (i) What are the components of the CPU's Control Unit? **(2 marks)**

(ii) Give the functions of each of the mentioned components in part (i) above. **(4 marks)**

(iii) Give the main functions of the Arithmetic and Logic Unit. **(2 marks)**

(b) Why do you think that accessing a register in faster than accessing memory? **(2 marks)**

(c) A new microprocessor has just been manufactured. Explain the factors you will need to consider when studying this new microprocessor. **(5 marks)**

(d) Assume that the bus of this processor has 64 address lines and that the most 4 significant bits are used to identify a memory module.

(i) What is the address space of its memory? **(1 mark)**

(ii) What is the total amount of memory it can access? **(1 mark)**

(iii) How many bits are used to write an address of its memory location? **(1 mark)**

(iv) How many modules are in this memory **(1 mark)**

(v) How big is each module? **(1 mark)**