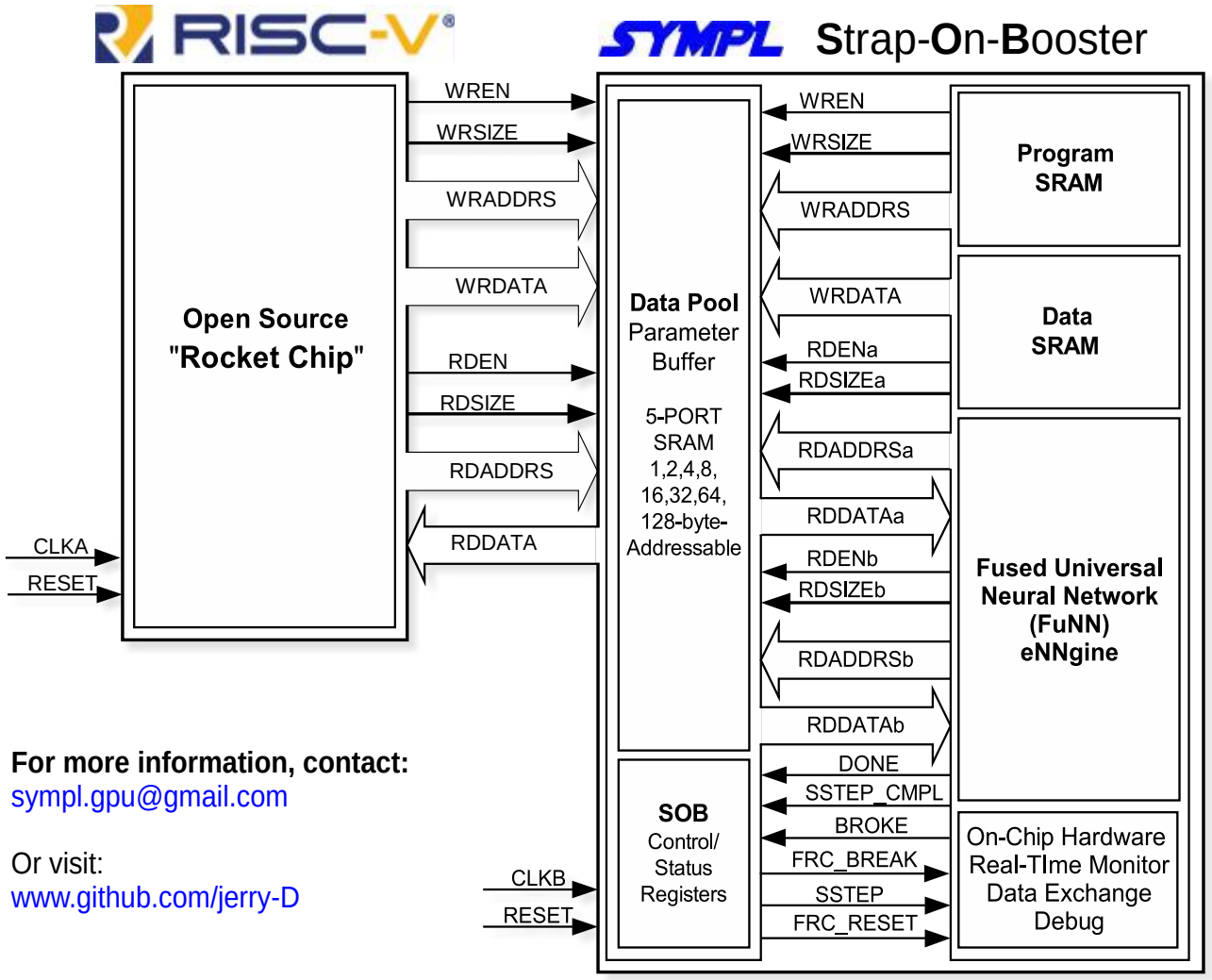
Universal Floating-Point Strap-On-Booster ("SOB")

Designed for ready implementation in XILINX® Kintex® Ultra™ FPGAs, the ***SYMPL* SOB** is designed to give your RISC-V "Rocket Chip" heavy lift capability, especially for web-based Artificial Intelligence (AI) applications. Here's why:

- Simple SRAM interface permits easy connection of SOB to your Rocket Chip directly (as if SRAM) or via AXI4 interface
- 64-bit universal floating-point ISA can pull/push dual operands (scalars or vectors) of up to 128 bytes each every clock cycle using REPEAT and auto-post-modify indirect addressing mode
- Automatic conversion of human-readable decimal character sequences up to 28 decimal digits in length to bfloat16, binary16, binary32 or binary64 format numbers with **zero** latency in big data scenarios
- Special cascaded instructions allow a single "parent" SOB to have as many as qty. (16) "child" SOBs connected to it and allow 100% visibility into them in real time
- 16-input x 16-layer Fused Universal Neural Network (FuNN) eNNgine that can compute directly with human-readable decimal character sequences and includes 10 built-in single-clock activations and their derivatives such as TanH, Logistic, SQNL, SoftPlus, Gaussian, SQ-RBF, ReLU, LReLU, SoftMax, HardMax, Exponential (refer to the SYMPL FuNN eNNgine flyer for more information)
- Implements in hardware **ALL** IEEE® 754-2008 mandated operators with a single instruction per operation. Since all operators are memory-mapped, you can easily add, remove or replace any of these with your own custom operators/TPUs, NPUs, etc., to implement RNNs, LSTMs, DNNs, etc.
- Simple hardware allows RISC-V to issue individual commands to perform single operations on scalar or vector operands or you can easily push your own programs and data set into it.

Preliminary Information



For more information, contact:
sympl.gpu@gmail.com

Or visit:
www.github.com/jerry-D

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