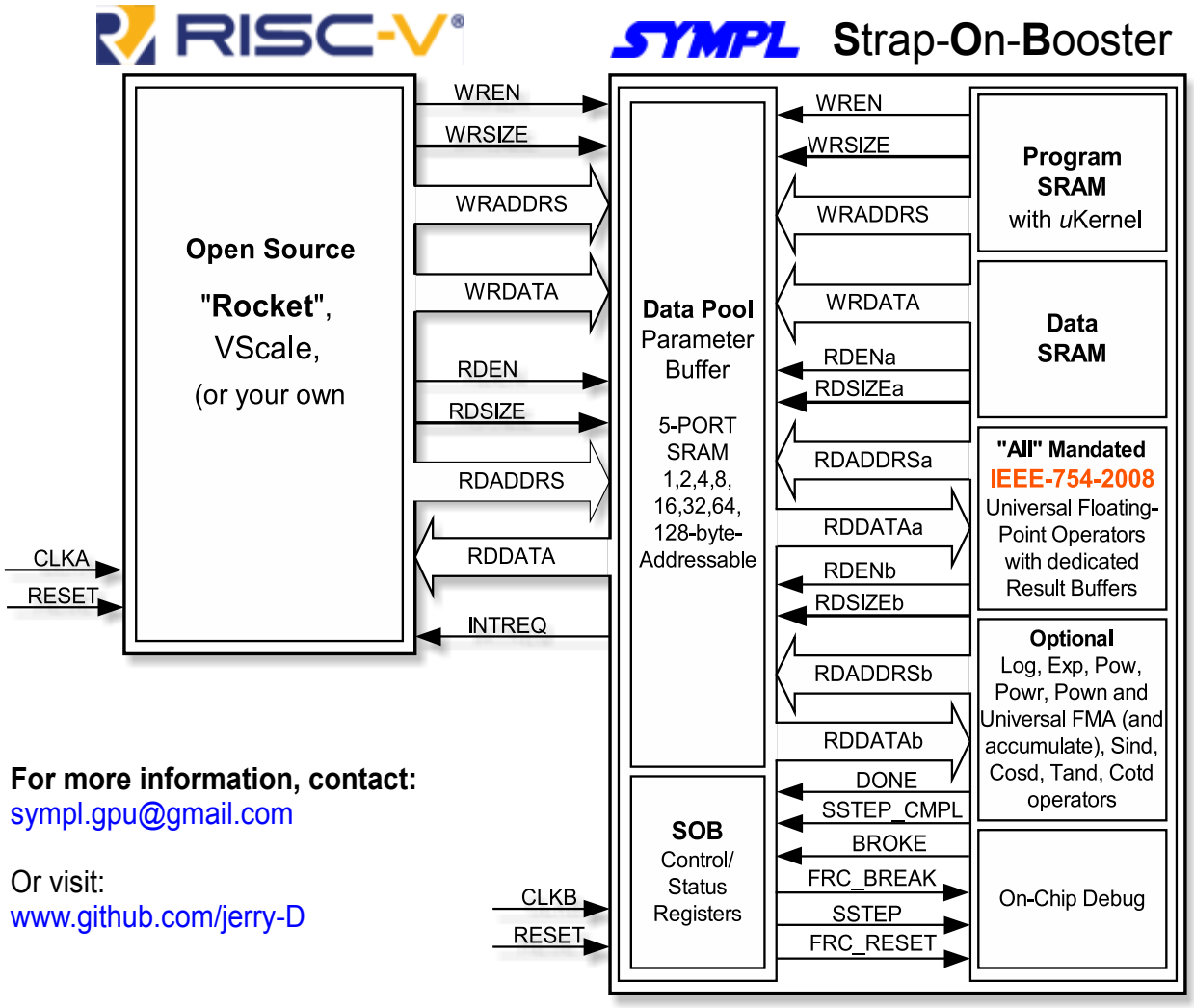
SYMPL Compute Engines

Universal Floating-Point Strap-On-Booster ("SOB")

Designed for ready implementation in XILINX® Kintex® Ultra™, INTEL® ARRIA®, and MICROCHIP PolarFire™ -class FPGAs, the ***SYMPL* SOB** is designed to give your RISC-V "Rocket Chip" heavy lift capability, especially for web-based Artificial Intelligence (AI) applications. Here's why:

- ❑ Simple SRAM interface permits easy connection of SOB to your Rocket Chip directly or via AXI4 interface
- ❑ 64-bit "opcode-less" ISA can pull/push dual operands (scalars or vectors) of up to 128 bytes each every clock cycle using REPEAT and auto-post-modify indirect addressing mode
- ❑ Automatic conversion of human-readable decimal character sequences up to 28 decimal digits in length to bfloat16, binary16, binary32 or binary64 format numbers with **zero** latency in big data scenarios
- ❑ Special cascaded instructions allow a single "parent" SOB to have as many as qty. (16) "child" SOBs connected to it
- ❑ Universal FMA with qty. (32) "fat" accumulators can compute DIRECTLY with human-readable decimal character sequences up to 28 decimal digits in length--including those with "token" exponents, e.g., "K", "M", "B", "T" and "%"
- ❑ Implements in hardware **ALL** IEEE® 754-2008 mandated operators with a single instruction per operation. Since all operators are memory-mapped, you can easily add, remove or replace any of these or your own custom operators/TPUs. For example: RNNs, LSTMs, DNNs, etc.
- ❑ Simple micro-kernel allows RISC-V to issue individual commands to perform single operations on scalar or vector operands or you can push your own programs and data set into it



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Preliminary Information

Version 1.00 Sept. 10, 2019

SYMPL is presently an alias used by an individual developer.
SYMPL Strap-On-Booster IP is presently not available for commercial use.