1. sti Rt, Rs, Imm

a. ALUSrc : 1
b. RegDst : 0
c. ALUOp : 10
d. MemWrite : 0
e. MemRead : 0
f. Branch : 0
g. MemtoReg : 0
h. RegWrite : 1

2. andi Rt, Rs, Imm

f

3. sw Rt, Offs(Rs).

b

4. since longest operation is "lw" which needs

IM → RRF → Mux → ALU → DM → Mux → W RF

400 + 180 + 80 + 150 + 320 + 80 + 180 = 1390 ps  $f_{mx} = \frac{1}{1390 \times 10^{-12}} = 7.19 \times 10^{8}$ Hz

400 + 100 + 80

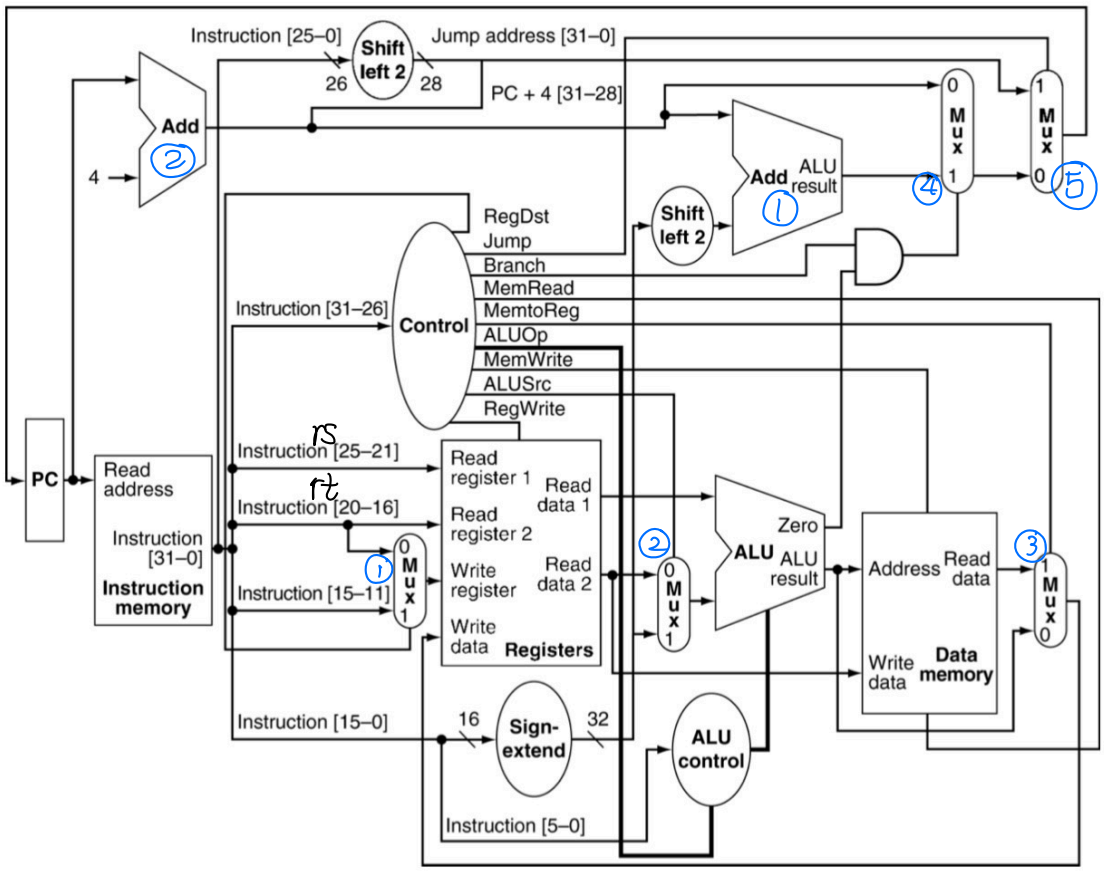
= 1310 ps

5. set PC at 0x00080000. since affected signal has either stuck-at-0 or stuck-at-1 fault. we use instruction

addi $s0, $0, 1

if $s0 value is 1, there is stuck-at-0 fault on bit 16 of output of IM. otherwise there is not stuck-at-0 fault.

6.




$2^4 + 2^2$

10101 00011 00010 0000000000000100

43 3 2

sw ← 2 b  $V1 rs  $V0 rt  20.

SW $V0, 20($V1)

for mux ①: we don't care its output

mux ②: 0000 0000 0000 0000 0000 0000 0000 0100

mux ③: 24 X

mux ④: PC + 4.

mux ⑤: PC + 4.

ALU input: 4, 20

Add ① input: PC + 4, 80.

Add ② input: PC, 4

Read register 1: 00011

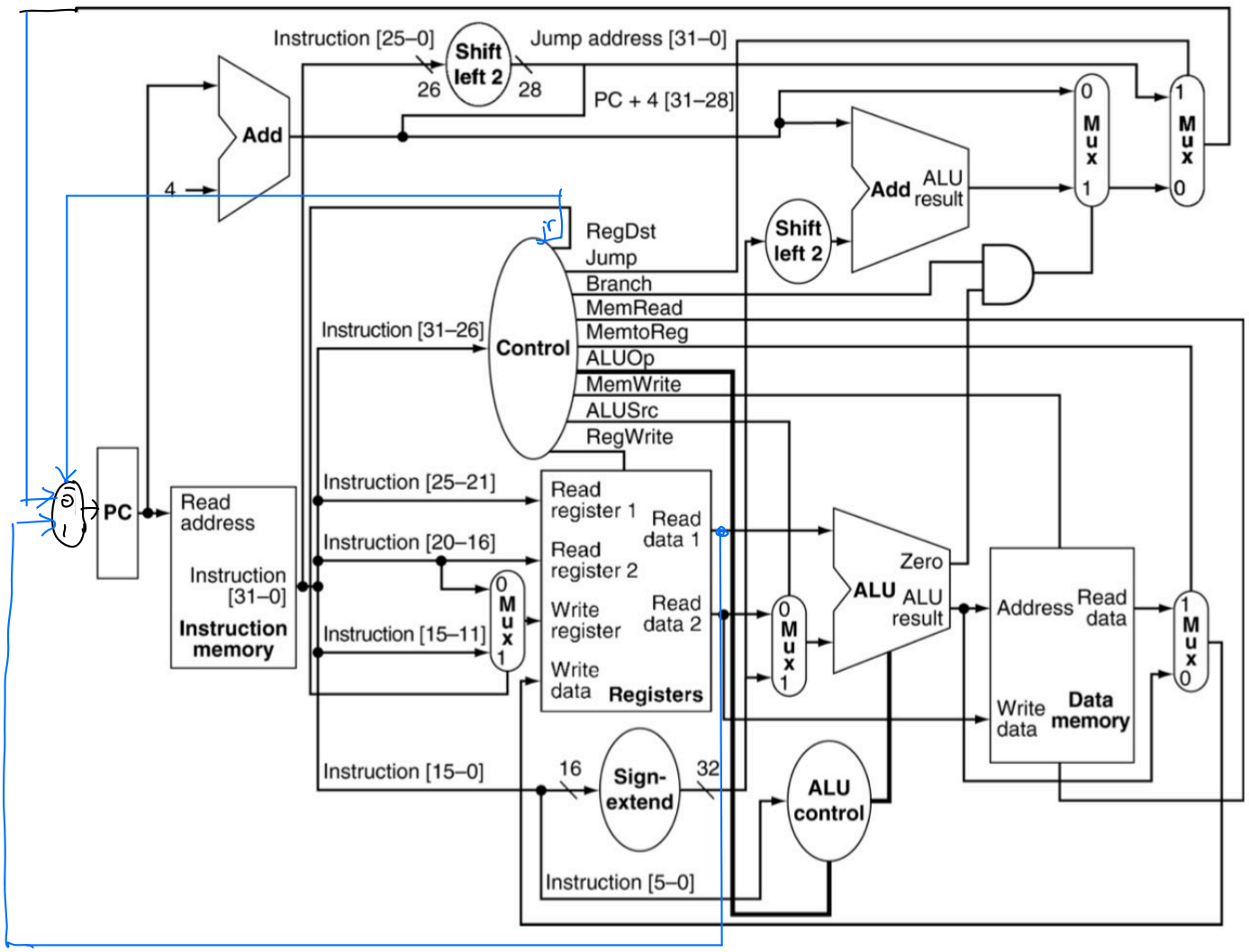
Read register 2: 00010

Write register: don't care

Write data: don't care

RegWrite: 0.

7. we can add a control signal Jr. determined by ALUop and instruction [5:0]. Add a mux before PC, when control signal of jr is 1, mux will output data of Read data 1. when jr is 0, mux will output origin value.




8- 1) Critical path is Register → Mux → ALU
100 + 30 + 120 = 250 ps
v Reg → ALU
Sign → Mux → ALU
100 + 120 = 220ps
?

control signal can take 250 ps to generate MemWrite signal

2) ALUOp is the most critical control signal to generate quickly. It needs to generate in 100+30-50=80ps.

critical Reg → ALU ∴ AluSrc 100-30=70ps
100ps ALU Op 50 ps

9. 1) 360 ps

2) 300 + 200 + 280 + 360 + 180 = 1320ps  360 × 5 = 1800ps

3) clock cycle = Instruction + 4 = 2004.

2004 × 360 = 721440 ps.

$CPI = \frac{2004}{2000} = 1.002$