CPE 487: Digital System Design

Design Project:

Due date:
For Part I: 4/26/17
For Part II: 5/5/17

Note:

(1) This is a design project and will take you sometime to finish it. So, I suggest you to start this home work immediately.
(2) The total points for part I is 50 points, and part II is 25 points.
(3) To get full credit for Part I, you MUST simulate your design so as to fully test the functionality of the counter and print your simulation results clearly.

Part I: (50 points)
This homework requires you to design a behavioral model of a MOTOROLA MC14510B binary-coded-decimal (BCD) counter. Your tasks include:

(1) Read carefully the Data Sheet of Motorola MC14510B (download at the class schedule web page). Please pay special attention to page 1 (the Truth Table), page 5 (State diagram for up counting and down counting), page 6 (input and output signals) and page 7 (simulation waveform)

(2) Your external interface should include these signals:
Input signals:
pre_set, cin_b, reset, updown, clk, P (3 downto 0)
Output signals:
cout_b, Q (3 downto 0)

You can use whatever name for the above signals that you'd like, this is just to give you an example that what kind of interface signals you should have in your Entity according to the Data Sheet. Please use a std_logic_vector for the 4-bit parallel input signal and the 4-bit counter output.

(4) Write your own VHDL code to build a behavioral model of this 4-bit BCD counter and simulate it. You need to test the truth table, and cover all the illegal states as shown in Page 5 in your simulation. Show your VHDL code and simulation results. In your simulation waveforms, please display the counter output as unsigned decimal. Also, please annotate your simulation results to mark and explain different testing points. Note: In your design, you DO NOT need to model the delay times

Part II (25 points)

(1) Modify your 4-bit counter so that the pre-set operation becomes synchronous. That is, the pre_set operation only occurs on a rising clock edge. If a rising clock edge

occurs while pre_set is high, the input data on P is loaded into the counter. Show your code and simulate your design with sufficient vectors to check the modified pre_set operation.

(2) Based on your new 4-bit BCD design, use structural modeling to design a 16-bit (4-digit) BCD counter. Show your code. You DO NOT need to show simulation results for this part.