PolarFire Design Document

Out of The Box (OTB) System

rev 1.00.000

1. Overview

The goal of this Out of The Box design is to provide a starting point to develop a Mi-V IP based system on the Avalanche Development Board targeting the Microsemi PolarFire FPGA.

Some features of the Avalanche board are included in this design: UART, user LEDs, minimal Wi-Fi interface and pushbuttons. On the RISC-V side: Interrupts (System Timer, External IRQs), programmable Timer, GPIO and UART configuration and management and access to different memory devices.

A production (CM) test routine is also hidden in the design. It is activated by depressing pushbutton #2 for more than 2 seconds. The only way to exit this test is to reset the board.

2. Description

Platform	Avalanche Development Board
Target	PolarFire MPF300TS-1FGC484
Clock(s)	Main: 50MHz MMIO Sub-system: 50 MHz
FPGA usage	Around 15.2k LE (5.1%)

3. Functions

Device	Description
UART	- Use to communicate/interact with the board. - Echo text received back to the host when the Morse emitter is active. - Send messages/instructions to the host for the BIT execution.
System Timer	- Generate a 0.5 Hz heartbeat on the green LED 2 (not active during BIT execution)
Pushbutton #1	- Upon depression, activate/deactivate a Morse code emitter. If activated, any character typed in the Terminal window of the host computer will be encoded and emitted using LED 1 red.
Pushbutton #2	- Upon depression, start an advanced BIT with messages/results sent to the Terminal window of the host computer. - Upon depression for more than 2 seconds, start a production (CM) test routine.

Delay Timer	- Programmable timer used to generate delays during the BIT and Morse code emitter.

4. FPGA Blocks Configuration

Device	Configuration
CoreUARTapb	Configured through Mi-V code (115200 / 8 / 1 / No parity / No Flow Control)
CoreGPIO_Basic	User pushbutton #1: GPIO_0 - INT[0] connected to Mi-V External IRQ 30 User pushbutton #2: GPIO_1 - INT[1] connected to Mi-V External IRQ 29 LED 1 green: GPIO_2 LED 1 red: GPIO_3 LED 2 green: GPIO_4 LED 2 red: GPIO_5
CoreGPIO_Pan9320	FACT_RST signal: GPIO_0 nRESET signal: GPIO_1
CoreTimer	Timer interrupt connected to Mi-V External IRQ 28

5. Memory Description

Memory Device	Type	Size
Mi-V Boot	LSRAM	128KB (32768 x 32 bits)

6. Memory Map

Device	First Address	Last Address
MMIO – UART	0x6000 0000	0x6000 0FFF
MMIO – GPIO (LEDs/Pushbuttons)	0x6000 1000	0x6000 1FFF
MMIO – GPIO (Pan9320)	0x6000 2000	0x6000 2FFF
MMIO – GPIO (Timer)	0x6000 3000	0x6000 3FFF
Memory – Mi-V Boot (LSRAM)	0x8000 0000	0x8001 FFFF