PolarFire Design Document

ADC (MCP93x3) Demo

rev 1.1.000

1. Overview

The goal of this ADC demo is to provide a starting point to work with the MCP93x3 ADC available on the Avalanche Development Board using a Mi-V softcore system.

Some features of the Avalanche board are included in this design: BasicIO Interface (UART, user LEDs and pushbuttons) and the MCP93x3 interface. On the RISC-V side: Interrupts (External IRQs), MCP93x3 drivers, GPIO and UART configuration and management and access to different memory devices.

2. Description

Platform	Avalanche Development Board
Target	PolarFire MPF300TS-1FGC484
Clock(s)	Main: 50MHz MMIO Sub-system: 50 MHz
FPGA usage	Around 15.5k LUT (5.1%)

3. Functions

Device	Description
Basic IO - UART	- Use to communicate/interact with the board. - Echo values read from the ADC channels.
System Timer	- Generate a 0.5 Hz heartbeat on the green LED 2.
Basic IO - Pushbutton #1	- Upon depression, read ADC channel 0 and send it to the host PC serial terminal.
Basic IO - Pushbutton #2	- Upon depression, read ADC channel 2 and send it to the host PC serial terminal.

4. FPGA Blocks Configuration

Device	Configuration
BasicIO_Interface	UART for Terminal communication configured through Mi-V code (115200 / 8 / 1 / No parity / No Flow Control) User pushbutton #1: USER_PB1_IRQ connected to Mi-V External IRQ 30 User pushbutton #2: USER_PB2_IRQ connected to Mi-V External IRQ 29 Other ports pushed as Top Level ports to be mapped on I/O pads.
MCP9303_Interface	ADC_DR_N input: set to VCC, not using the ADC IRQ feature DATA_IRQN output: not connected to Mi-V core

5. Memory Description

Memory Device	Type	Size
Mi-V Boot	LSRAM	128KB (32768 x 32 bits)

6. Memory Map

Device	First Address	Last Address
MMIO – BasicIO_Interface	0x6000 0000	0x6000 0FFF
MMIO – MCP9303_Interface	0x6000 1000	0x6000 1FFF
Memory – Mi-V Boot (LSRAM)	0x8000 0000	0x8001 FFFF