Igloo 2 Design Document

RISC-V Systick Blinky (Hello World!)

1. Overview

The goal of this Out of the Box design is to provide a starting point to develop a RISC-V system on the Creative Development Board targeting the Microsemi Igloo2 FPGA.

Some features of the Creative board are included in this design: UART, user LEDs and pushbuttons. On the RISC-V side: Interrupts (System Timer), GPIO and UART configuration.

2. Description

Platform	Creative Development Board
Target	IGLOO 2 M2GL025-VF256
Clock(s)	Main : 66 MHz MMIO Sub-system : 66 MHz DDR2 : 132 MHz
FPGA usage	Around 55%

3. Functions

Device	Description
UART	- At power-up, send “Hello World!” to the host - Echo text received back to the host afterward.
System Timer	- Generate a 4 LED pattern (LED2 green, LED1 green, LED2 red, LED1 red) every 2 seconds.
Pushbutton #1	- Upon depression, freeze LED1 red until it is released.
Pushbutton #2	- Upon depression, freeze LED2 green until it is released.
Timer_0	- No currently used (RISC-V code required)
Timer_1	- No currently used (RISC-V code required)

4. FPGA Blocks Configuration

Device	Configuration
CoreUARTapb	Configured through RISC-V code (115200 / 8 / 1 / No parity / No Flow Control)
CoreGPIO_IN	Hard configuration User pushbutton #1: GPIO_0 User pushbutton #2: GPIO_1
CoreTimer_0	TIMNT connected to RISC-V External IRQ 29
CoreTimer_1	TIMNT connected to RISC-V External IRQ 30
CoreGPIO_OUT	Hard configuration - LED 1 green: GPIO_2 - LED 1 red: GPIO_0 - LED 2 green: GPIO_1 - LED 2 red: GPIO_3

5. Memory Description

Memory Device	Type	Size
RISC-V Boot	eNVM	4.6KB (4728 x 8 bits)
RAM	DDR2	64MB (32M x 16 bits)

6. Memory Map

Device	First Address	Last Address
MMIO – UART	0x7000 1000	0x7000 1FFF
MMIO – GPIO-IN (Pushbuttons)	0x7000 2000	0x7000 2FFF
MMIO – Timer_0	0x7000 3000	0x7000 3FFF
MMIO – Timer_1	0x7000 4000	0x7000 4FFF
MMIO – GPIO_OUT (LEDs)	0x7000 5000	0x7000 5FFF
Memory – RISC-V Boot	0x6000 0000	0x6000 1277
Memory – RAM	0x8000 0000	0x81FF FFFF