Creative Design Document

FreeRTOS on Mi-V Demo

rev 1.00.000

1. Overview

The goal of this FreeRTOS on Mi-V demo is to provide a starting point to work with FreeRTOS on a Mi-V softcore system using the Creative Development Board.

Some features of the Creative board are included in this design: BasicIO Interface from the FPGA FE Library (UART, user LEDs, pushbuttons) and the DDR2 external memory. On the RISC-V side: FreeRTOS port (v 8.2.3), GPIO and UART configuration and management and access to different memory devices.

2. Description

Platform	Creative Development Board
Target	IGLOO2 M2GL025-VF256
Clock(s)	Main: 50MHz MMIO Sub-system: 50 MHz DDR2 : 100 MHz
FPGA usage	Around 13.6k LUT (49.10%)

3. Functions

Device	Description
UART	- Use to communicate/interact with the board.
LEDs	- Use to show the activity of the different tasks.
System Timer	- Not used in this demo.
Pushbutton #1	- Not used in this demo.
Pushbutton #2	- Not used in this demo.

4. FPGA Blocks Configuration

Device	Configuration
Basic IO - UART	Configured through Mi-V code (115200 / 8 / 1 / No parity / No Flow Control)
Basic IO - GPIO	User pushbutton #1: GPIO_0 - INT[0] connected to Mi-V External IRQ 30 User pushbutton #2: GPIO_1 - INT[1] connected to Mi-V External IRQ 29 LED 1 green: GPIO_2 LED 1 red: GPIO_3 LED 2 green: GPIO_4 LED 2 red: GPIO_5
CoreTimer	32 bits wide counter, configuration through Mi-V code TIMINT output: connected to Mi-V External IRQ 28

5. Memory Description

Memory Device	Type	Size
Mi-V Boot	eNVM	11.6KB (11632 x 8 bits)
RAM	DDR2	64MB (32M x 16 bits)

6. Memory Map

Device	First Address	Last Address
MMIO – Basic IO (UART, LEDs, PBs)	0x7000 0000	0x7000 0FFF
MMIO – Timer 1	0x7000 1000	0x7000 1FFF
Memory – Mi-V Boot	0x6000 0000	0x6000 2D70
Memory – RAM	0x8000 0000	0x81FF FFFF