



Experiment 5 - Design of an Operational Amplifier Using PSpice

Lab Report

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Abstract

This report uses PSpice to design an operational amplifier. In Op-Amplifier, four kinds of building blocks are used in the experiment: Emitter follower, common emitter amplifier in NPN transistor, current mirror circuit with Widlar current mirror, and a differential input stage with active load in single-end output. The experiment meets the requirements of the project by using a combination of building blocks. Besides, the voltage transfer curve (VTC), a standard method for measuring voltage gain, is also involved in the experiment. Finally, the frequency response of the amplifier circuit and the stability of the system will also be reflected in this report.

Declaration

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1 Introduction

This experiment using PSpice simulator to design and build an operational amplifier. As shown in Figure 1, four types of building blocks are needed to make the whole operational amplifier circuit in the experiment: Differential input stage with active load in single-end output for the first stage of an amplifier, emitter follower both can be used to adjust the AC load of the differential amplifier and used to decrease the output resistances of the op-amp, current mirror circuit to bias the current flow into both differential amplifier (Widlar current mirror) and common emitter amplifier [1]. Also, the main content of the experiment is to measure the input resistance, output resistance, voltage gain, and frequency response are designed to meet design requirements show in the objectives part. In this experiment, all the requirements of the experiment are achieved.

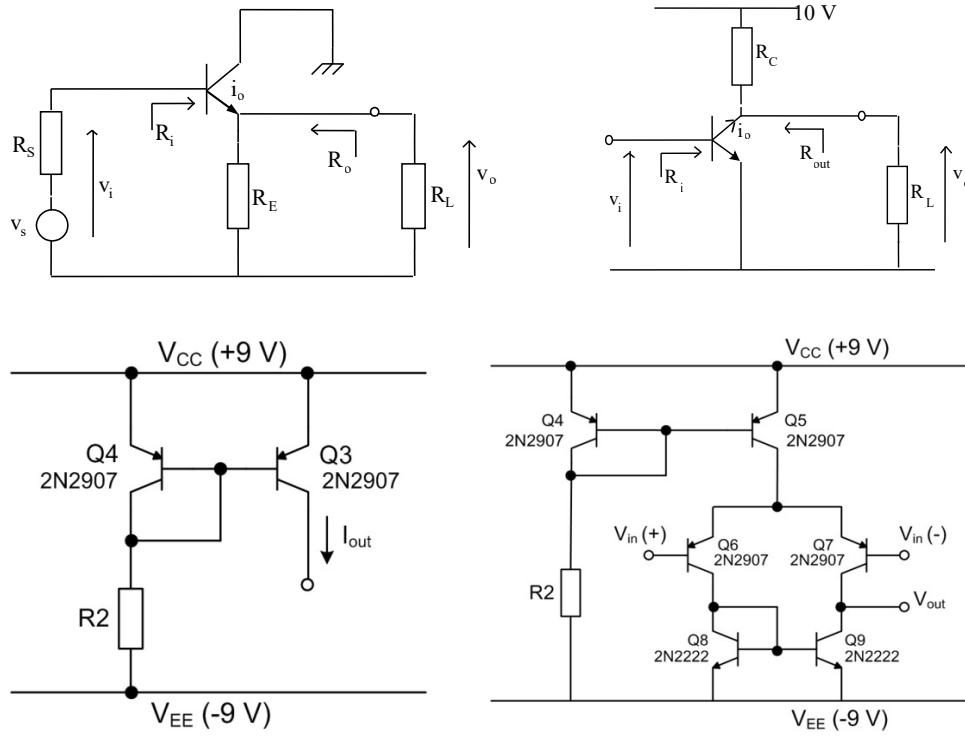


Figure 1. The Common Emitter Amplifier, Common Collector, Simple Current Mirror and Differential Amplifier with Widlar current mirror (taken from [2])

2 Objectives

The project objectives of this experiment can be divided into two parts: the first is the specifications of the project to be achieved, and the second is the skills of the experiment to be achieved.

2.1 Specification of Design

The design objectives of the experiment can be divided into two categories. The first category is the design objectives achieved by adjusting the bias current through theoretical calculation. The second category is the objectives that can be naturally achieved by using the pre-lab design method.

For the first category:

- The input impedance of the Op-Amplifier greater than $100\text{ k}\Omega$
- The output impedance of the Op-Amplifier less than $1\text{ k}\Omega$
- Open-loop voltage gain more significant than 500k
- The output voltage of Op-Amplifier near to the 0 Volt
- Current from the voltage source is less than 5 mA

For the second category:

- Frequency response down to DC
- A voltage source provides voltage from +9 to -9V

2.2 Skills and Course Objectives

- Build a circuit parallel using PSpice
- Understanding the characteristic curves of two different BJTs
- Understanding the internal structure and external encapsulation of Op-Amplifier
- Understanding the process of testing and designing Op-Amplifier
- Understand the frequency response and build Bode plots
- Understand the relationship between the stability of Op-Amplifier phase compensating capacitor

3 Theory

This chapter includes the function analysis of different building blocks and the configuration evaluation of the whole amplifier circuit of the experiment.

3.1 Building Blocks

3.1.1 Emitter Follower

In this experiment, two emitter followers are used in the circuit, the first part of which is used as a connection between the differential amplifier and the common emitter amplifier. As shown in Figure 2, The first emitter follower is used to improve the voltage gain of the differential amplifier because the emitter follower can provide a high input impedance. For the second emitter follower, it used to decrease the output impedance for the Op-amplifier.

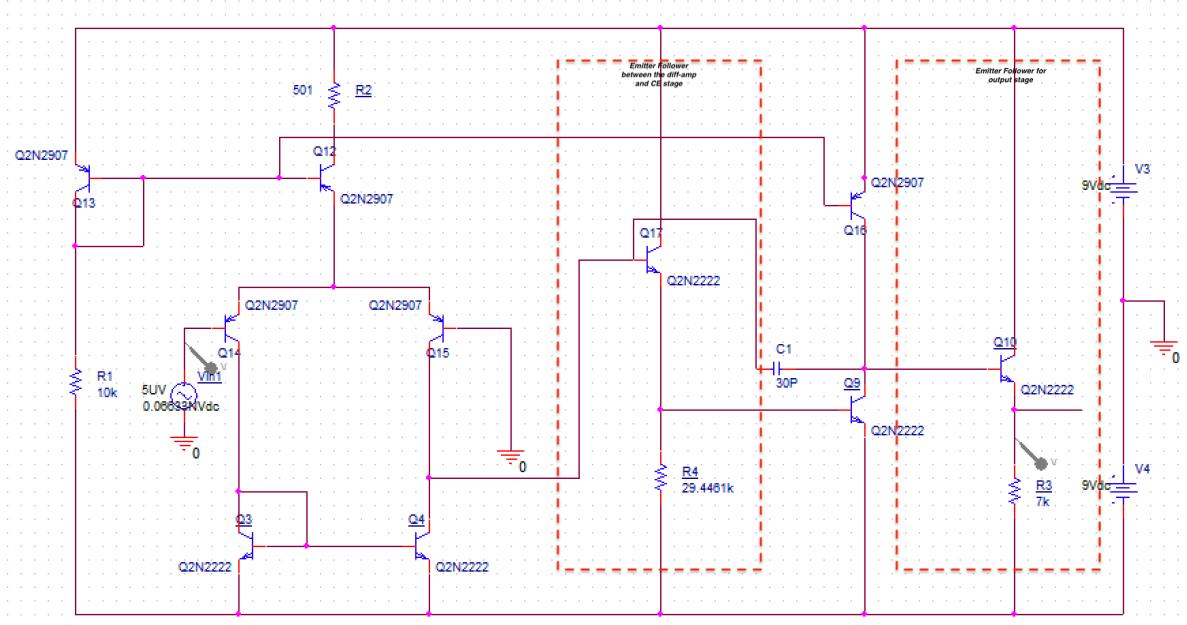


Figure 2. Common Collector Stage in Op-Amplifier

3.1.2 Common Emitter Amplifier

Common emitter amplifier is used as the second voltage gain, as shown in Figure 3, the voltage gain depends on the conductance g_m and AC load, which can be considered by the $R_{CE(NPN)}$ and $R_{CE(PNP)}$ in parallel. The calculation section will be expanded in the next chapter.

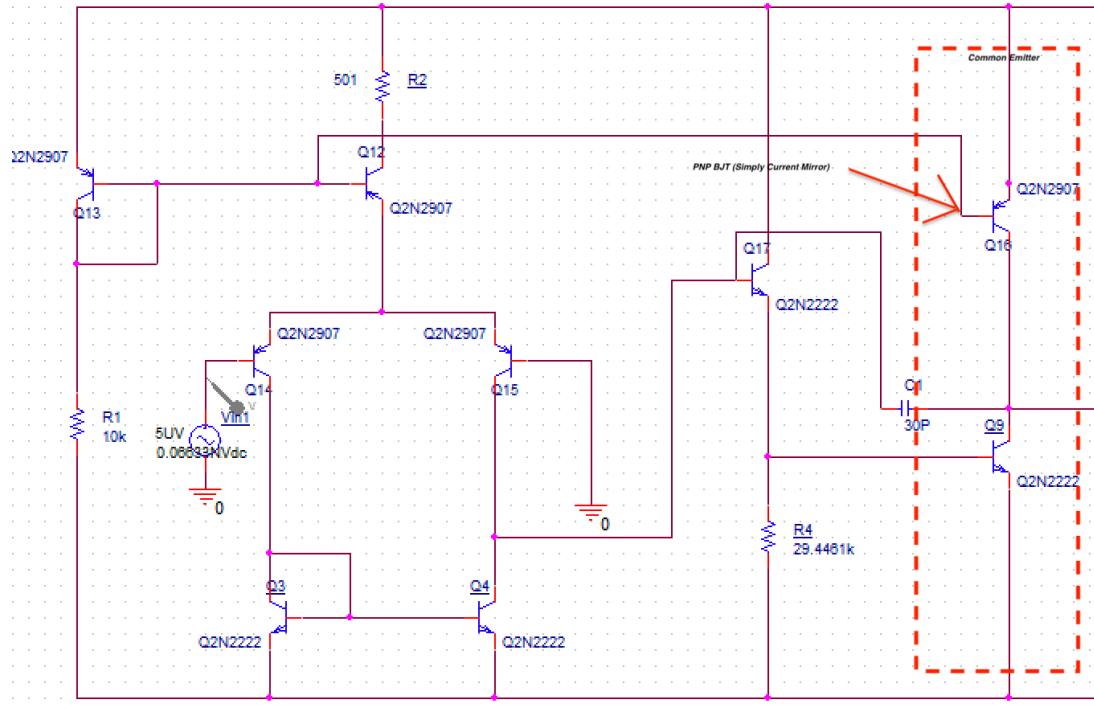


Figure 3. Common Emitter Stage in Op-Amplifier

3.1.3 Simple Current Mirror

As shown in Figure 4, the simple current mirror is used to bias the common-emitter stage, and the part of the differential amplifier stage also needs the I_{ref} to setup. However, in the actual experiment, the resistance of the mirror circuit is limited, otherwise, the current of the simple mirror circuit is quite different from the expected value.

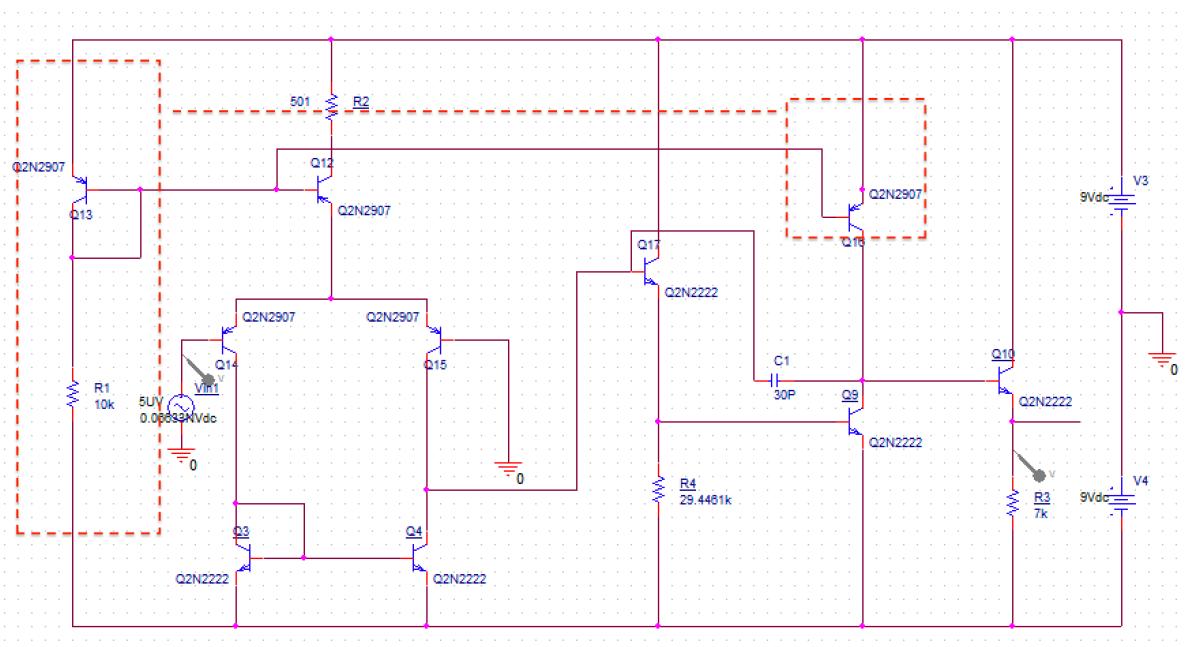


Figure 4. Simple Current Mirror

3.1.4 Widlar Current Mirror

For the Widlar Current Mirror in Figure 5, the output current of this circuit is supplied to the differential amplifier.

The current relationship between the I_{ref} and I_{out} is shown in the formula (1):

$$I_{out} R_E = V_T (\ln \frac{I_{ref}}{I_{out}}) \quad (1)$$

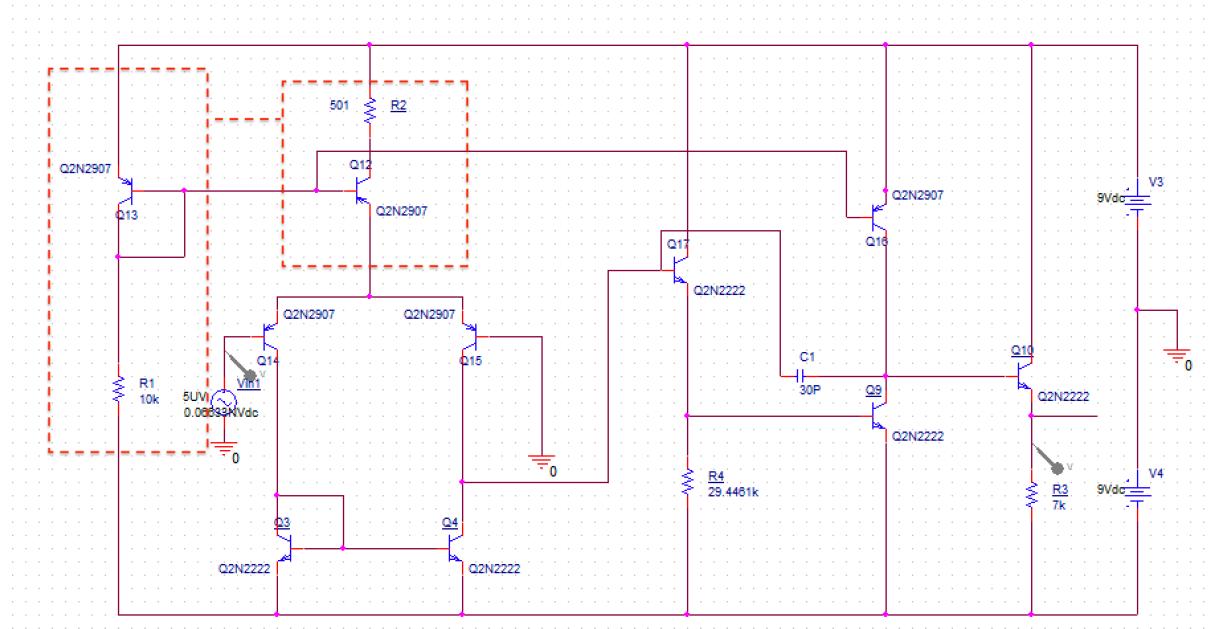


Figure 5. Widlar Current Mirror

3.1.5 Differential Amplifier

The differential input stage with active load in single-end output is the first stage to give the voltage gain. For the voltage gain of this stage shows in the formula (2) and (3):

$$A_{V(Diff)} = g_m \cdot AC\ Load \quad (2)$$

$$AC\ Load = R_{CE(Q2)} // R_{CE(Q4)} // R_{in(CC\ Stage)} \quad (3)$$

3.2 Op-Amplifier Circuit Configuration

The configuration of the Op-Amplifier circuit is shown in Figure 6, the two-differential input V_{in+} and V_{in-} with a phase difference of 180 degrees enter the differential amplifier, which has a single-ended output to the emitter follower stage, the emitter follower stage ensures the input impedance is approximately ten times that of the differential amplifier of AC load. Then the signal enters the common-emitter stage and is amplified again.

Finally, the signal is output to the emitter follower to ensure that the output resistance of the whole Op-Amplifier is less than $1\text{ k}\Omega$.

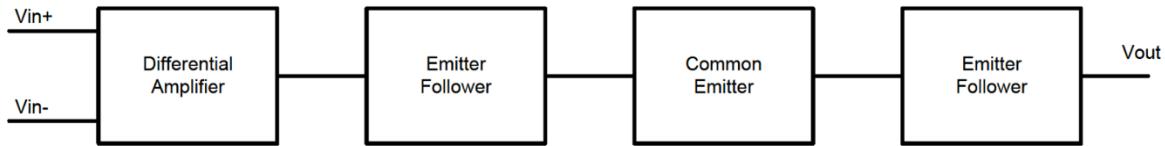


Figure 6. Block Diagram of Op-Amplifier (taken from [3])

4 Experiment Preparation - Transistor Output Characteristics

In this section, the 2N2222 transistor will be observed the characteristic output curve (I_c and V_{CE}). The V_{CE} is set to the 0 to 20 V in 0.5 V steps, and the range of I_B is set from 0 to 40 μA in steps of 4 μA .

4.1 Materials and Methods

All experiments below are based on OrCAD Capture CIS Lite 17.2 (PSpice). As shown in Figure 7, the experiment used bivariate Settings for V_{CE} and I_B , and the characteristic curve of 2N2222 NPN transistor was obtained by using a bivariate DC Sweep. The simulation configuration of this experiment is shown in Figure 8.

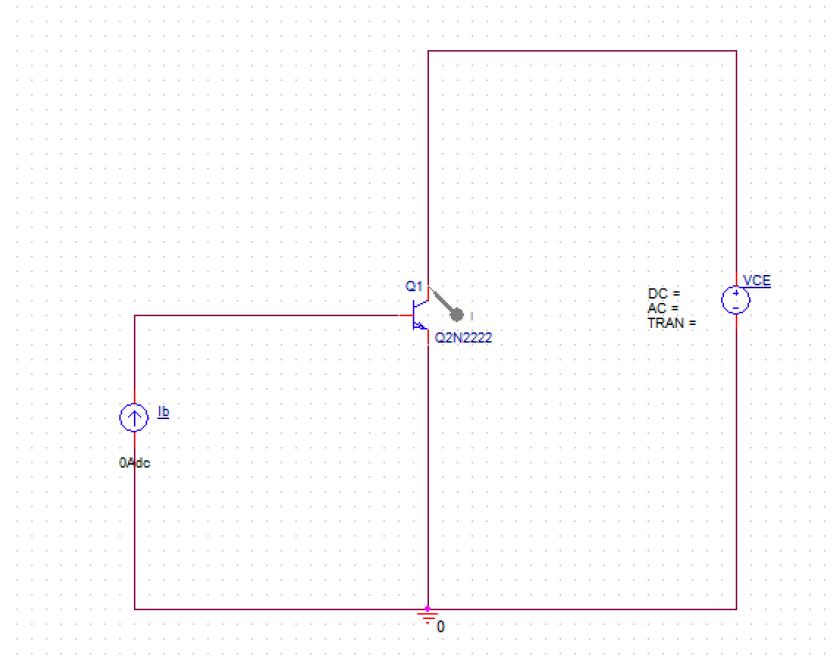


Figure 7. Part1 Circuit Diagram

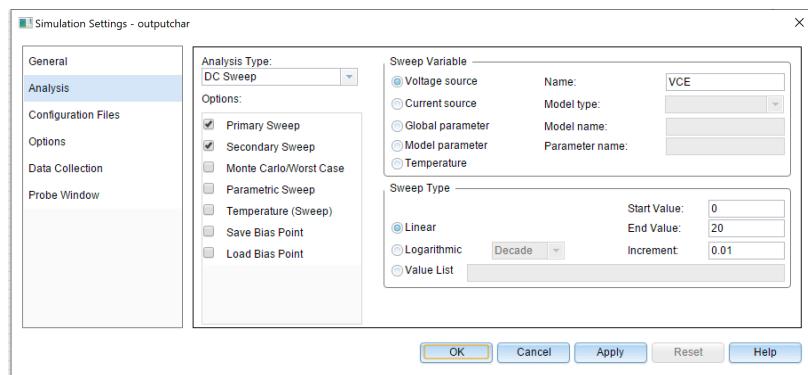


Figure 8. The Part1 Simulation Configuration

4.2 Results

The result of current gain is shown in Figure 9, and the DC current gain β in collector current at 2 mA, the β is calculated in the formula (4):

$$\beta = I_C / I_B = 2.0002 \text{ mA} / 12 \mu\text{A} \sim 166.6 \quad (4)$$

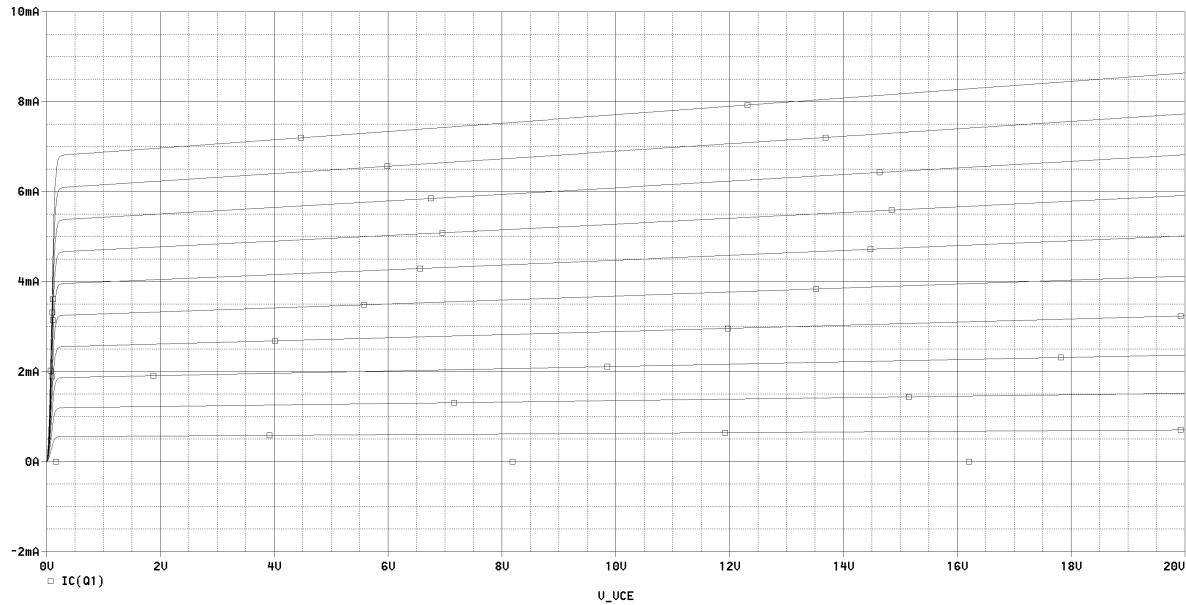


Figure 9. Characteristic Curve of 2N2222 NPN transistor

As shown in Figure 10. The AC current gain β_0 can be estimated by the formula (5):

$$\beta_0 = \Delta I_C / \Delta I_B \sim 183.225 \quad (5)$$

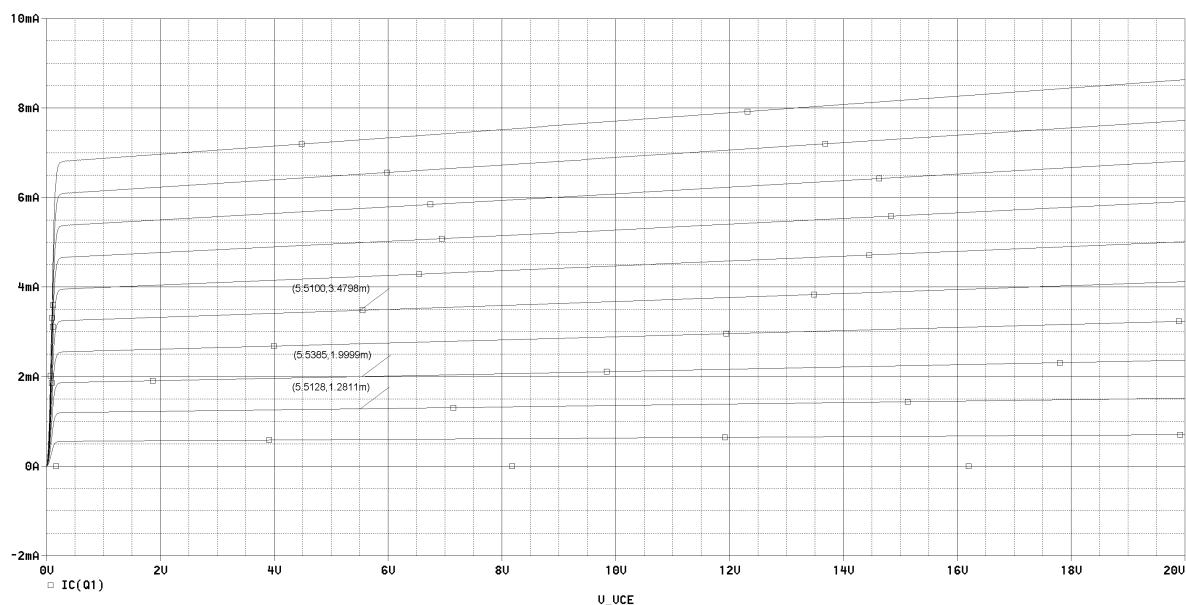


Figure 10. Characteristic Curve of 2N2222 NPN transistor in Calculating the AC Current Gain

5 Achieving the Specification of the Operational Amplifier

5.1 Theoretical Calculation

5.1.1 Theoretical Calculation Data Preparation

Based on Part 1 results and PSPICE catalog data, the parameters are shown in Table 2.

Table 2. Experiment Metadata of Q2N2222 and Q2N2907 (Typical Values)

| V_T | $V_{A(NPN)}$ | $V_{A(PNP)}$ | β_{NPN} | β_{PNP} |
|---------|--------------|--------------|---------------|---------------|
| 0.025 V | 72 V | 116 V | 179 | 232 |

5.1.2 Input Resistance and Current Mirror Estimation

As shown in Figure 11, the input resistance required by the differential amplifier can adequately define the I_{out} current, which is the Widlar output current I_{R2} (Assume no base current).

For differential amplifier with single ended output (with active load), the input resistance is defined as:

$$R_{in(Diff)} = 2 r_{be(PNP)} = \frac{\beta_0(PNP)}{20I_C} \quad (6)$$

The requirement of input impedance is greater than $100 \text{ k}\Omega$, rewrite equation (6) into inequality form:

$$100 \text{ k}\Omega \leq R_{in(Diff)} = \frac{\beta_0(PNP)}{20I_C} \quad (7)$$

And the output current I_{out} is approximate twice the emitter current of Q4:

$$2 I_{Q4(E)} \sim I_{out} \quad (8)$$

It can be seen from (7) and (8) that the I_{out} current is inversely proportional to the input impedance of the differential amplifier. After calculation, if the input impedance can meet the specification, I_C must be less than $116 \mu\text{A}$, and the I_{out} must less than $232 \mu\text{A}$.

The output current I_{out} can be calculated by the Widlar current mirror circuit which is:

$$I_{out} R_2 = \frac{1}{V_T} \ln(\frac{I_{ref}}{I_{out}}) = 25 \text{ mV} \cdot \ln(\frac{I_{ref}}{I_{out}}) \quad (9)$$

The I_{ref} of a simple mirror circuit needs to be assumed, considering that the total current cannot exceed 5 mA , since the mirror circuit has a mirror effect, it is assumed to the 1.5 mA . From the formula (9), the I_C is set to the $55 \mu\text{A}$ for higher input resistance. Therefore, the R_2 is nearly 593Ω .

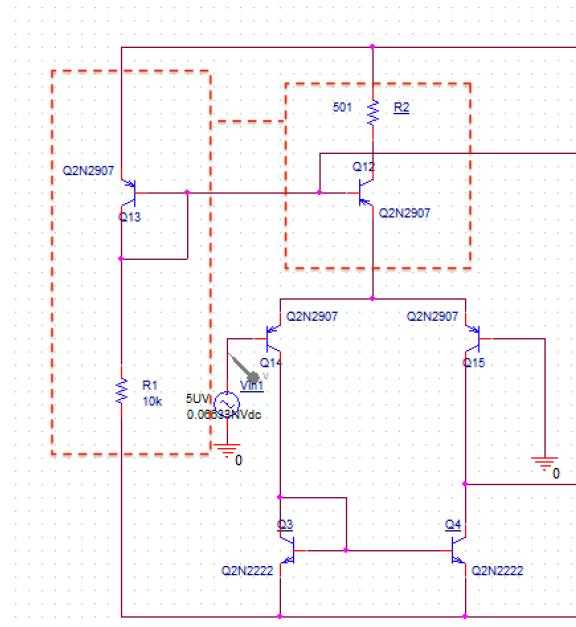


Figure 11. Calculate Differential Amplifier Output Current by Input Resistance

For the simple current mirror, the R_1 is based on the formula (10):

$$R_1 = \frac{V_{cc} - V_{ee} - V_{be(on)}}{I_{ref}} \quad (10)$$

Assume the $V_{be(on)}$ of Q13 is 0.6 V, the R_1 is 11.6 kΩ.

5.1.3 Emitter Follower Coupling and Differential Amplifier Estimation

Because emitter follower has a high input resistance, it is used in this experiment as a circuit connecting between the differential amplifier and common emitter. Since the voltage gain of the differential amplifier circuit is defined as follows:

$$A_{V(Diff)} = g_m \cdot AC\ Load \quad (11)$$

As shown in Figure 12:

$$AC\ Load = R_{ce(Q15)} // R_{ce(Q4)} // R_{in(Emitter\ Follower)} \quad (12)$$

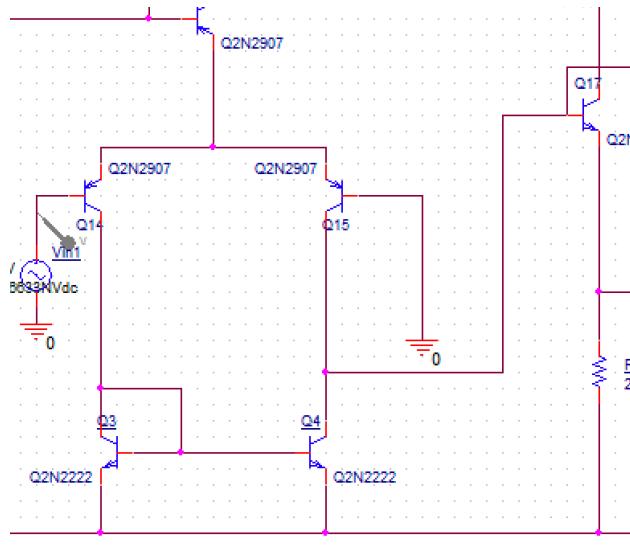


Figure 12. Voltage Gain of Differential Amplifier Calculation

It can be concluded from equation (12) that the input resistance of the emitter follower directly affects the voltage gain of the differential amplifier.

Based on experience, it is required that:

$$R_{in(CC)} \sim 10 (R_{ce(Q15)} // R_{ce(Q4)}) \quad (13)$$

After calculation, it can be concluded that the resistance of $R_{ce(Q15)} // R_{ce(Q4)}$ is about 800 kΩ. According to equation (13), the input resistance of emitter follower can be obtained to the 8 MΩ. Therefore, when the input resistance of the next stage of the differential amplifier is much higher than the load resistance of the differential amplifier itself, the voltage gain can be reduced to:

$$A_{V(Diff)} = \frac{1}{V_T} \frac{V_{An} V_{Ap}}{V_{An} + V_{Ap}} \quad (14)$$

As shown in Figure 13, the resistance R_4 can be calculated by the input resistance of emitter follower:

$$8 \text{ M}\Omega = R_{in(CC)} = r_{be(CC)} + (\beta + 1) (R_E // r_{be(CE)}) \quad (15)$$

The size of R_4 ($(R_E(CE))$) is calculated as 1 MΩ. It is found that the regulation of R_4 directly affects the output voltage close to 0V. In order to meet the requirement, the voltage gain of the differential amplifier can be appropriately discarded.

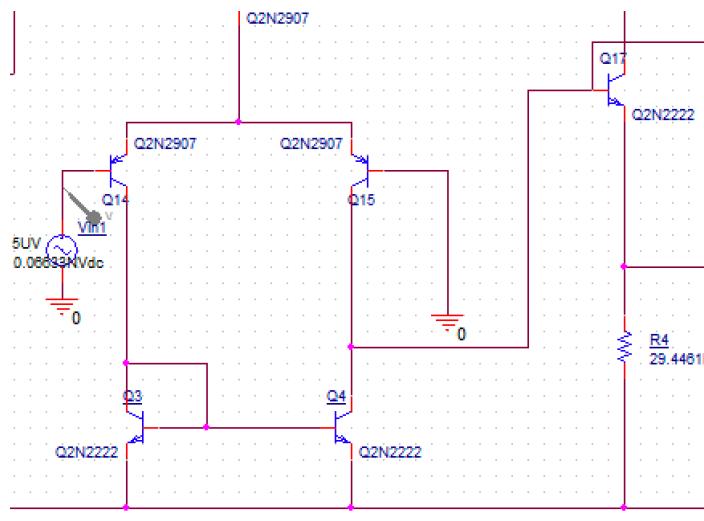


Figure 13. The R4 Approximation and Trade-offs

In the experiment, R_4 takes $30\text{ k}\Omega$, and the voltage gain of the compromised differential amplifier is approximately 900 by the formulas (11) and (12).

5.1.4 Voltage Gain Estimation

The voltage gain of the differential amplifier obtained from the previous section is about 900. Since the total voltage gain required in the requirement list is more significant than 500K, the voltage gain of the CE circuit can be calculated as follows:

$$A_{V(CE)} > \frac{500k}{A_{V(Diff)}} \sim 555 \quad (16)$$

As shown in Figure 14, the voltage gain of the common emitter amplifier depends on the input impedance of the output stage of the emitter follower. The formula (17) shows the relationship between the voltage gain and input impedance:

$$A_{V(CE)} = -g_m \cdot AC\ Load \quad (17)$$

$$AC\ Load = R_{ce(Q16)} // R_{ce(Q9)} // R_{in(Emitter\ Follower\ of\ Q10)} \quad (18)$$

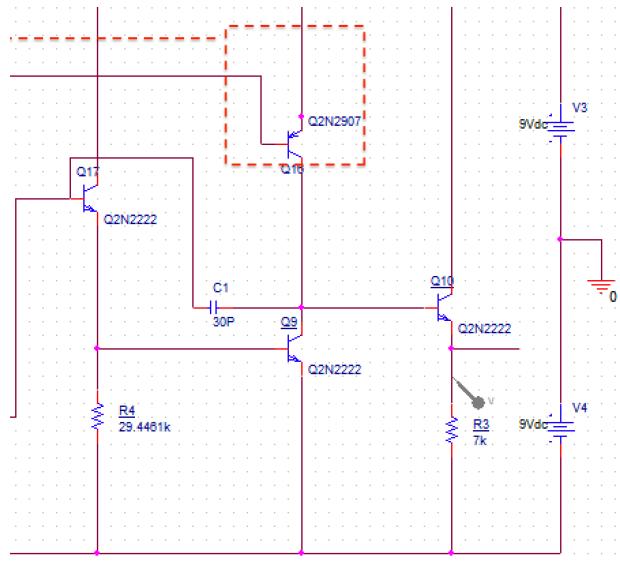


Figure 14. The Voltage Gain of Common Emitter Estimation

However, it can be concluded from equations (17) and (18) that if the input resistance of the emitter follower is much higher than the load resistance of the common emitter, the voltage gain of the common emitter tends to the theoretical value which is:

$$A_{V(CE)MAX} = \frac{1}{V_T} \frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}} \sim 1770 \quad (19)$$

5.1.5 Output Resistance Estimation

The output impedance of Op-Amplifier can be approximated as follows (R_S is the output resistance of common emitter and differential amplifier):

$$R_{out} = (\frac{r_{be}+R_S}{1+\beta_0})//R_E \sim (\frac{r_{be}+R_S}{\beta_0})//R_E \quad (20)$$

In the experiment, it was assuming the R_E is 7 kΩ, the output resistance is about 400 Ω. The selection of R_E depends on the output voltage close to 0 V, and the result of 7 kΩ which is obtained after adjusting the resistance several times.

5.1.6 Resistance Selection Summary

Four resistors need to be adjusted in this experiment. After theoretical and practical adjustment, the results are as follows in Table 2:

Table 2. Experimental Resistance Selection

| R_1 | R_2 | R_3 | R_4 |
|-------|-------|-------|------------|
| 10 kΩ | 501 Ω | 7 kΩ | 29.4461 kΩ |

Both R3 and R4 should be larger, but because of the need to compromise some of the voltage gains and the requirement that the output voltage is 0 V, the resistance value will be reduced. Ideally, R3 and R4 are more appropriate levels around 100 kΩ, and the reference current should be smaller, so R1 should be more significant.

5.2 Materials and Methods

5.2.1 VTC of Op-Amplifier Experiment Method (Task 2 to 4)

In the experiment part II, task-2 to 4 required to draw the voltage transfer curve to observe the characteristic curve of Op-Amplifier, from which the amplitude range of the input signal and the overall voltage gain of the amplifier circuit can be observed. Besides, the output of the circuit can be close to 0V by adjusting the DC offset in the VTC.

First, as shown in Figure 11, the input of one end of the differential amplifier as VDC was set, and the input signal of the other end is directly grounded. Then use DC sweep from -9 to 9 V. Finally, voltage electron probe was added to the output end, then the simulator started to measure the output curve. The DC sweep needs to be narrow in the useful range in which the range was set to the $-20 \mu V$ and $20 \mu V$, which is shown in Figure 12.

For Task 3, the open-loop gain is the slope of the curve in the effective amplification range. The derivative function D() of PSPICE was used in the experiment to calculate the tangent slope.

For Task 4, by using the VTC, the offset is the difference between the original point and the intersection of the curve to the X-axis.

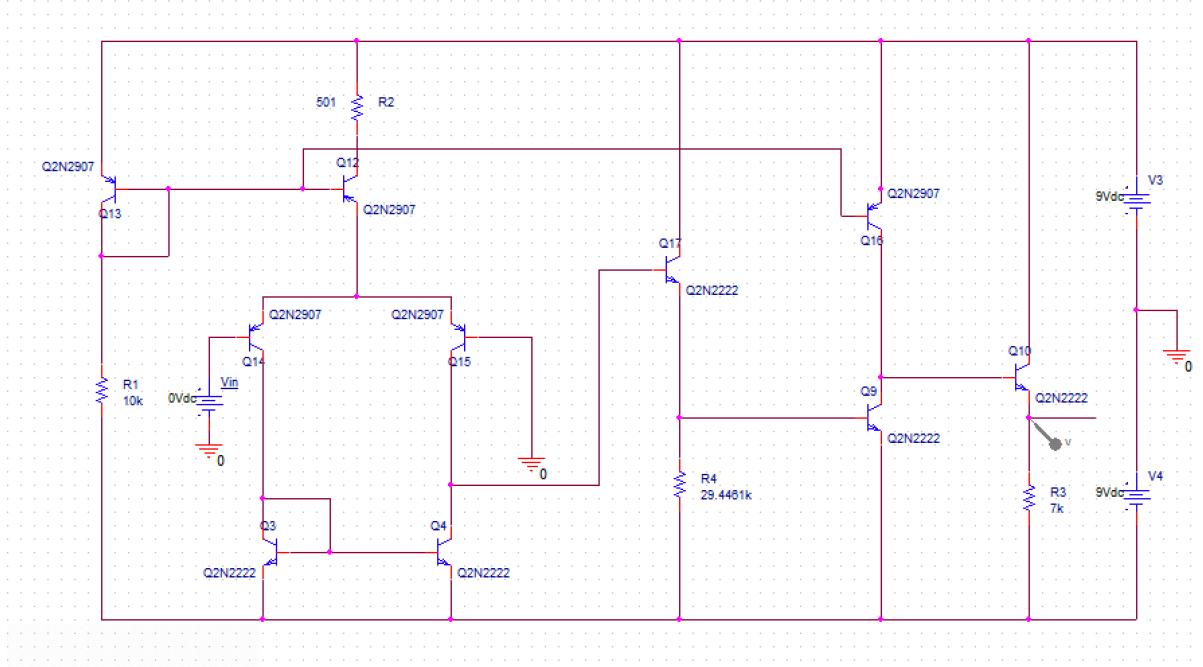


Figure 11. Measuring VTC Circuit Configuration

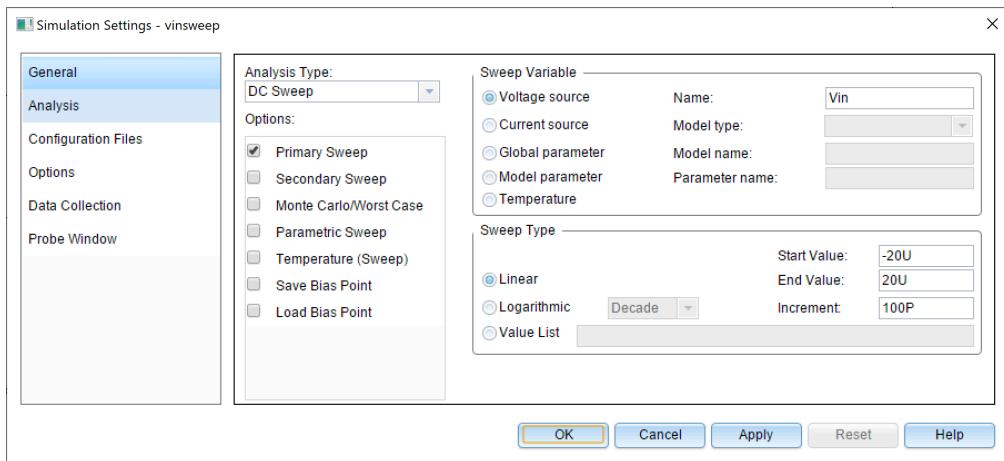


Figure 12. DC Sweep Settings in the Useful Range

5.2.2 Experiment Method of Transient Simulation (Task 5)

In this part, the sinusoidal signal is input within the allowable range of a small signal, and instantaneous simulation is used. The correctness of voltage gain obtained by the VTC curve is verified by comparing the voltage gain of the output signal and input signal. Table 3 shows the VSIN input source configuration data in Part II Task 5.

Table 3. VSIN Input Source Configuration Data in Part II Task 5

| VOFF | VAMPL | FREQ | AC |
|------|-----------|------|-----------|
| 0 V | $4 \mu V$ | 1 Hz | $4 \mu V$ |

As shown in Figure 13 and Figure 14, the circuit configuration and simulator configuration are used to simulate the process of small-signal input and amplification from a single end of the differential amplifier. The maximum allowable signal range of the op-amp is checked by changing the amplitude of the small signal.

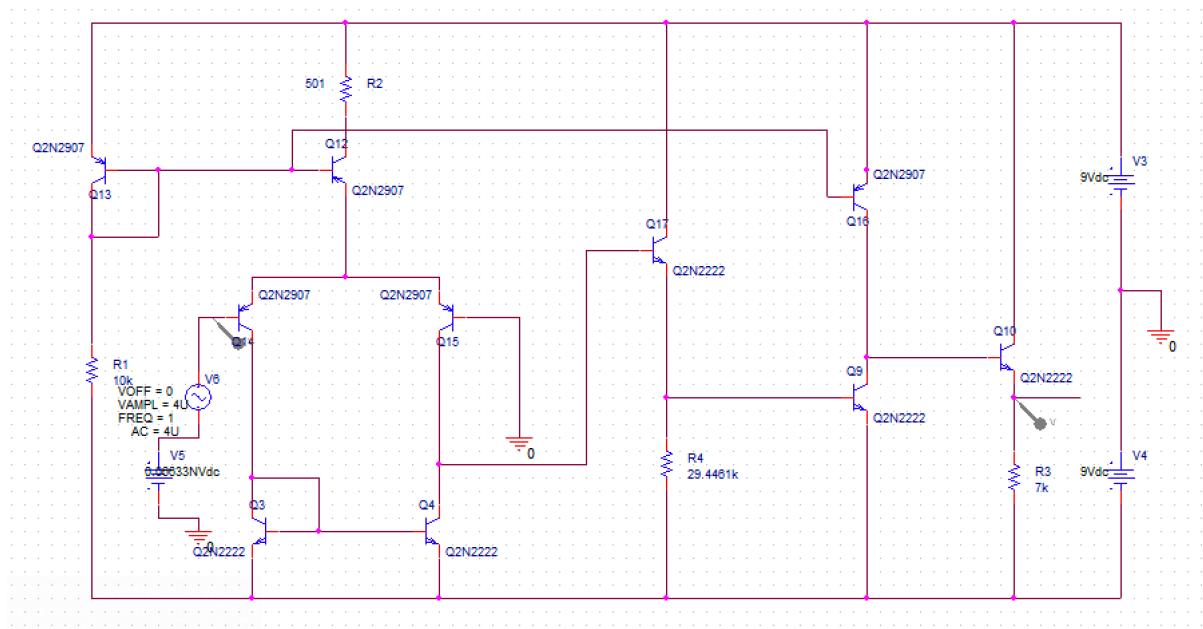


Figure 13. Configuration Circuit in Task 5 (Transient Simulation)

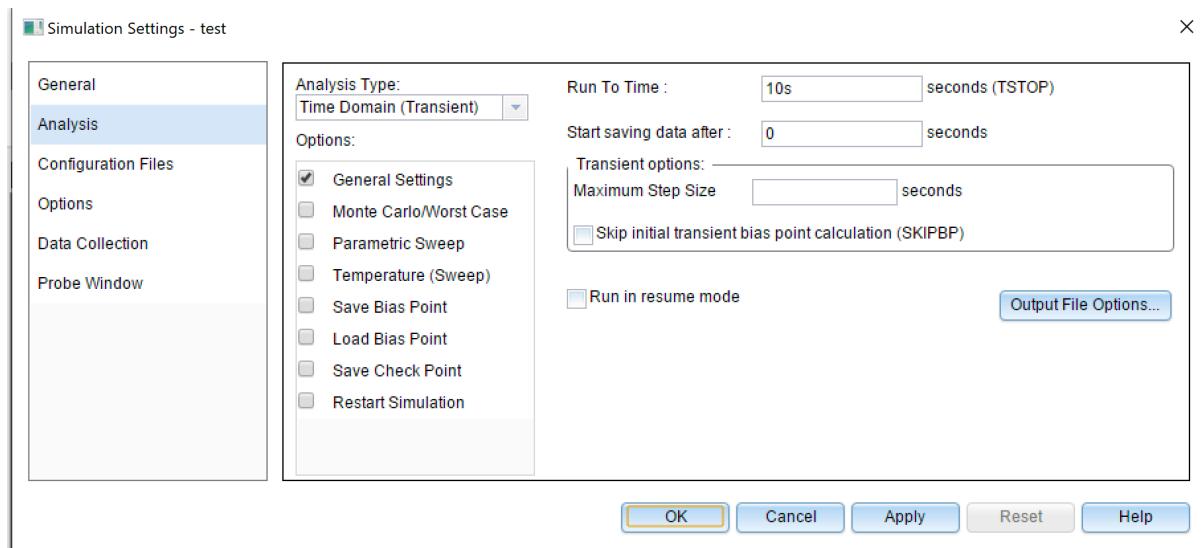


Figure 14. Transient Simulation Configuration Table Setup

5.2.3 Experiment Method of Input and Output Impedance in Op-Amplifier (Task 6)

As shown in Figure 15, the input resistance is measured using a single input small signal and a ground connection at the other input. The change of the input resistance is analyzed using AC sweep with voltage and current probes.

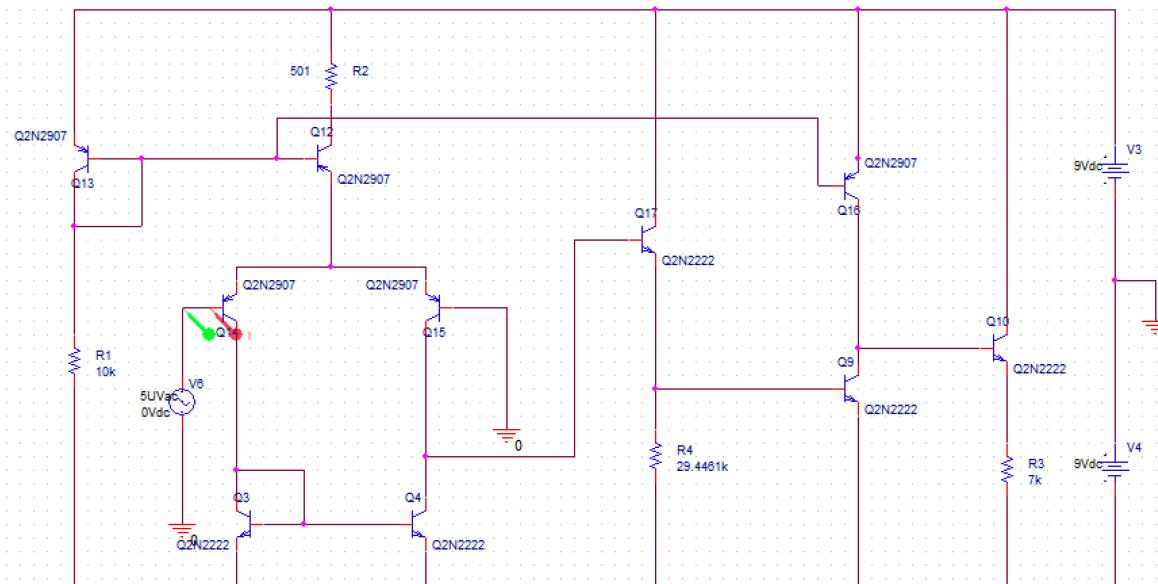


Figure 15. Input Impedance Measurement

According to the Figure 16, by deleting all input AC signals and adding a small AC signal source at the output position and adding voltage and current probes at the output port, the AC sweep image is drawn. Also, the AC sweep configuration of input impedance and output impedance is shown in Figure 17.

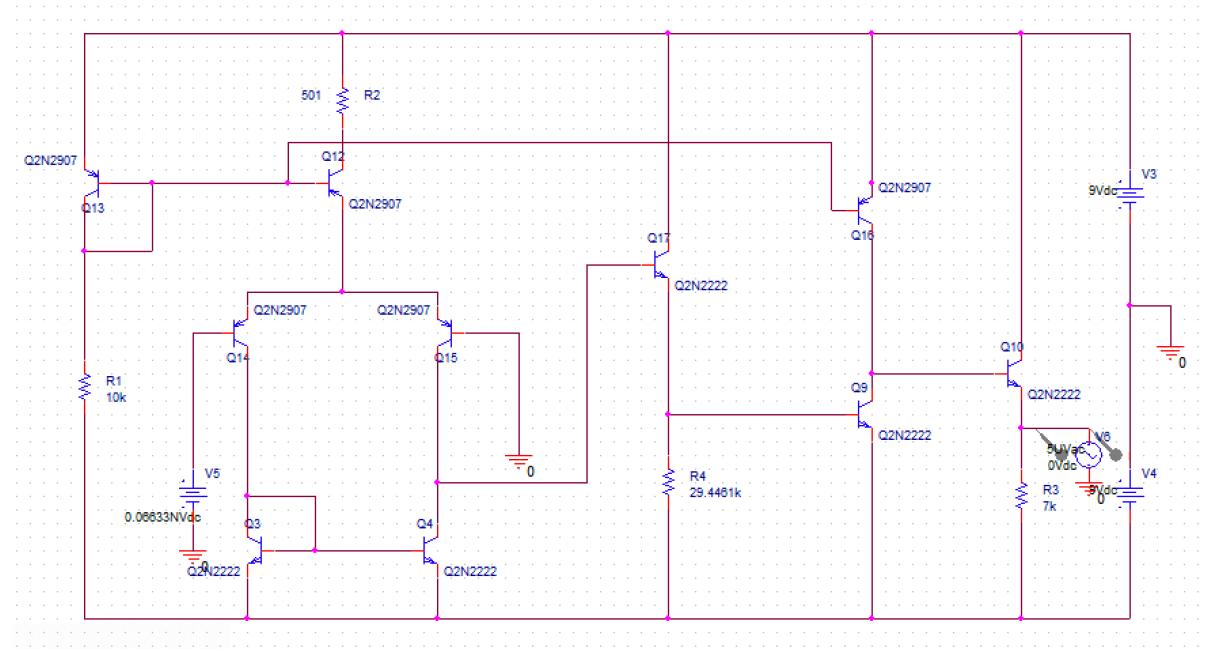


Figure 16. Output Impedance Measurement

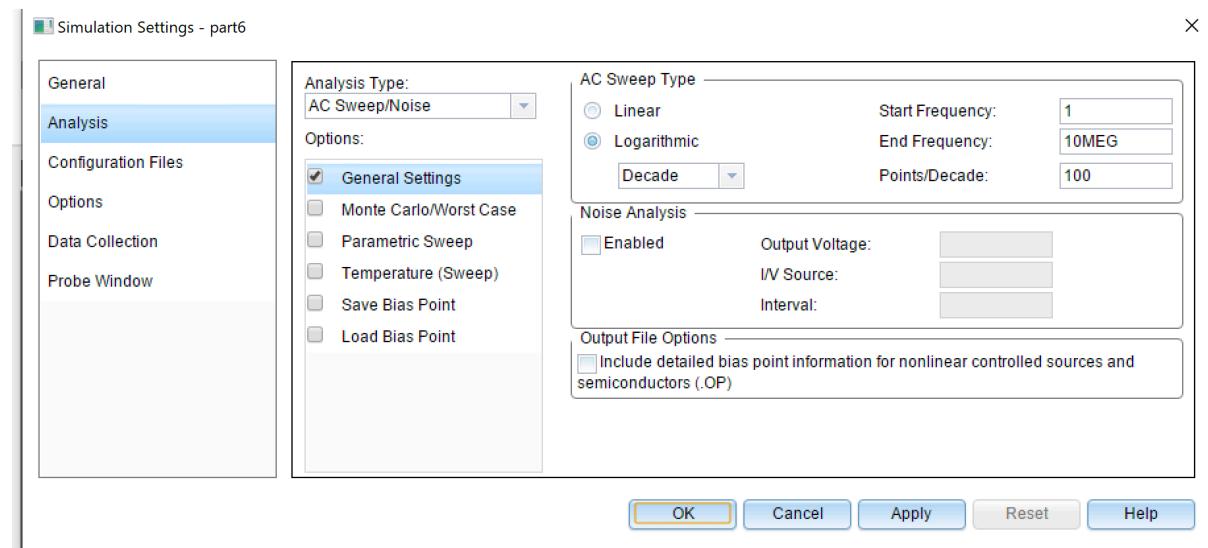


Figure 17. AC Sweep Configuration

5.3 Results

5.3.1 VTC of Op-Amplifier Result (Task 2 - 4)

The DC offset is set to the 0.06633 nV, and an effective range of small signal and open-loop voltage gain is obtained by using VTC. Figure 18 shows the DC sweep from -9 V to +9 V. The effective range of the small-signal can be roughly obtained from Figure 18. However, due to the low scanning accuracy, the obtained value cannot be trusted in Figure 18.

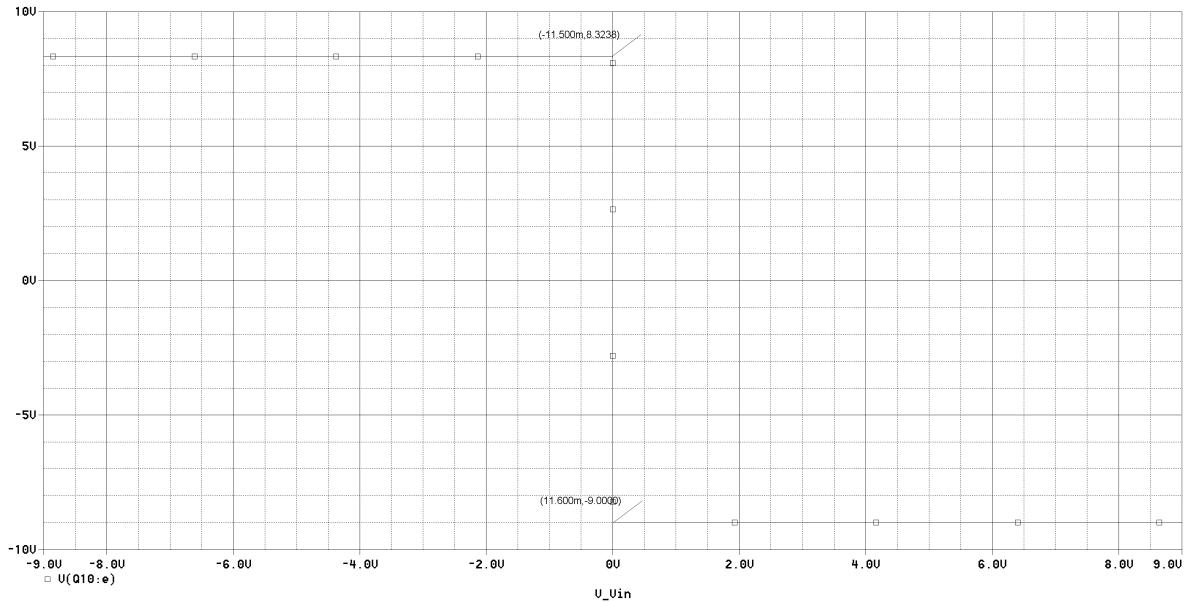


Figure 18. DC Sweep From -9 V to +9 V

A smaller scan range will be attempted below. Figure 19 shows the DC sweep range from $-200 \mu V$ to $200 \mu V$. The effective range of small signals from the figure is from $-9.23 \mu V$ to $10.77 \mu V$. Voltage gain can be obtained by calculating the tangent slope, which is:

$$A_V = \frac{8.1848 - (-8.7220)}{(-9.2308 - 10.773)10^{-6}} \sim 845179 \quad (21)$$

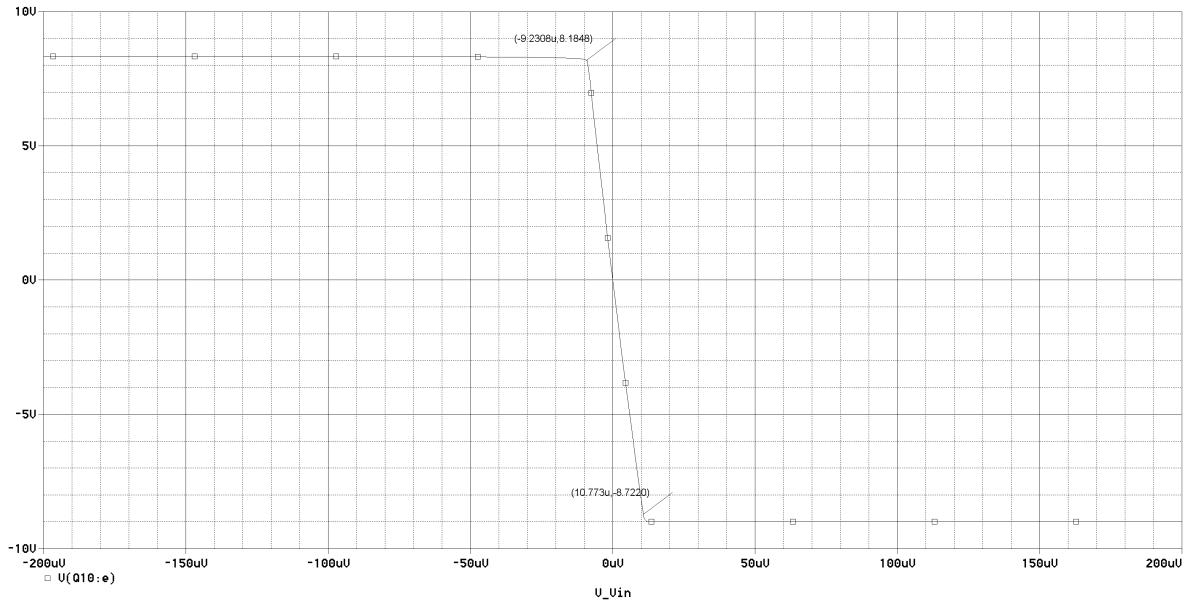


Figure 19. DC Sweep From $-200 \mu V$ to $200 \mu V$

From Figure 20, continue to reduce DC sweep from $-20 \mu V$ to $20 \mu V$, the effective range of small signal from the figure is from $-8.717 \mu V$ to $11.54 \mu V$. Voltage gain can be obtained by calculating the tangent slope, which is:

$$A_V = \frac{8.0975 - (-8.9666)}{(-8.717 - 11.54)10^{-6}} \sim 859668 \quad (21)$$

Because of the error in marking the turning point of VTC, there is a specific error in the range of a small signal, which is one of the reasons for the possible asymmetry of image.

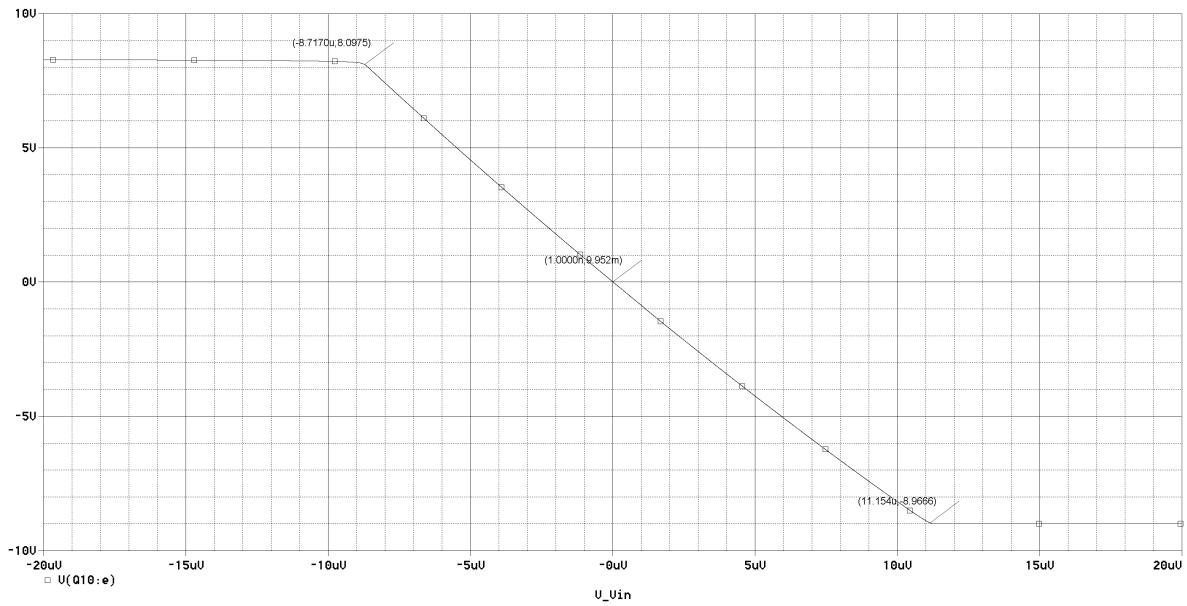


Figure 20. DC Sweep From $-20 \mu V$ to $20 \mu V$

5.3.2 Transient Simulation (Task 5)

The real signal amplification process is simulated by inputting a small signal by using the transient simulation. When the amplitude of the input signal is $5 \mu V$, the image is as shown in Figure 21. The output peak voltage is 4.5136 V. It can be concluded that the voltage gain is 902720 when the input signal frequency is 1 Hz.

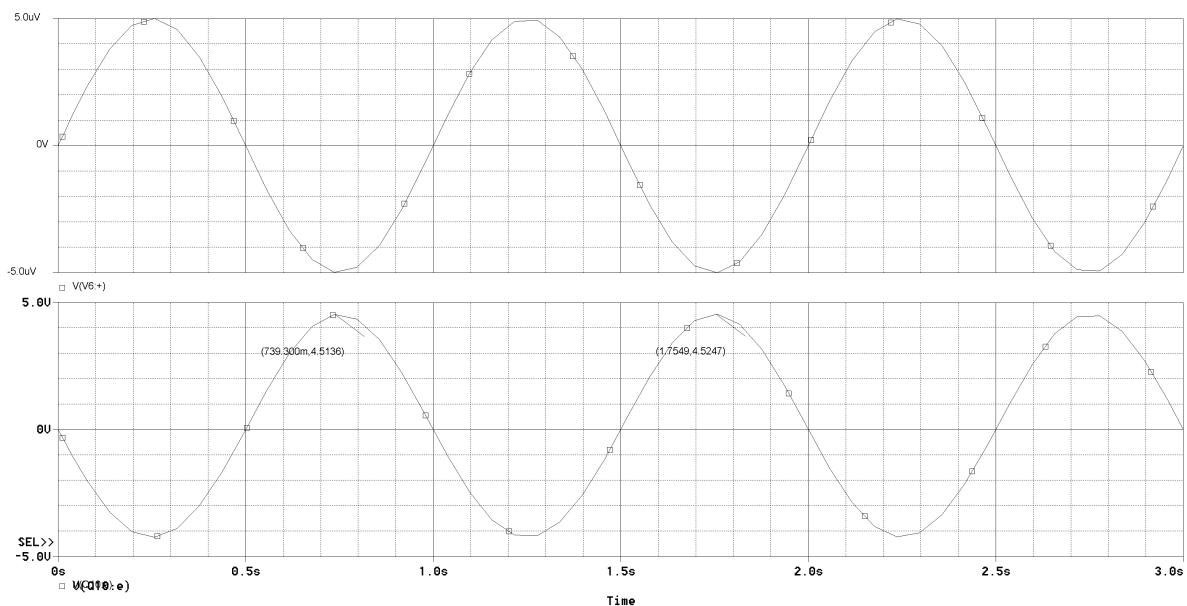


Figure 21. Transient Simulation in $5 \mu V$

As shown in Figure 22, when the amplitude of the input signal is $4 \mu V$. The output peak voltage is 3.6 V. It can be concluded that the voltage gain is 900000 when the input signal frequency is 1 Hz.

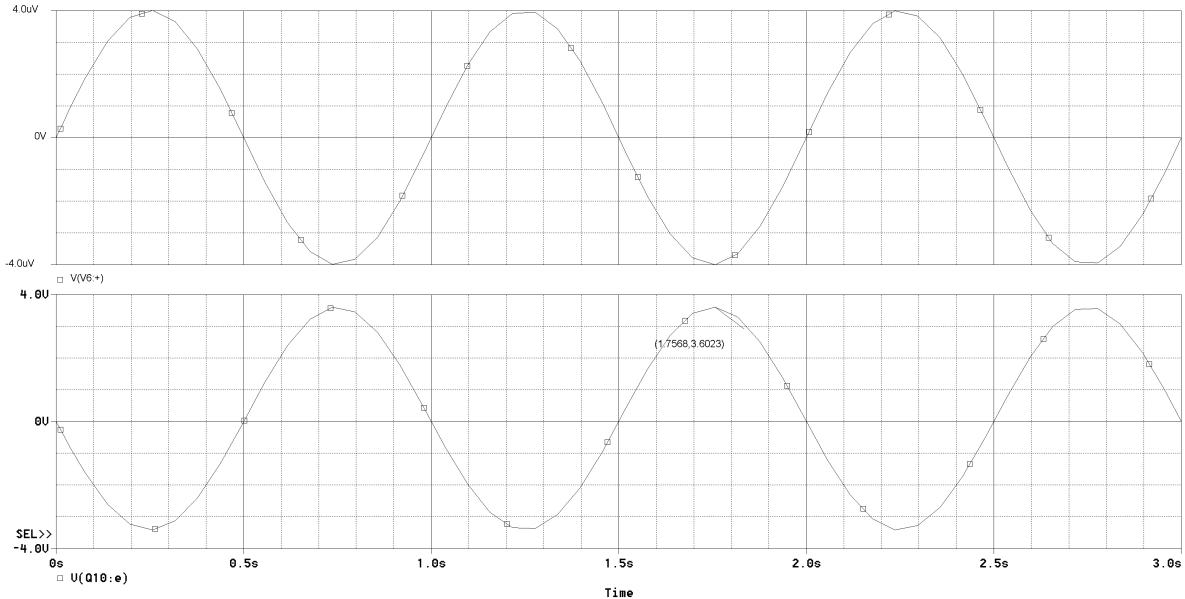


Figure 22. Transient Simulation in $4 \mu V$

In Figure 23, when the amplitude of the input signal is $3 \mu V$. The output peak voltage is 2.64 V. It can be concluded that the voltage gain is 880000 when the input signal frequency is 1 Hz. Through the above experiments, the requirement of voltage gain has been realized.

5.3.3 Input and Output Impedance in Op-Amplifier (Task 6)

The input resistance of the Op-Amplifier circuit is shown in Figure 23. It can be obtained from the diagram that the input impedance is about 241k ohms at low frequencies. When the frequency rises to 30kHz, the input resistance increases further and decreases when it reaches the maximum value.

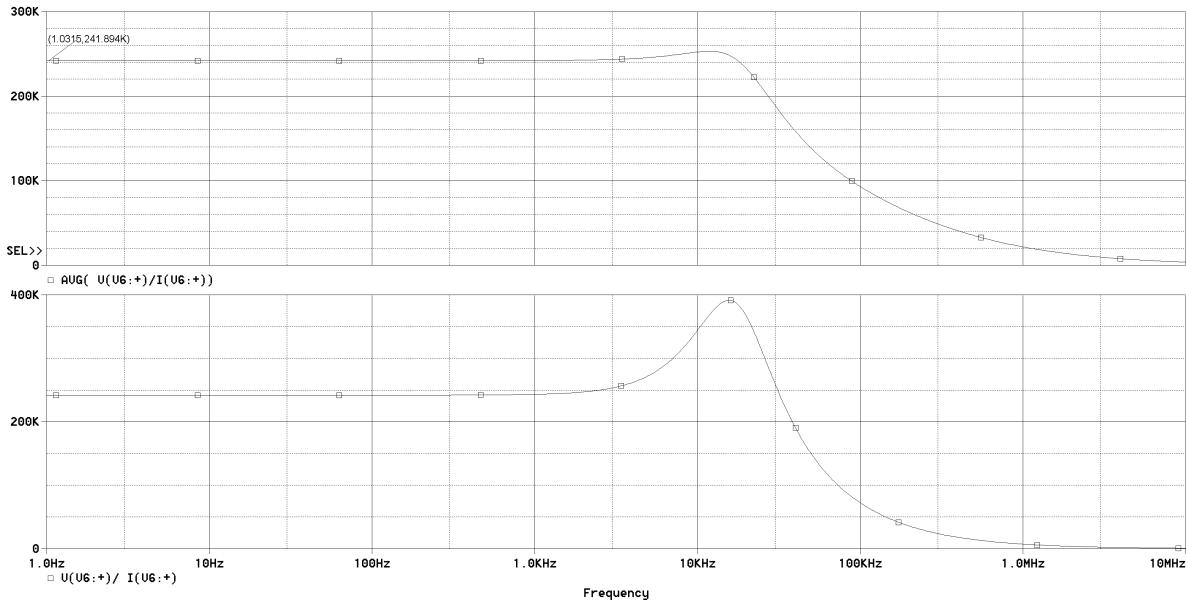


Figure 23. Op-Amplifier Input Resistance and Average Input Resistance

Figure 24 shows the output impedance and the average output impedance of the Op-Amplifier. It can be seen from the figure that in the range of DC to 5KHz, the output resistance is about 166 ohms, and then the output resistance decreases rapidly. At the frequency of 1MHz, the output resistance is about 23 ohms.

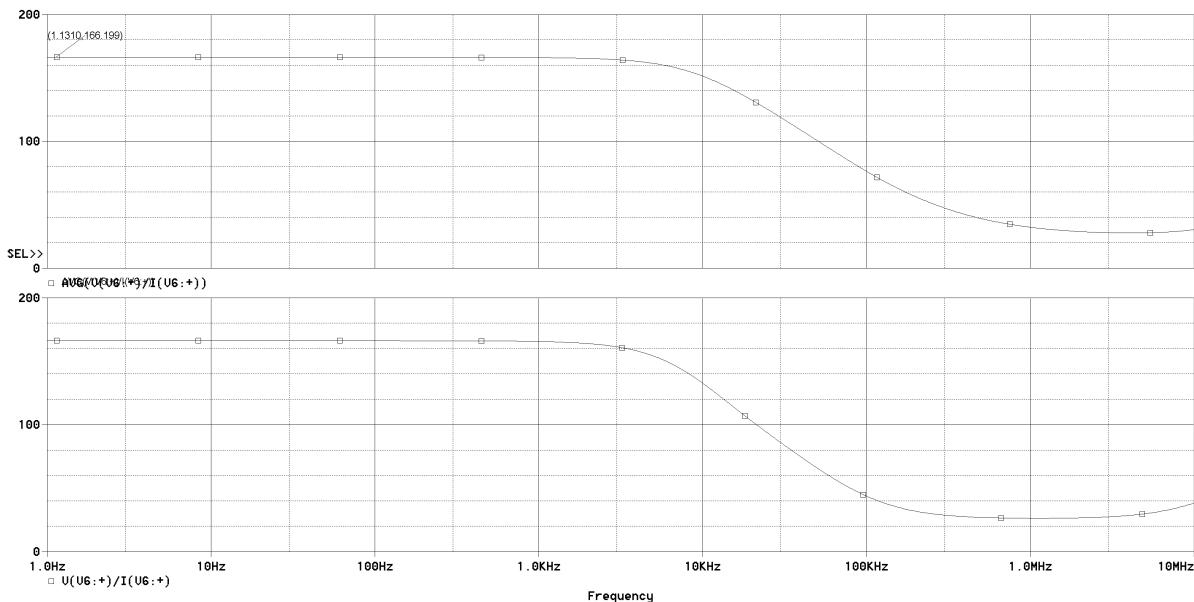


Figure 23. Op-Amplifier Output Resistance and Average Output Resistance

5.3.4 Op-Amplifier DC Level (Task 7)

Figure 24 shows the currents and voltages on the schematic, it can be seen from the figure that the current of simple mirror circuit is slightly higher, but the overall current output is less than 5mA, and the output voltage is close to 0V.

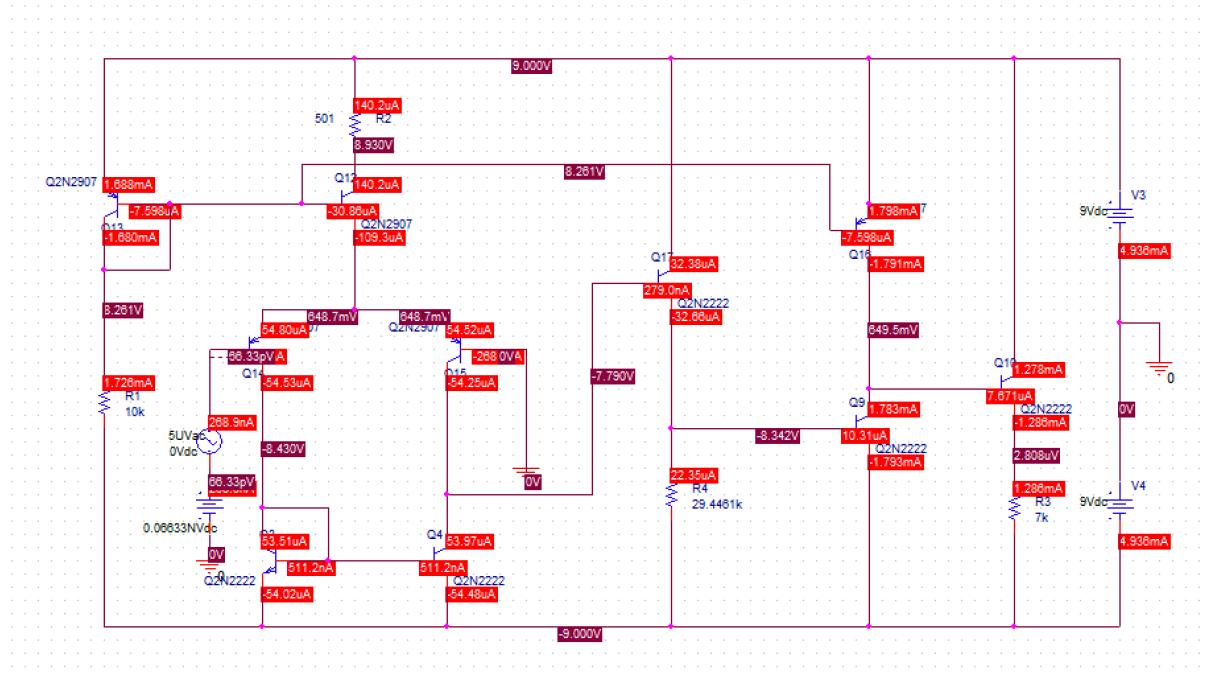


Figure 24. Currents and Voltages on the Schematic

5.4 Discussion and Explanation

5.4.1 Open Loop Voltage Gain

- Theoretical value analysis

If the output resistance of the next stage of the differential amplifier and the common-emitter is much higher than the load resistance, then this Op-Amplifier is called the theoretical maximum voltage gain. The maximum theoretical voltage gain in this experiment is defined as follows:

$$A_{VMAX} = \frac{1}{V_T} \frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}} \cdot \frac{1}{V_T} \frac{V_{An}V_{Ap}}{V_{An}+V_{Ap}} \sim 1770 \cdot 1770 \sim 3132900 \quad (22)$$

- Experimental voltage gain analysis

However, due to other requirements, there is a compromise on the voltage gain in this experiment. The first compromise is that the emitter resistance R4 of the matched differential amplifier's emitter follower is relatively sensitive to the output voltage. During the experiment, if there is a small change in the resistance, the output voltage will change relatively large. It is proved that R4 cannot reach the theoretical value. The above causes the voltage gain of the differential amplifier to be different from the theoretical value. Finally, the test results show that the voltage gain of the Op-Amplifier almost reaches 859668. The actual voltage gain of the following experiment is compared with the theoretically estimated voltage gain.

From the formula (11) and (12):

$$A_{V(Diff)} = g_m \cdot AC\ Load \sim 900 \quad (23)$$

From the formula (17):

$$A_{V(CE)} = -g_m \cdot AC\ Load \sim -850 \quad (24)$$

Total voltage gain:

$$|A_V| = A_{V(Diff)} A_{V(CE)} \sim 765000 \quad (25)$$

The main reasons for the difference between the estimated and experimental values are as follows:

- The input resistance of Q10 is not much higher than the load, so the voltage gain is not expected to be high
- In order to achieve the output voltage close to 0 V, the resistance calculated by the theoretical value is adjusted
- The voltage gain measured by the experiment also has the experimental error of manual marking

5.4.2 Input and Output Impedance

Based on the formula (7), the input resistance calculated theoretically is $210 \text{ k}\Omega$ in the low frequency. The input resistance measured by the experiment is about $241 \text{ k}\Omega$. This is a relatively approximate estimate, but there are still errors. The main reasons are as follows:

- Errors in the current estimation of mirror circuit
- Current exists at the base of transistor
- Errors in the experimental measurement of input resistance

For the formula (20), the output resistance calculated theoretically is 400Ω . However, the actual measurement results are 166Ω under the low-frequency condition. There is a significant difference between the experimental and measured values, but both meet the requirements. The main reasons are as follows:

- R_s calculation of formula (20) is incomplete
- Measurement error

For high-frequency response, the reason why the input resistance and output resistance decrease substantially is that under high frequency, the traditional small-signal model is not applicable, and the original open circuit R_{bc} will become short-circuit. Excessive discussion of high frequency in this Op-Amplifier makes no sense, because for such amplifiers, feedback circuits are used to make compromises between gain and bandwidth.

5.4.3 DC Level Evaluation

- Current Evaluation

For the simple current mirror I_{ref} , the initial value of the current value setting is high, mainly because the total current does not exceed 5 mA, after evaluation, the I_{ref} can be set to the 1 mA. Besides, the current of the final output stage is set too high, which results in smaller input resistance of the common collector and a low

voltage gain of the common emitter. For the Widlar current mirror, the current is appropriate because the input resistance meets the requirement.

- Resistance Evaluation

The R3 and R4 settings are too small, but due to other requirements, appropriate compromises need to be made. Resistance sizing is a complex task, because some functions may have maxima in a small range, and when one requirement is found to be met, there is a great chance that other requirements will be affected.

- Voltage Evaluation

After constant adjustment of the resistance, the output voltage is close to 0 V, which meets the requirements. Requiring R3 to have a 9 V voltage is difficult for the following reasons: First, this requires the transistor Q10 (CC) to operate within a reasonable range and the output voltage of 0 V, which means that the voltage at the collector of Q9 (CE) is about $V_{be(on)}$. Second, because the resistance value R3 is uncertain, it is challenging to preset the current through emitter follower.

6 Obtaining the Frequency Response of Design Amplifier

6.1 Theoretical Calculation

6.1.1 Phase Margin and Stability of System

As shown in Figure 25, the transfer function of Op-Amplifier G(s). The system was initially an open-loop system in this experiment since the circuit will use a closed-loop system in the future to provide feedback and improve the stability of the system [4].

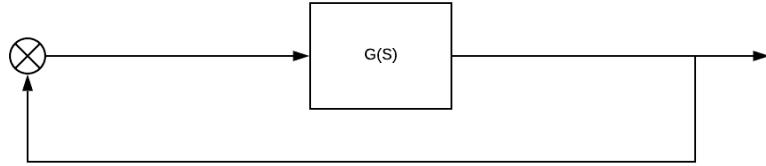


Figure 25. Closed-Loop System of Op-Amplifier

In Figure 26, the transfer function can be treated to the $\frac{G(S)}{1+G(S)}$, if the gain of this closed-loop system is ∞ . It means when the denominator is zero, the $G(S)$ equal to the minus one.



Figure 26. Equivalent Diagram of Closed Loop System of Op-Amplifier

When the $G(S)$ equal to the minus one, the system turns to the unstable [4]. In terms of phase and voltage gain, it shows that:

$$G(S) = 1 \text{ or } 0 \text{ dB} \quad (26)$$

$$\text{phase} = -180^\circ \quad (27)$$

For example, the transfer function which is defined by:

$$G(S) = \frac{1.3(s+2)}{(s+0.1707)(s^2+0.8293s+5.858)} \quad (28)$$

As shown in Figure 27, using MATLAB, the bode function can analyze the stability of the system. The phase margin is defined as the frequency at which the gain intersects 0 dB is in phase with the length of the segment at -180 degrees [4].

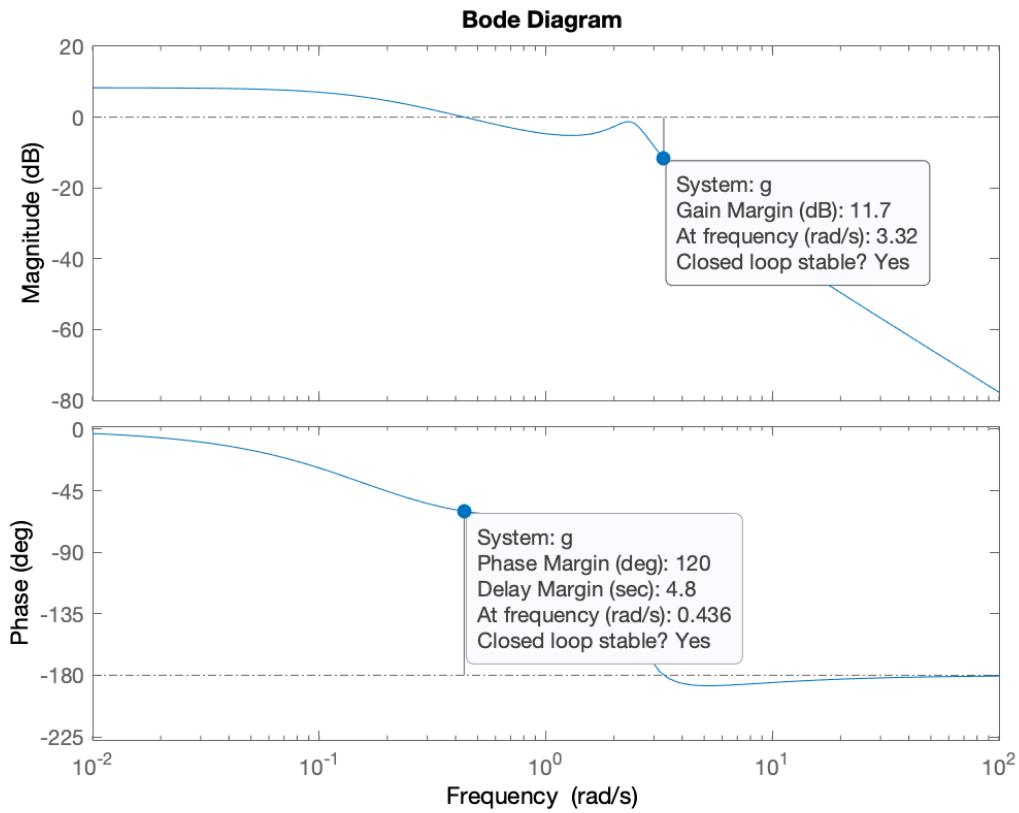


Figure 27. Bode Plot Analysis Stability of System (taken from [5])

6.2 Materials and Methods

6.2.1 Frequency Response of Op-Amplifier

As shown in Figure 28, the differential gain and phase difference of the Op-Amplifier are measured. The VAC in the small-signal range is used for signal input at both input ends, and two voltage probes are used for measurement. During the measurement, the difference between the two input signals is taken, and the signal voltage is measured at the output simultaneously.

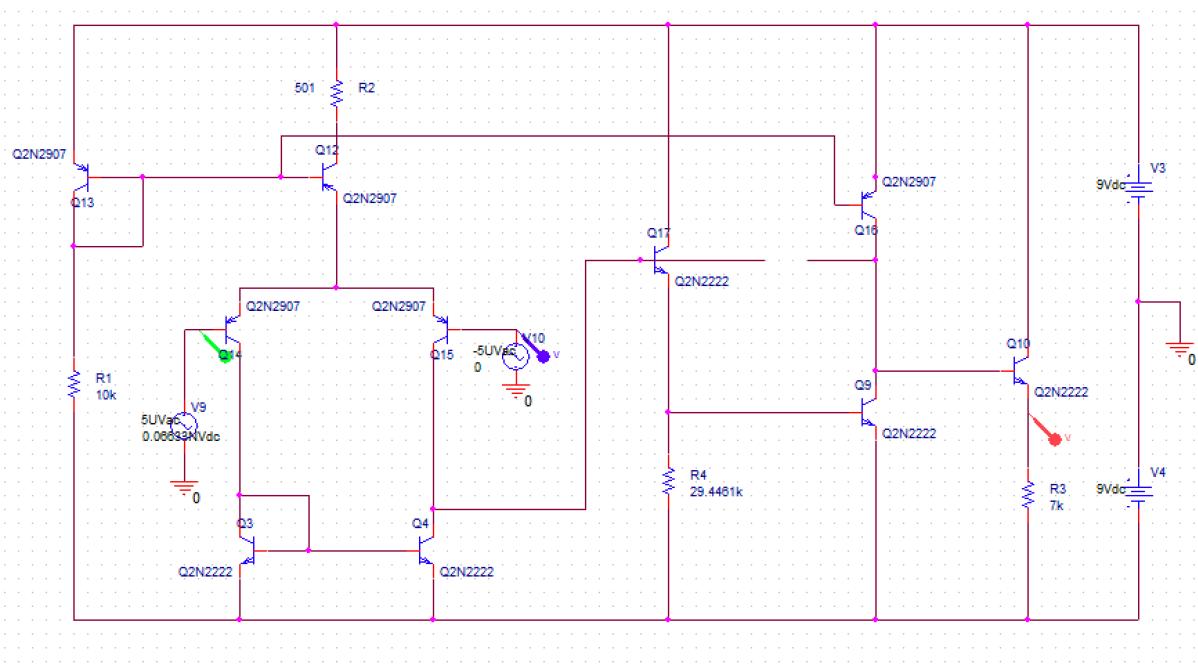


Figure 28. Differential Gain in Frequency Analysis by Bode Plot

Then the plot window templates in PSpice are used to print the bode plot (See in Figure 29).

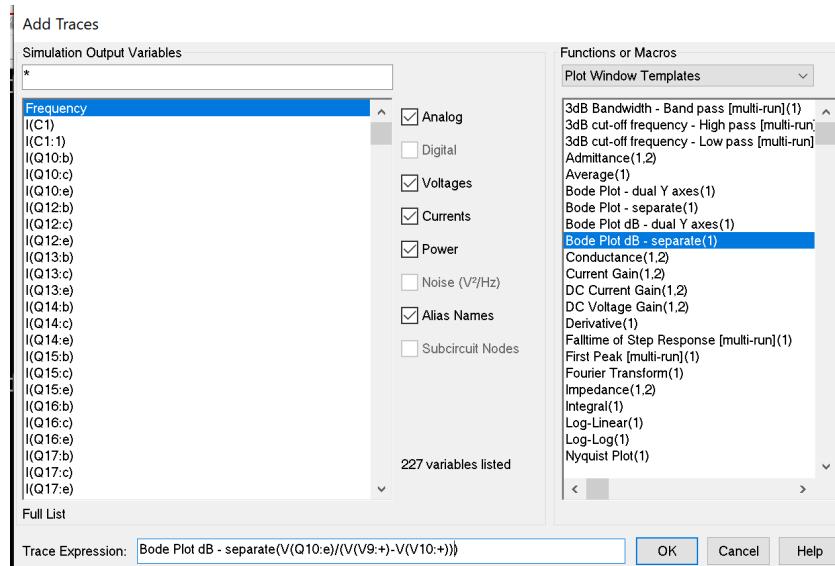


Figure 29. Bode Plot by PSpice

6.2.2 Frequency Response of Op-Amplifier with Phase Compensator

As shown in Figure 30, a phase compensator was added into the circuit, the Bode Plot is drawn with an initial value of 30 pF and then compared with the previous using a 40 pF capacitor.

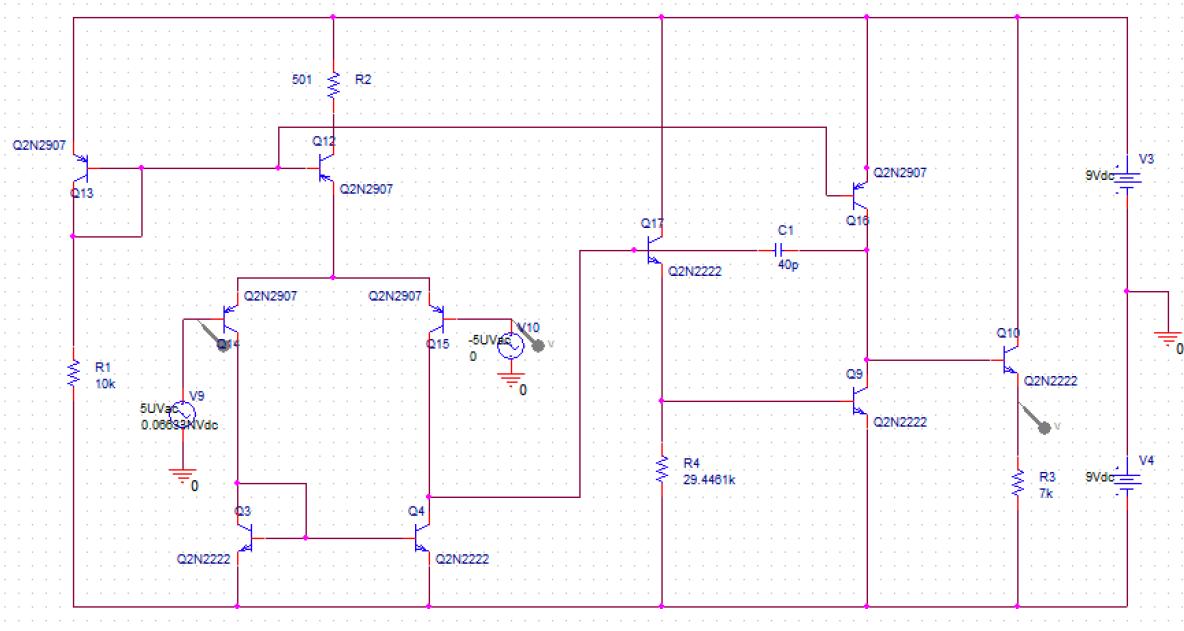


Figure 29. Circuit with Phase Compensator Capacitor

6.2.3 Frequency Response of Op-Amplifier in Common-Mode Signal

As shown in Figure 30, the common mode is no different from task 1 except that all input signals are synchronized. Besides, the input signal takes half of the two signals as the denominator.

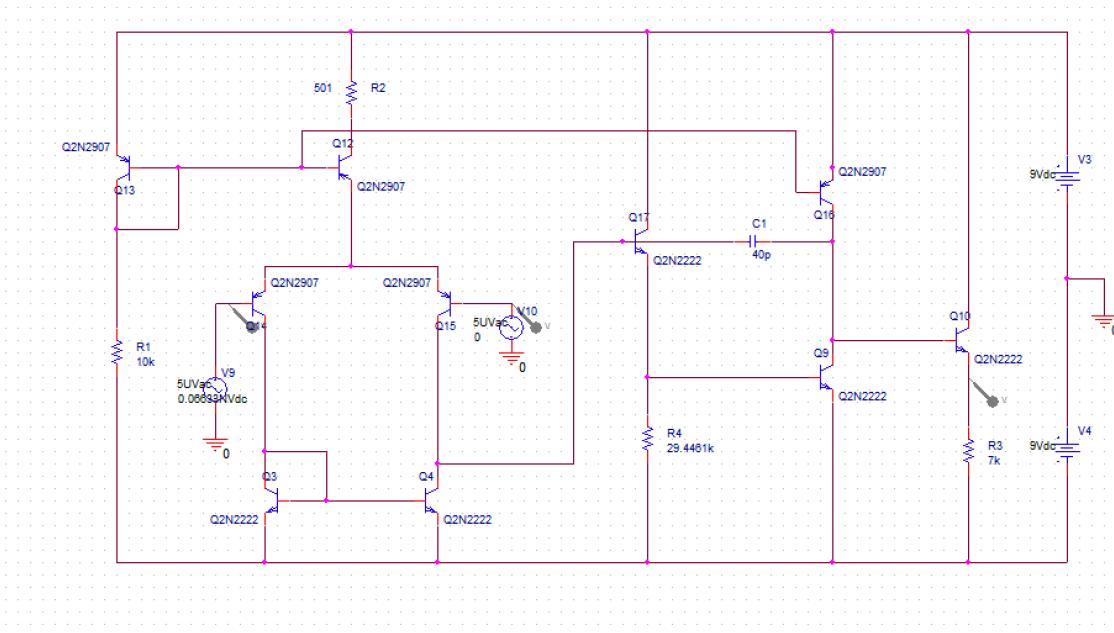


Figure 30. Circuit with Common Mode Signal

6.3 Results

6.2.1 Bode Plot of Op-Amplifier

In Figure 31, the 3dB point is at the frequency of 9.849 kHz, since the amplifier circuit can start at 0 Hz, it can obtain a stable voltage gain in the range of 0 to 9.849 kHz. Also, when the voltage gain is 0 dB, the frequency is 26.451 MHz.

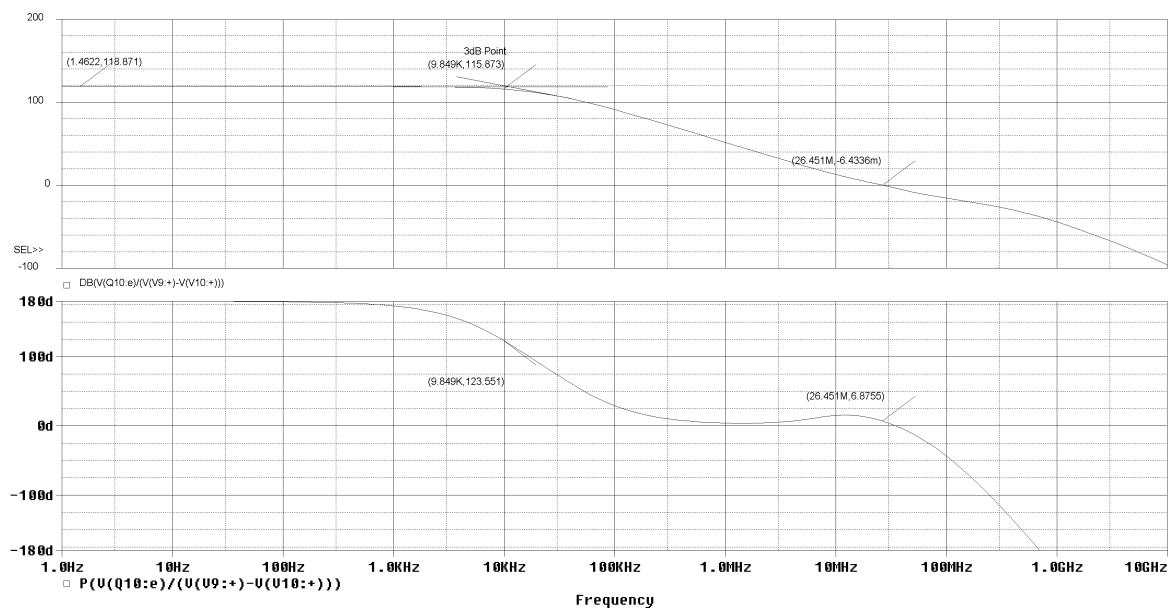


Figure 31. Bode Plot of Op-Amplifier without Phase Compensator

6.2.2 Bode Plot with Phase Compensator

Figure 32 shows the phase compensator capacitor of 10 pF, the corner frequency is 37.598 Hz, and when the voltage gain is 0 dB, the frequency is 12.627 MHz.

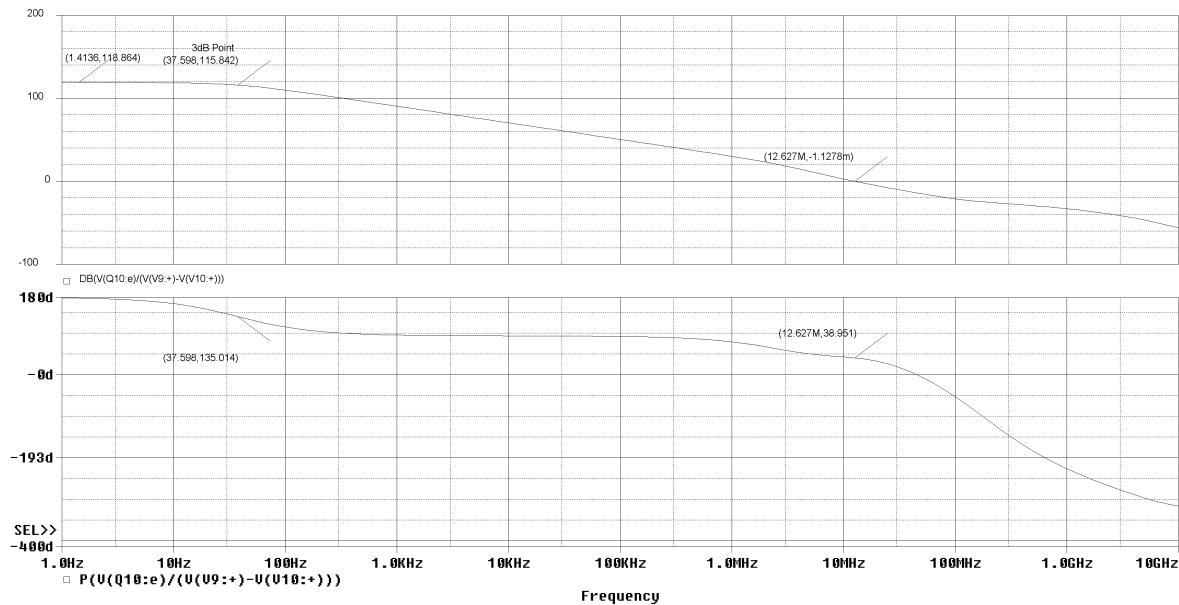


Figure 32. Bode Plot of Op-Amplifier with Phase Compensator of 10 pF

Figure 33 shows the phase compensator capacitor of 30 pF, the corner frequency is 12.723 Hz, and when the voltage gain is 0 dB, the frequency is 6.6847 MHz.

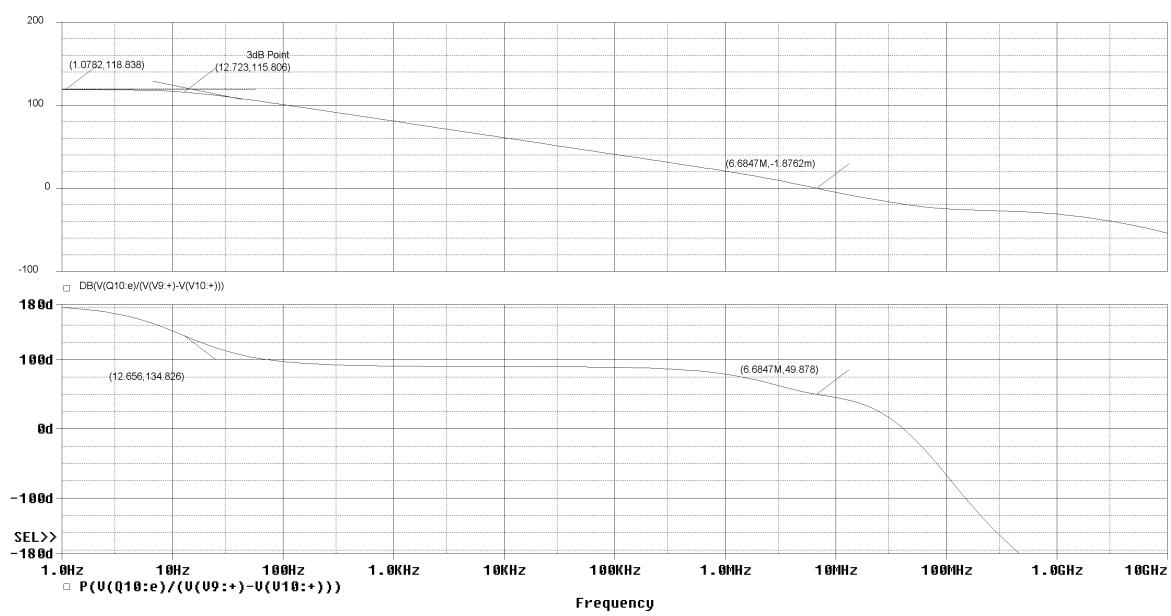


Figure 33. Bode Plot of Op-Amplifier with Phase Compensator of 30 pF

6.2.3 Frequency Response in Common-Mode Signal

The bode plot of the common-mode signal is shown in Figure 34. It can see from the diagram that the common-mode gain is small.

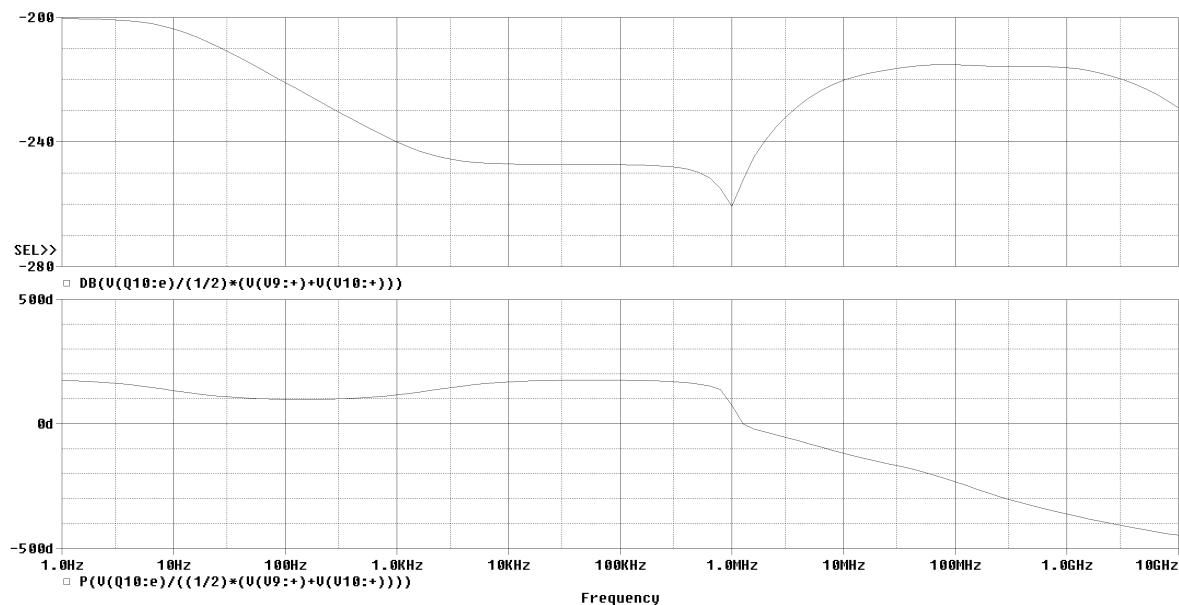


Figure 34. Bode Plot of Op-Amplifier in Common-Mode Signal

6.4 Discussion and Explanation

Problems with system stability and capacitive phase compensators are analyzed in detail in General Question in the next section.

7 The Design Specification Table

7.1 Table of Specification

| Parameter | Specification | Value |
|---------------------------------------|-------------------|--|
| Differential input impedance | > 100 k | 241.894 k (DC) |
| Open-loop voltage gain | > 500,000 | 859668 (Typical) |
| Output impedance | < 1 k | 167 Ω (DC) |
| DC output voltage | \sim 0 V | 2.8 μ V |
| DC offset voltage | None given | 0.06 nV |
| Frequency response | Down to DC (0 Hz) | Down to DC |
| Total current consumption | < 5 mA | 4.936 mA |
| Bandwidth with compensation capacitor | None given | 37.598 Hz (10 pF) 12.723 Hz (30 pF) |

7.2 Comment of Specification Table

- Differential input impedance

The differential input impedance parameter is about twice as large as the requirement, which is not surprising since the differential impedance is the first step in the current design of the entire system. From the formula (7), the R_2 is set to the 593 Ω in the first design, which causes the input resistance to meet the requirements.

- Open-loop voltage gain

The open-loop gain met the requirements, but this parameter was not satisfactory.

After the preliminary report was completed, a new design produced an open-loop gain of around 1200k. The main reason for the new design is that the voltage gain of the differential amplifier is significantly increased. Compared with the design mentioned in the report, the reason for the low open-loop voltage gain is that the input impedance of emitter followers after the differential amplifier is small, resulting in a low gain of the whole system. Besides, the voltage gain of the common emitter is also affected by the input impedance of the emitter follower on the output side.

- Output impedance

From the formula (20), the output impedance meets the requirements, which brings the Op-Amplifier properties closer to the theory.

- DC output voltage

The output voltage is a value close to 0 V after much adjustment. It is challenging to adjust the DC voltage output, because when the output voltage is adjusted to 0V, other parameters may not meet the requirements.

- DC offset voltage

The DC offset voltage is minimal, by using the VTC, the DC offset can be seen that the distance between the intersection of the image and the x-axis and the origin is measured.

- Frequency response

From the bode plot, it can be concluded that Op-Amplifier can start from 0 Hz to 3dB point. For this experiment, the bandwidth is 9.849 kHz, which is satisfactory. However, such experiments have drawbacks. Since AC analysis can only select a minimal AC parameter and DC analysis cannot be used, a small DC signal should

be added to observe the voltage gain of the system to prove the frequency response down to DC (0 Hz).

- Total current consumption

The total current consumption is 4.936 mA, which is close to the requirement. It is not a very good parameter. In practice, there may be a temperature change that causes the current to increase abnormally and damage other circuits. If the reference current of the mirror circuit is assumed to be smaller and the resistance parameters are appropriately changed, the total current cannot exceed 3 mA.

- Bandwidth with compensation capacitor

Since the compensation capacitance can reduce the bandwidth and improve the system stability, when the compensation capacitance is 10pF, the bandwidth is significantly reduced to about 38Hz, which can be compared to a low pass filter. However, specific bandwidth depends on specific requirements and actual use.

8 General Discussions and Conclusion

8.1 General Question

- a) What can you deduce about the stability of your amplifier from the Bode plots in Part III?

From section 7.1, formula (26) and (27), it shows that the phase margin is related to the system stability.

$$G(S) = 1 \text{ or } 0 \text{ dB} \quad (26)$$

$$\text{phase} = -180^\circ \quad (27)$$

Figure 35 shows the phase margin of the Op-Amplifier, it shows the phase margin Φ_M is 186.86 (Phase margin can be larger than 180). The above results show that the frequency response of the system is stable within 26.451 MHz, but it can be seen from the diagram that the phase will drop sharply after 26.341 MHz and reach negative 180 degrees when approaching 1GHz. Under some extreme conditions, the system may tend to be unstable. However, such an Op-Amplifier generally uses a lower frequency in the feedback circuit to obtain a more significant gain.

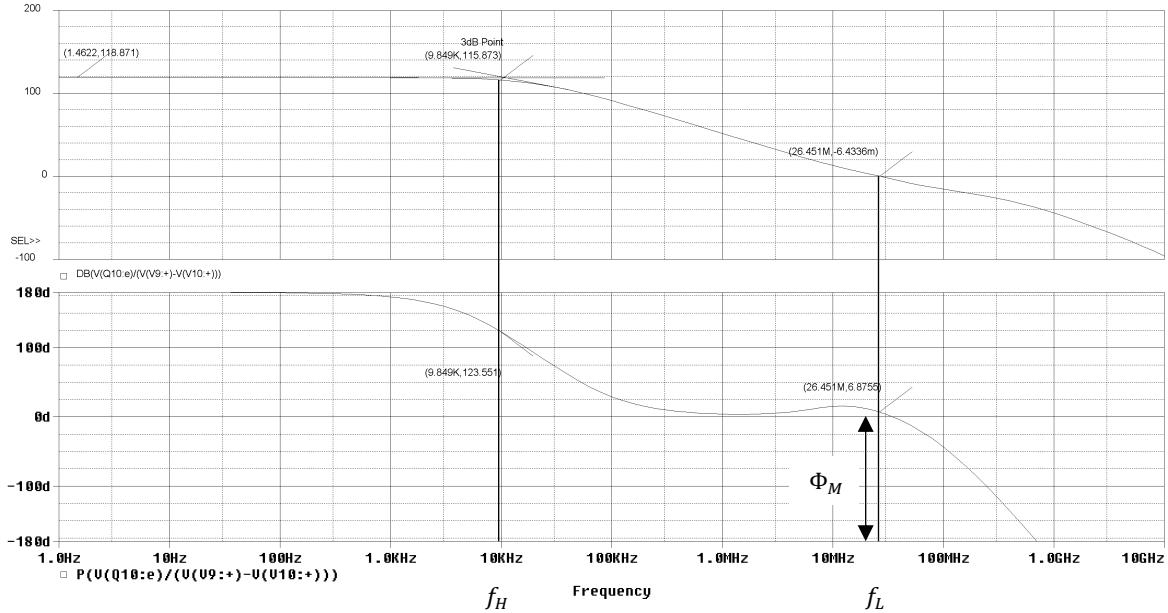


Figure 35. Phase Margin without Phase Compensating Capacitor

The phase margin after adding the 30 pF phase compensator is shown in Figure 36. The phase margin is increased to 230. The whole system is relatively more stable than before because the phase margin is relatively higher. Considering the whole system, since the frequency response calculated by the whole experiment is carried out under the computer simulation conditions, the transfer function of the amplifier may change under the actual conditions due

to the influence of temperature, humidity. These small changes may cause the amplifier to become unstable at the rated frequency. It is why phase margins reserve a certain height.

In many cases, a system appears to be very stable and may be unstable, as shown in Figure 36. The phase margin is relatively high. However, there is a local lowest point in the system. If there is a small change in the system, the whole system will tend to be unstable.

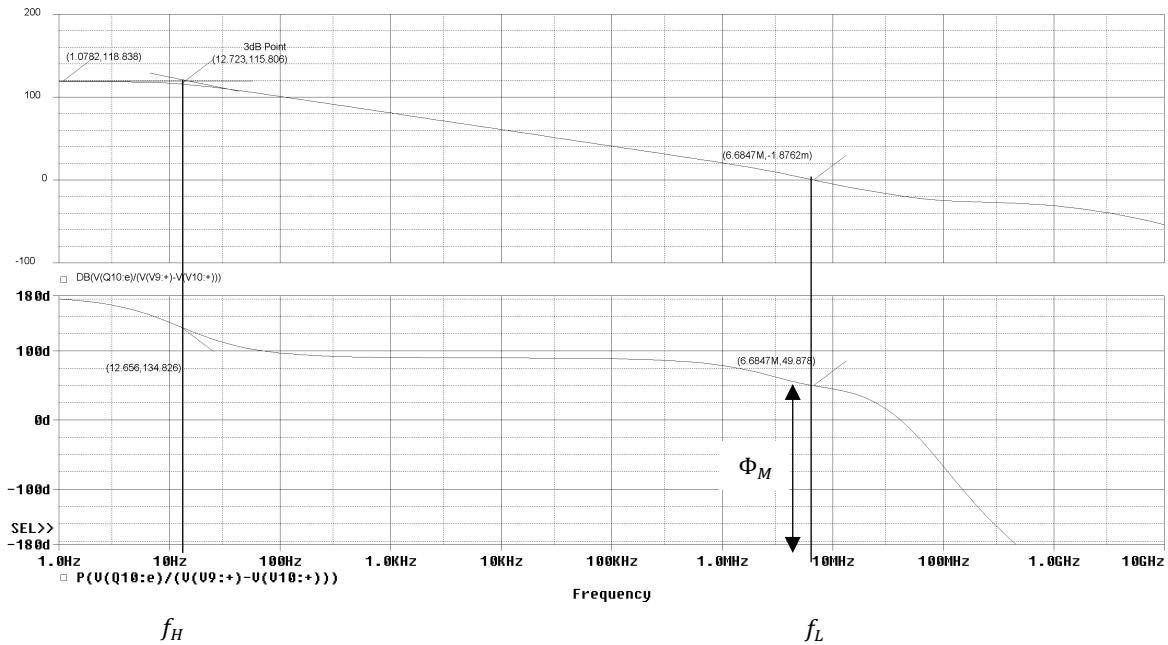


Figure 35. Phase Margin with Phase Compensating Capacitor in 30 pF

As a summary, the use of a 30pF phase compensator in this experiment can make the system relatively stable. However, due to the uncertainty of the real situation, it is dangerous that the system reaches -180 degrees at around 1GHz. The next section will summarize the function of the phase compensator by comparing the 10pF phase compensator with a 30pF phase compensator.

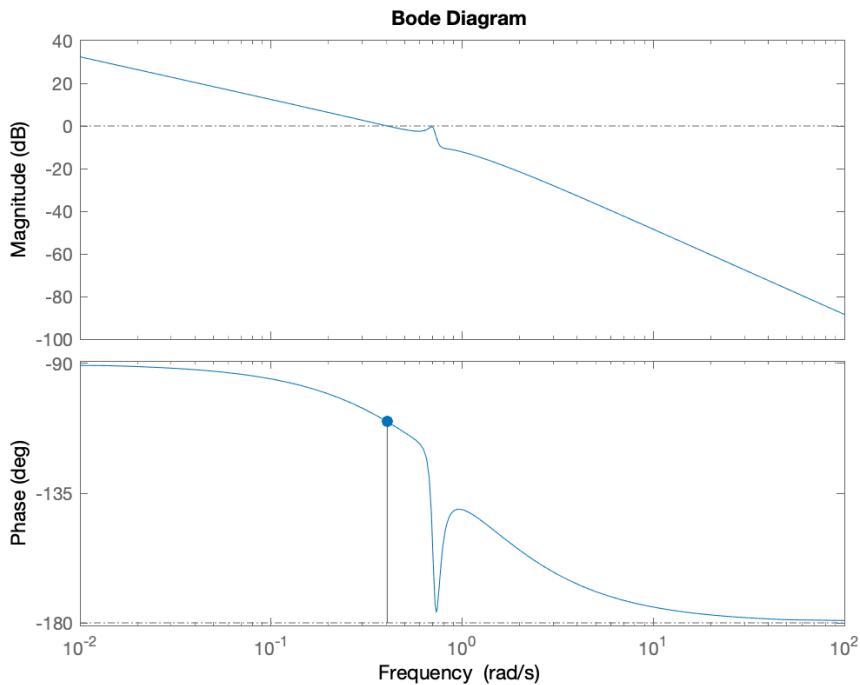


Figure 36. A System in Which Data Are Stable and May be Unstable (taken from [5])

b) What is the purpose of the 'Phase compensating capacitor'?

The function of phase compensating capacitor is to sacrifice the voltage gain bandwidth in exchange for a portion of system stability, that is, to reduce the cut-off frequency so that the system exhibits phase stability over a broad frequency range.

As shown in Figure 36, the comparison diagram with or without phase compensator. It can be seen quantitatively that with the increase of compensation capacitor, the bandwidth is smaller, but a certain phase margin is obtained at the cost of bandwidth. In other words, the larger the compensation capacitor is, the larger the phase margin is, and the smaller the bandwidth is.

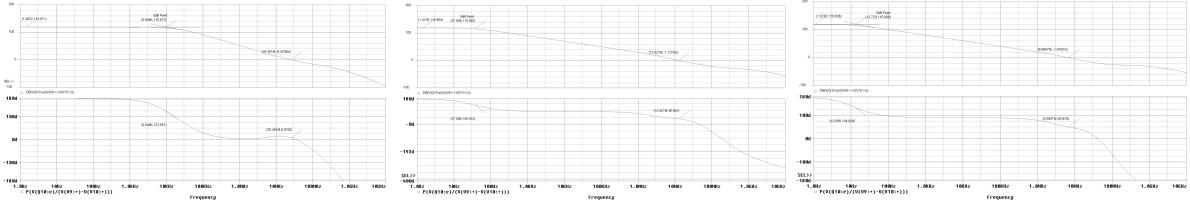


Figure 36. Bode Plot (without Compensating capacitance, 10 pF and 30 pF, left to right, Note the Bode Plot range of 10 pF is 180d to -400d)

In summary, the phase compensator increases the stability of the system by reducing the bandwidth. However, the phase compensator is limited because the bandwidth cannot be 0 in this type of Op-Amplifier. Otherwise, the system cannot provide a stable phase and gain.

8.2 Experiment Summary and Improvement

8.2.1 Objective Achievement

The fulfillment of project requirements is satisfactory. However, as mentioned in the design specification, the open-loop voltage gain is slightly lower than the theoretical analysis. Besides, the current of the entire circuit meets the requirements, but considering other practical factors, the total current is relatively high, which may lead to circuit damage under extreme conditions. For the circuit with phase compensator, the stability of the system is relatively increased. However, it cannot guarantee the instability of the system under extreme conditions, such as a sudden increase in frequency and temperature.

8.2.2 Problems and Improvement

There are some difficulties in this experiment. Firstly, it is difficult to control the output voltage close to 0V by only theoretical calculation and to change the resistance parameters. Secondly, much time has been spent on the theoretical basis of phase compensator. Besides, it is suggested that the experiment can be divided into two parts: the first part is dedicated to theoretical calculation, and the second part is used to PSpice simulation verification. Because some students directly simulate without theoretical calculation, a lot of time is wasted.

References

- [1] B. Hart, "Designing the Widlar current mirror," *International Journal of Electrical Engineering Education*, vol. 40, no. 4, pp. 285-298, 2003.
- [2] S. Hall, "Lecture Notes-Module ELEC 271 2020."
- [3] S. Hall, "Experiment 5_ Design of an Operational Amplifier Using PSpice."
- [4] N. S. Nice, "Control System Engineering," *Addison-Westley Publishing Company*, pp. 240-260, 1995.
- [5] B. Douglas, "Gain and Phase Margins Lecture Note."