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XI'AN JIAOTONG-LIVERPOOL UNIVERSITY

EEE112 Integrated Electronics and Design nMOS IC Design Project Report

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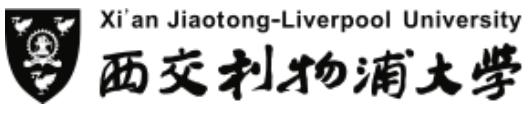
Friday, May 17, 2019



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1. Abstract

In this report, simple Integrated Circuit (IC) design will be shown. First, this circuit is a combination logic circuit, by using the simple logic transformIntroduction could know a simple integrated circuit is called OR gate in digital circuits. Then, the possible W/L is calculated by known resistance, and then implemented in IC design. In design, it is actually a problem of optimum solution. The size of MOS has been known. By avoiding the problem in design rules, the optimum design is obtained, that is, the minimum design area. By writing and learning this report, the students knows the semiconductor design and manufacturing process.

2. Main body

2.1 Fabrication Process Flow of nMOS ICs and Design Rules' description

2.1.1 Fabrication Process Flow of nMOS

The actual production process of MOS will be described below. Firstly, the resistance design of integrated circuit is considered. The whole resistance of MOS is shown in the Figure 1.

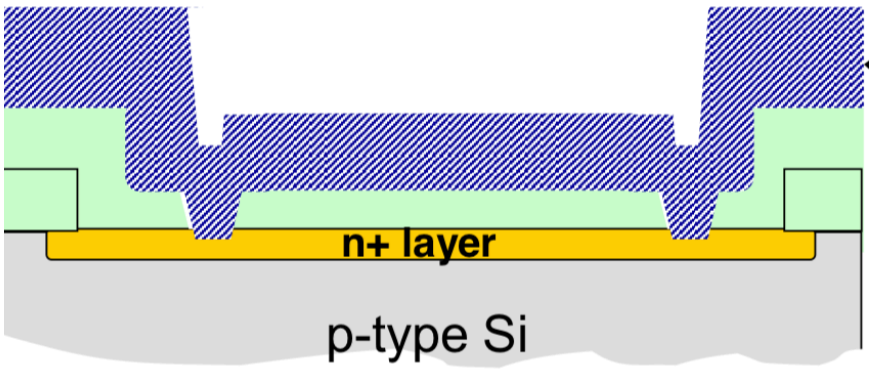

Figure 1: RESISTANCE OF MOS[1]

In the design, we use three parts of mask to make up the whole layout. The first part is oxide mask (Yellow part), second part is contact mask (Black part) and third is Al mask (Broken line part). In this design, we called oxide mask to the active region. The Figure 2 has shown the layout.

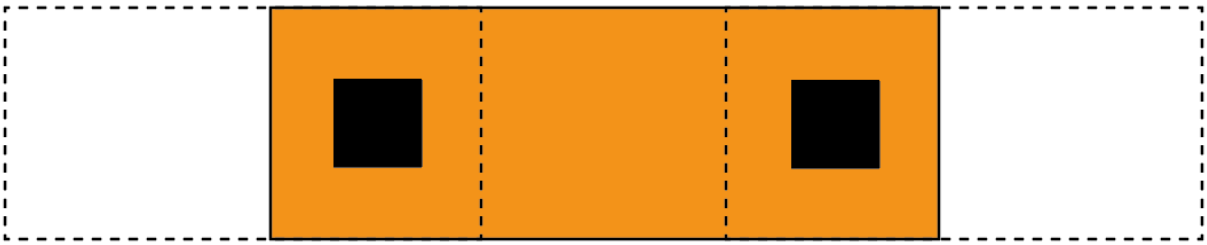

Figure 2: WHOLE LAYOUT OF RESISTANCE

The manufacturing process of the integrated resistor is as follows:

1. First, a layer of silicon dioxide is added on the basis of doped polysilicon, and then passed through the way of photoresist to let the whole structure is from Figure 3 to Figure 4.

Figure 3: STEP 1

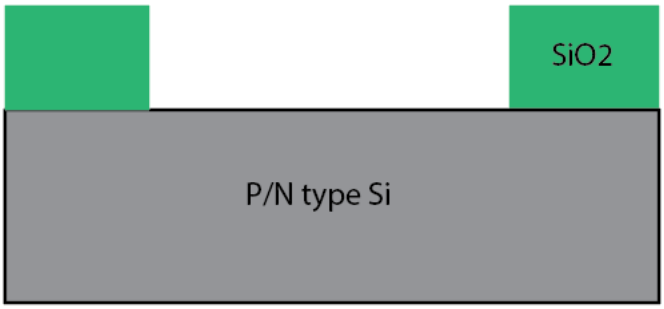

Figure 4: STEP 2

2. Then the method of particle shooting is mixed. It is shown in the Figure 5.

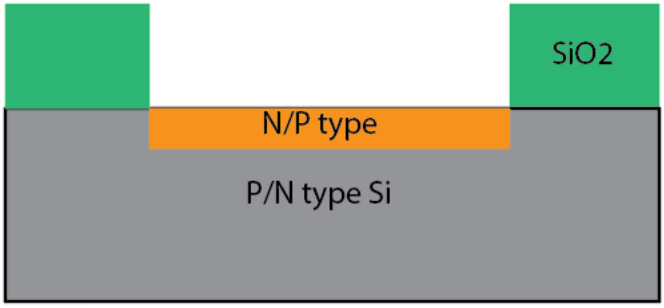

Figure 5: STEP 3

3. Fig. 6 is obtained by adding a layer of silica to this layer and etching it.

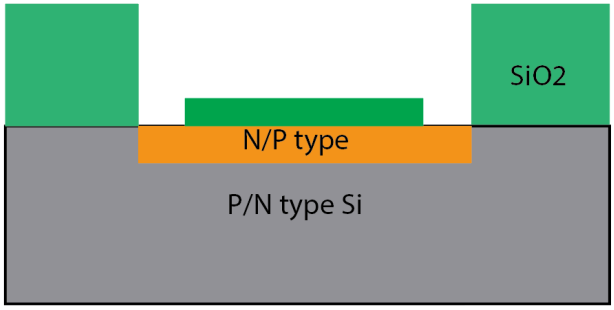

Figure 6: STEP 4 and 5

4. Finally, the metal layer is added and etched to obtain the final product.

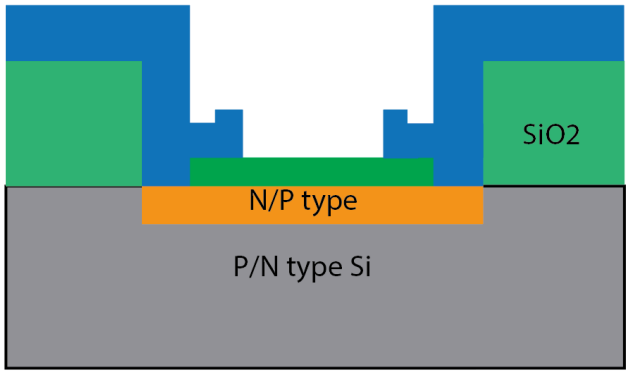

Figure 7: STEP 6 and 7

After that, the assembly process of NMOS will be involved. Figure 8 shows the basic structure of NOMS. NMOS in this report, the layout is shown in Figure 9, which is divided into four masks. The first mask is called active region, which is the basis of the whole structure. The second is Gate. The third is contact region, which is the part where metal contacts n-type semiconductor. The last layer is metal layer.

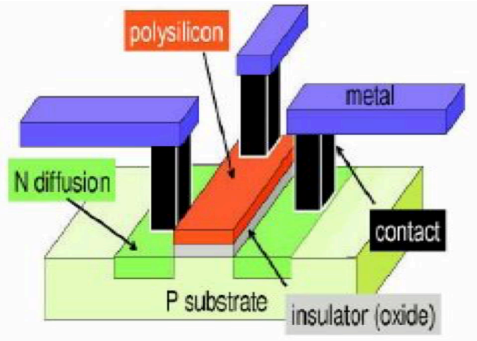

Figure 8: BASIC STRUCTURE OF NMOS[1]

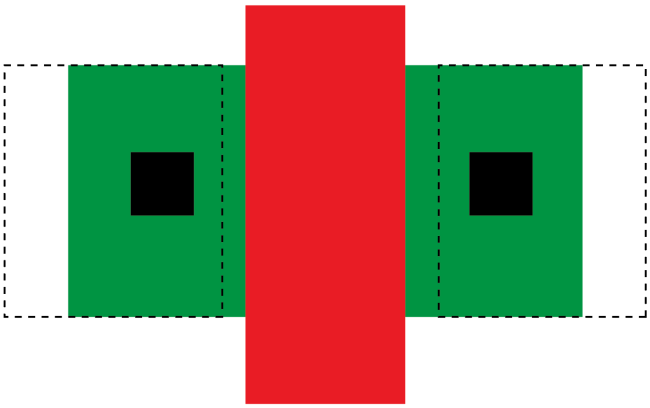

Figure 9: LAYOUT OF NMOS

The production process will be described in detail below. In the first step of this process, a plane of p-type poly-silicon is needed, and then a layer of silica is added to the plane of p-type poly-silicon. After etching, part of the silicon dioxide is removed.

This process is shown in Figure 10.

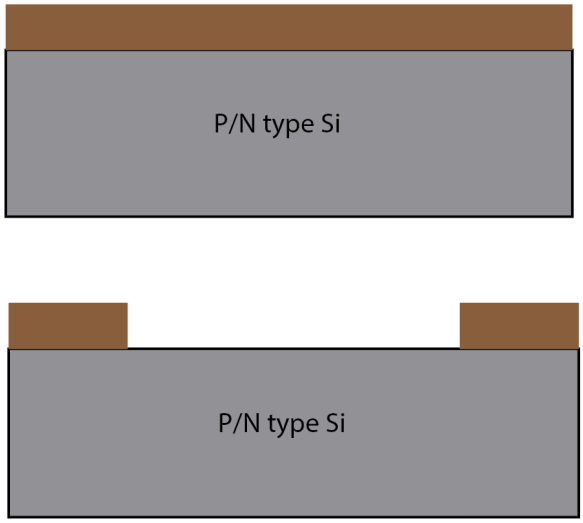

Figure 10: STEP 1

A very thin layer of silicon dioxide is then added and then permeated by heavily doped poly-silicon and etched to form Fig. 11.

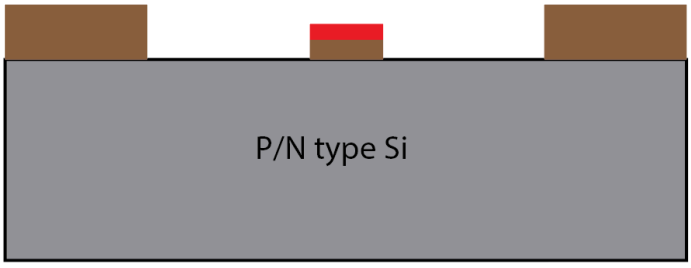

Figure 11: STEP 2

Two p-type poly-silicons were formed by ion infiltration. Two p-type poly-silicons were formed by ion infiltration. The final result is shown in Fig. 12.

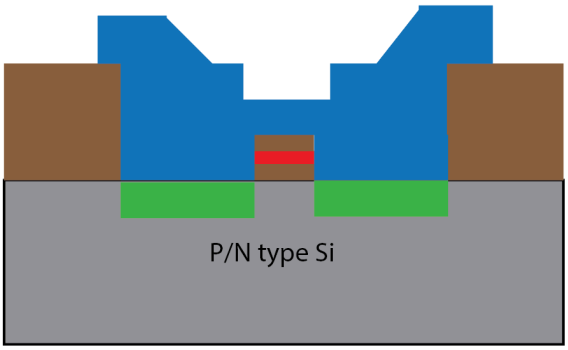

Figure 12: FINAL STEP

2.1.2 Design Rules' description

Active Area Rules		
R1	Minimum Active area Width	3λ
R2	Minimum Active area Spacing	3λ
Poly-Silicon Rules		
R3	Minimum Poly Width	2λ
R4	Minimum Poly Spacing	2λ
R5	Minimum Gate extension of Poly over Active	2λ
R6	Minimum Poly-Active Edge Spacing (Poly Outside of Active area)	λ
R7	Minimum Poly-Active Edge Spacing (Poly Inside of Active area)	3λ
Metal Rules		
R8	Minimum Metal Width	3λ
R9	Minimum Metal Spacing	3λ
Contact Rules		
R10	Poly Contact size	2λ
R11	Minimum Poly Contact Spacing	2λ
R12	Minimum Poly Contact to Poly Edge Spacing	λ
R13	Minimum Poly Contact to Metal Edge Spacing	λ
R14	Minimum Poly Contact to Active Edge Spacing	3λ
R15	Active Contact size	2λ
R16	Minimum Active Contact Spacing (On the same Active region)	2λ
R17	Minimum Active Contact to Active Edge Spacing	λ
R18	Minimum Active Contact to Metal Edge Spacing	λ
R19	Minimum Active Contact to Poly Edge Spacing	2λ
R20	Minimum Active Contact Spacing (On different Active regions)	6λ
Supply Rail Metal		
R21	V_{DD}	>3λ
R22	Ground	>3λ
Resistor Rules		
R23	Minimum resistor width	2λ

For the design rules of semiconductors as shown above, some details are explained below. Let first focus on the R21 and R22, the V_{DD} and ground is made by metal, however, in practical engineering manufacturing, input and output voltage must be reserved a certain space, which is why there is such a requirement. Then, the resistance is made of active area, following the R23, the minimum resistor width is 2$\boldsymbol{\lambda}$. Then, for the R8 and R9, there are only some limitations, such as width and spacing. This also means that metals can have a lot of room to operate. For example, the metal area can directly cross the active area. It could save a lot of space. For the R1 and R2 mentions the libation of active area and R3, R4 has settled some limit of poly-silicon. It should be noted that if the poly-silicon part passes through the activation region, two distances need to be reserved. This is the R5 mentioned. Secondly, there is the distance between contact and contacts on different materials. For example, if two contact are both in the same active region, the width is 2$\boldsymbol{\lambda}$, however, if two contact are in the different active region, the space needs to leave 6$\boldsymbol{\lambda}$. In addition, contacts which in the active region and contact in the poly-silicon region, there are no limitations in there. However, if there are different metal area, it should follow the R9.

2.2 Design of the logic circuit

Firstly, the aim of design is building an OR gate. However, to implement the OR gate logic circuit, the basic design of IC has only NOR gate to use, if an inverter is added, the OR gate can be obtained by transformation. The formula of digital circuit is as follows:

$$X = \overline{\overline{A + B}} = A + B$$

Therefore, a simple NOR gate is implemented as follows in the Figure 13:

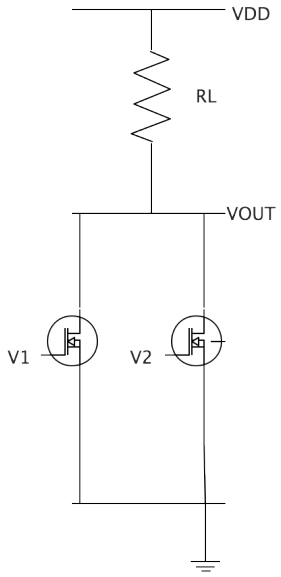

Figure 13: NMOS NOR GATE

The truth table of NOR gate is shown in the Table 1.

V1	V2	Vout
0	0	1
0	1	0
1	0	0
1	1	0

Table 1: TRUTH TABLE OF NOR GATE

In fact, this load resistance can also be replaced by MOS. Of course, considering the complexity, load resistance should be used first. Later, it need to add an inverter to provide OR gate support. The circuit diagram of the inverter is shown in the Figure 14.

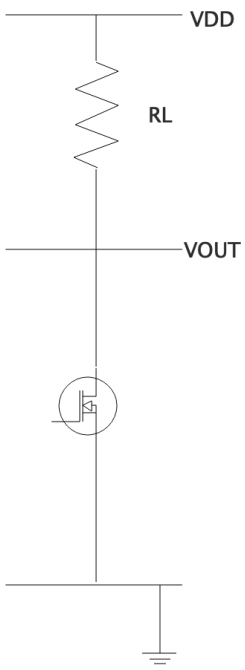

Figure 14: INVERTR CIRCUIT IN NMOS

The truth table of inverter is shown in the Table 2.

Vin	Vout
0	1
1	0

Table 2: TRUTH TABLE OF INVERTER

So if you combine the two, you get OR Gate. That is to say, the output of Figure 13 is connected to the input of Figure 14. The Figure 15 shows OR gate circuit. And the truth table of OR gate is shown in the Table 3.

VA	VB	VC	Vout
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	1

Table 3: TRUTH TABLE OF OR GATE

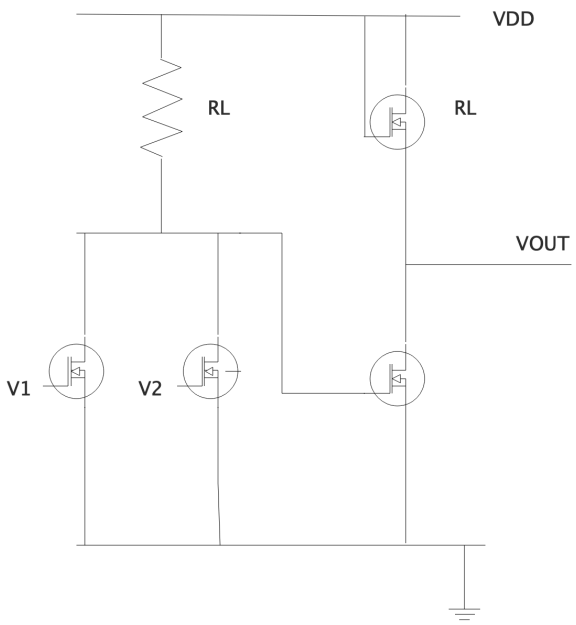

Figure 15: OR GATE IN NMOS CIRCUIT

Next, it calculates the proportion of MOS design. It is relatively simple to calculate the proportion of NOMS in the first part, namely NOR GATE. By using the process parameters shows below in the Table 4.

Normalized Device Constant β_0	1.8×10^{-4} A/V^2
Threshold Voltage VT	0.3 V
Supply Voltage VDD	5 V
High Input Voltages (A and B) V_{IN}	V_{DD}

Low Input Voltages (A and B) V_{IN}	0 V
MOSFET Load Resistance RL	5 kΩ
Sheet Resistance RS	100 Ω/□

Table 4: PROCESS PARAMETERS

First, the load resistance is known to be 5000 ohms. Then the important parameters β is determined the size of the MOS, it should be calculated first. We assumed that the gate voltages are both equal to the V_{DD}, which means that the gate is in the working mode. However, in this mode, there are two specific working modes, one is linear region, the other is saturated region. By using the formula:

$$V_{DS(sat)} = V_{GS} - V_{TN}$$

Which could calculate whether the mode is in the liner or saturation mode.

$$1. V_{DS} < V_{DS(sat)} \quad i_D = \beta[(V_{GS} - V_{TN})v_{DS} - v_{DS}^2/2]$$

$$2. V_{DS} > V_{DS(sat)} \quad i_D = \beta(V_{GS} - V_{TN})^2/2$$

Because the voltage of the input 5 V of two gates has been assumed and if the $V_{out} = 0.1V$, so the V_{DS} is a very small voltage, then it must in the linear region. By calculus the resistor voltage divider, which means:

$$\frac{0.5R_D}{0.5R_D + R_L} = \frac{V_{out}}{V_{DD}} = \frac{0.1V}{5V} = 0.02$$

Because $R_L = 5000\Omega$

We know that $R_D \approx 200\Omega$

Then using the equation: $i_D = \beta[(V_{GS} - V_{TN})v_{DS} - v_{DS}^2/2]$

Using V_{Out}/I_D, the $\beta \approx 10^{-3}$

Because we know the $\beta = \beta_0(W/L)$

The W/L is equal to 6.

Because the load resistance is replaced by MOS, there is no way to get the actual resistance size, so for the sake of simple design, it is directly assumed that the following MOS ratio is the same as before. So the aspect ratios of D is 6.

Then using the equation: $i_D = \beta[(V_{GS} - V_{TN})v_{DS} - v_{DS}^2/2]$

Using $R_D = V_{Out}/I_D = 200\Omega$,

$$\frac{R_D}{R_D + R_L} = \frac{V_{out}}{V_{DD}} = \frac{0.1V}{5V} = 0.02$$

$$R_L \approx 10k\Omega$$

Focus on the top MOS, it is in the saturation mode, so the I_D:

$$i_D = \beta(V_{GS} - V_{TN})^2/2$$

Because $R_L = (V_{DD} - V_{out}/i_D) \approx 10k\Omega$

Then $\beta_L = 4.4 * 10^{-5}$

So W/L = 0.25

So the whole circuit diagram is shown in the Figure 16.

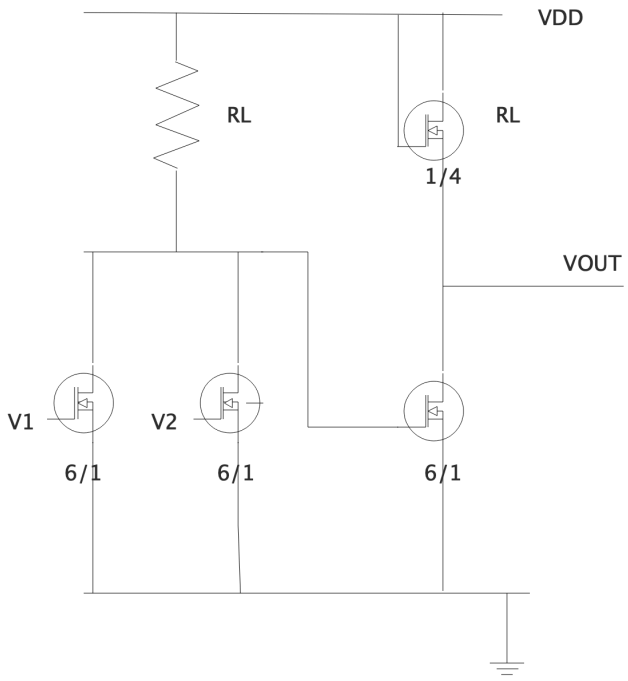

Figure 16: WHOLE CIRCUIT OF DESIGN PROJECT

However, if the ratio of MOS in the lower right corner changes, the ratio of MOS in the upper right corner also needs to be changed accordingly. For example, if the right corner is 12/1, then the right top of MOS needs to be changed to 1/2.

As a summary, computing integrated circuits requires the following steps:

1. The total circuit diagram is analyzed separately, that is, each module is analyzed by digital circuit method.
2. The relationship between input voltage and resistance is analyzed. If there is resistance in the circuit, the output size can be assumed. Then the current size can

be calculated by voltage, the operating mode of MOS can be analyzed and the specific proportion can be calculated. If the circuit uses MOS instead of resistor, it needs to assume a proportion, so that the proportion of the part replacing resistor can be calculated.

3. By using the W/L, then draw and design of the layout.

2.3 Result and Discussion

2.3.1 Changing the Value of Vout

Because both sides of V1 and V2 are the same, they have the same proportion. However, it is worth noting that the above calculations are based on the assumption that the output voltage is 0.1 V, but the actual situation is very likely to be different. Here, we assume that the voltage is two times larger and two times smaller. First, if the output voltage is 0.2 V, let's recalculate the ratio.

$$\frac{0.5R_D}{0.5R_D + R_L} = \frac{V_{out}}{V_{DD}} = \frac{0.2V}{5V} = 0.04$$

Because $R_L = 5000\Omega$

We know that $R_D \approx 417\Omega$

Then using the equation: $i_D = \beta[(V_{GS} - V_{TN})v_{DS} - v_{DS}^2/2]$

Using $V_{Out}/I_{D,}$ the $\beta \approx 5 * 10^{-4}$

Because we know the $\beta = \beta_0(W/L)$

The W/L is equal to 3.

In this case, the ratio is completely different. The output voltage is calculated below at 0.05 V.

$$\frac{0.5R_D}{0.5R_D + R_L} = \frac{V_{out}}{V_{DD}} = \frac{0.05V}{5V} = 0.01$$

Because $R_L = 5000\Omega$

We know that $R_D \approx 100\Omega$

Then using the equation: $i_D = \beta[(V_{GS} - V_{TN})v_{DS} - v_{DS}^2/2]$

Using $V_{Out}/I_{D,}$ the $\beta \approx 2 * 10^{-3}$

Because we know the $\beta = \beta_0(W/L)$

The W/L is equal to 12.

Through the table, we can get different results of different output voltage, it is shown in the Table 5:

V_{out}	$\frac{W}{L}$
0.2	3
0.1	6
0.05	12

Table 5: THE RELATIONSHIP BETWEEN VOUT AND W/L

Therefore, the larger the output voltage, the lower the rate of W/L. Subsequently, the W/L ratio of the inverters part will also be calculated.

2.3.2 Design Rules Application on 4 masks

The whole design is shown in the Figure 17.

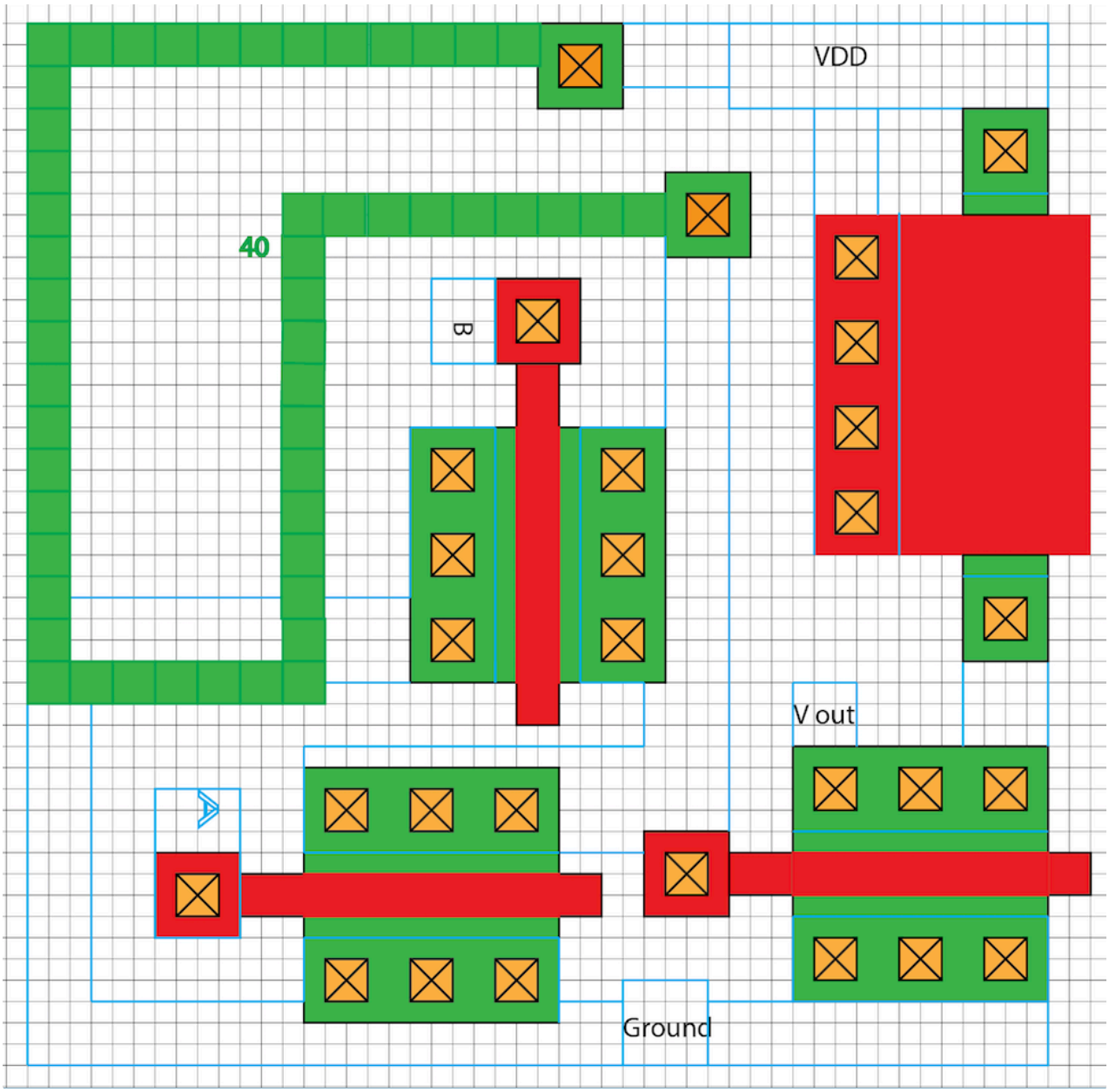

Figure 17 DESIGN OF PROJECT

2.3.3 Chip Area Calculation

This chip uses 49*50's area, which equals 2450 square. In fact, for this layout, I think he has reached a certain design limit. Because in this design, the width of the right half cannot be reduced, while the left half is inevitably wasted due to the use of three units to connect the ground wire. Due to the limitation of metal area and metal area, the length cannot be further reduced.

Firstly, this design uses a part of the MOS in B as a public bridge, and further reduces the area by connecting metal areas. Originally, this design wanted to directly replace the contact of the resistance part with the MOS in B. However, in the design process, the resistance appears a counting pair of corners, so it is impossible to constitute 50. So the idea had to be abandoned. In addition, the active area can also be used for public use, which can further reduce the area. This is the method of reducing the area that needs to be used in future design. It is shown in the Figure 18.

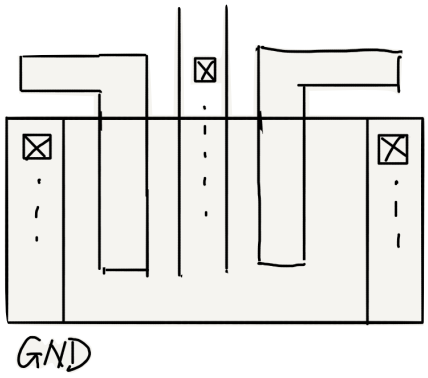

Figure 18: SHAREING ACTIVE REGION

In addition, for GROUND, only 4*4 space is reserved, and there is no need to reserve the size of a long bar. There are the same as the VCC. Then they are connected through metal areas, which saves a unit of space. The last way to save space is to directly connect the parts of the MOS that need to be connected to the ground wire, instead of using a ground wire and then connecting to each other through the metal area as usual, so that some space can be saved. For the improvement of this design, I think that in the future, the input voltage part can be transferred to the left part of the design drawing, and then converted to B function, that is to say, the right side of B is changed into the public connection part, and then using the principle that the active area is not related to the metal area, about three units of space can be saved. Finally, after further streamlining, the target size is: 2100.

4. Conclusion

Finally, as a summary, this design project let me understand the whole simple application process of MOS in integrated circuits. By designing the layout, I think it's a better way to use the computer to draw the previous layout, and then use the designed layout to further refine the space that can be reduced. Compared with the paper version, I think the computing storage method can make the design more flexible. In the future, this layout will be updated, because I think it still has room to shrink.

5. Reference

[1] C. Z. Zhao et al., "nMOSFELT" in ***Introduction to the Integrated Circuit***, 1st ed. Beijing, China, Science Press, 2011, ch. 7