mux

imm
result

0
1

shift
left 1

ADD

PC

mux

1
0

4

ADD

Control Unit

Jump
ToRegister
MemWrite
Branch
ALUOp
StoreSel
ALUSrc
WriteReg

Opcode

funct3

funct7

Instruction [6-0]

Instruction [14-12]

Instruction [31,25]

3

Branch
sign
zero

PCSrc

3

Instruction [19-15]

Instruction [24-20]

Instruction [11-7]

write

Source Reg1
(sr1)

Source Reg2
(sr2)

Destiny
Reg (rd)

CLK

Data

Read
data 1

Read
data 2

Register File [0-31]

3

ALUOp

Sign
Zero

Result

ALU

1
0

mux

LB sign
extend

WriteEn

Address

Data Memory
(RAM)

Read
data 1

Data

CLK

001
010

000   Out

011
100
101

mux

3

Progam
Counter

PCin   PC

clk

rst

Step

Clk/man

Instructions
memory (ROM)

Read
address

Instruction
[31-0]

32

CLK

Reset

Step

clk
/manual

Instruction[31-0]

Immediate
Generator

immediate [31- 0]

byte mask

0
1

mux

Multiplier

Multiplicand

Multiplier

Product

PC

CLK