University of Southampton	***School of Electronics and Computer Science***	***Coursework (2 of 4) Instructions***
Module: ELEC2205	Title: D3 Analogue Design	Lecturer: Dr. Sasan Mahmoodi
Deadline: 1 week after lab session	Feedback: tba	Weighting:

Instructions

This design exercise is all about putting your knowledge of analogue electronics to a practical use. Specifically you are required to design a multi-stage amplifier to a certain specification.

The general specification is as follows.

1. The design should use two stages (a common emitter stage with partially by-passed emitter resistance followed by a common collector stage).
2. The overall gain of both stages should be 6 ± 0.6.
3. The input impedance must be higher than 40 ± 4 kilo ohms.
4. The output impedance should be lower than 1.3 ± 0.13 kilo ohms.

You will be assessed on the basis of how close your actual circuit meets the above specification.

It is expcted that you will design each stage in semi independence, testing each individually before combining them to give the final multi-stage amplifier.

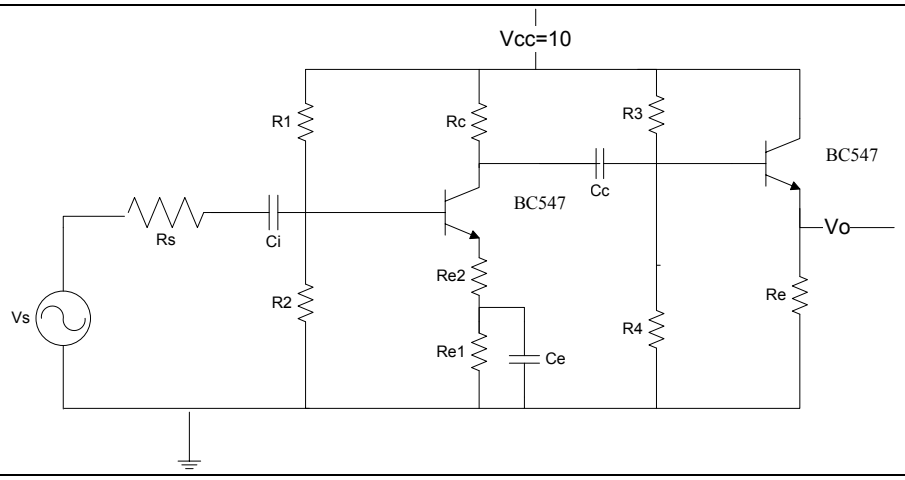

Figure 1: The circuit for the multi-stage amplifier

Restrictions

For this exercise you are restricted to the use of capacitors and resistors from the laboratory supply and the Motorola BC547 which is a specific NPN Bipolar transistor. You may not use any other devices without permission.

Your circuits should have supply voltages of *0* and V_{cc}*=10V*.

You should assume that the transistor has an average current gain β*=200*.

Preparation

Since laboratory time will be very limited for this exercise it is crucial that you carry out the following before coming in to the laboratory.

1. Derive using lecture notes, books or other sources the equations for the mid-band gain, input and output impedance for each of the stages of your amplifier.
2. Remember the output impedance of the first stage should at least be ten times less than the input impedance of the second stage to avoid loading between two stages.
3. Use these to estimate a set of component values such that you hit the desired targets.
4. Simulate your circuit as you were shown in the first year.
5. Repeat steps 2 and 3 until you are happy with the performance of each stage.
6. Combine the stages together and simulate again.
7. Make any necessary changes to the circuit so as to meet the design criteria.

You should determine how you are going to measure the gain, input and output impedance in practice.

In the laboratory

You should use the following steps to generate a plan for your work in the laboratory. This assumes that you have satisfactory designs for the whole and each part of the amplifier.

1. Construct the first stage in isolation.
2. Measure and record the gain, input and output impedance.
    a. If these do not agree with your theoretical predictions determine why.
    b. If necessary, using a principled approach adjust the parameters till you achieve your design solution.
3. Repeat the process for the 2nd stage.
4. Join up the two stages with a 1μF capacitor.
5. Measure the parameters and compare them with those required.
    a. As before adjust your component values until you achieve the desired solution.
6. If time allows try the advanced options below.
7. If there is any high frequency interference, you need to use a 10nF capacitor from Vcc to ground drawn in the circuit close to Q2.

    This 10nF capacitor is known as a ‘decoupling’ capacitor, and helps to ensure that the power supply has a low impedance even at high frequency, where the inductance of the long leads to the power supply can be significant. They are very common in practical circuitry. Occasionally circuits like this can be subject to ‘parasitic oscillations’ which are due to ‘stray’ C and L components caused by long wires etc. Laying your circuit out ‘tidily’, with short leads, helps to avoid these. The 10nF capacitor in particular should have short connections to the collector of Q2 and the ground side of Re. Should parasitic oscillations occur, you will observe them on the oscilloscope as instabilities and a broad band rather than a narrow trace. Ask for help if this occurs.

8. When using ‘electrolytic’ capacitors (typically of high value, with an aluminium ‘can’) , think carefully about which way round to connect it. For this type of capacitor it is important that the DC polarity is correct.
9. When measuring any property of the circuit, gain, input or output impedance etc, it is important that the amplifier is operating in its linear region, will ***all*** the signals being sinusoidal. You may need to pay particular attention to this when measuring the output impedance of the second stage.
10. Before measuring any AC property of the circuit, you are strongly advised to check that the DC operating point is correct, as this is essential to its proper operation. Check Vc,b,e for both transistors and ensure they are appropriate and as expected.
11. When measuring Ri and Ro, you need to use 1uF capacitors between the amplifier and the added resistor in the input or between the amplifier and the load added in the output.

Advanced options

You may have time in the laboratory and you may be interested in making the following observations:

1. You should measure the frequency response of your circuit. This can be done by manually sweeping the input frequency from below the lower cut off for the circuit up to the higher cut-off frequency. Before making any measurements you should first determine what these cut-offs are by inspecting the output as you change frequency. It is appreciated that you may not understand exactly the reasons for this behaviour but inspecting and determining the cut-offs will aid you in understanding later work.
2. It is expected that the first stage will be a common emitter circuit while the second stage will be an emitter follower and that they will be connected by an isolation capacitor. If this is the case then the behaviour of the common emitter stage is interesting with respect to the presence or absence of an emitter resistor by-pass capacitor. What is the gain when:
    a. There is no by-pass capacitor
    b. There is a partial by-pass
    c. The emitter resistance is totally bypassed.
    d. How does this relate to the theory you have found, enabling you to design this stage.

Submission

Please submit a paper copy of your report to the School Office and submit an electronic copy using the ECS electronic hand-in system, C-Bass, by 4pm on the due date. The electronics copy should be in PDF format.

You should bind a copy of your design completion form with the paper copy of the report. If this is not done then you will be awarded zero for technical achievement.

Please keep a copy of the design completion form your self.

The report should be no longer than 3000 words and must cover the following:

1. The theoretical basis for the calculation of the design parameter.
    a. Why is the choice of emitter follower, preceded by a common emitter circuit, a good one?
2. Justification as to why you chose the parameters you did.
3. Explanation as to how you measured gain etc.
4. Any optional results as detailed above.
5. Reflection on the success or otherwise of your design.

Crudely 80% of the marks will come from your technical contents and achievements and 20% for the report (structure, presentation and use of language), see below.

Relevant Learning Outcomes (LOs)

1. To design and simulate a multi-stage amplifier with discrete devices
2. To implement and debug the circuit
3. To write a scientific report
4. To perform scientific measurements
5. To compare the experimental results with theory

Marking Scheme

Criterion	*Description*	*LOs*	*Total*
1	Writing Report	3	20%
2	Theoretical Design	1	35%
3	Simulation	1	15%
4	Circuit Debugging and Implementation	2,4	10%
5	Achieving the goals	5	20%

Late submissions will be penalised at 10% per working day. No work can be accepted after feedback has been given.
You should expect to spend up to hours on this assignment. Please note the University regulations regarding academic integrity.