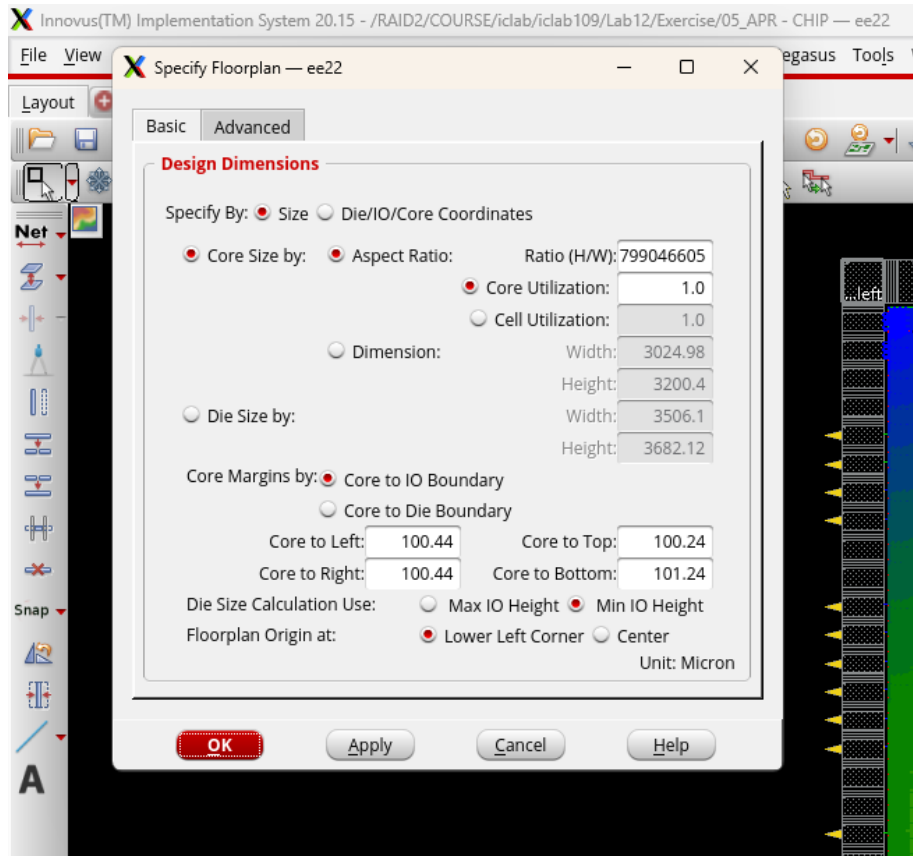
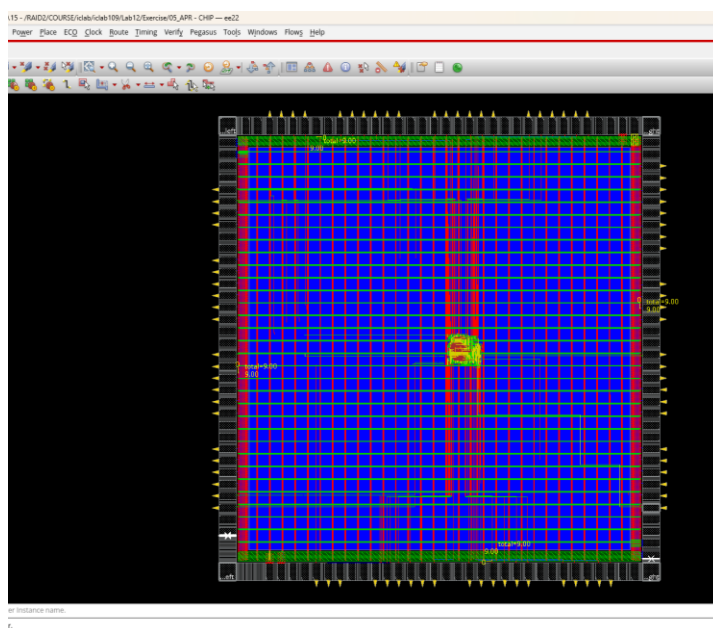


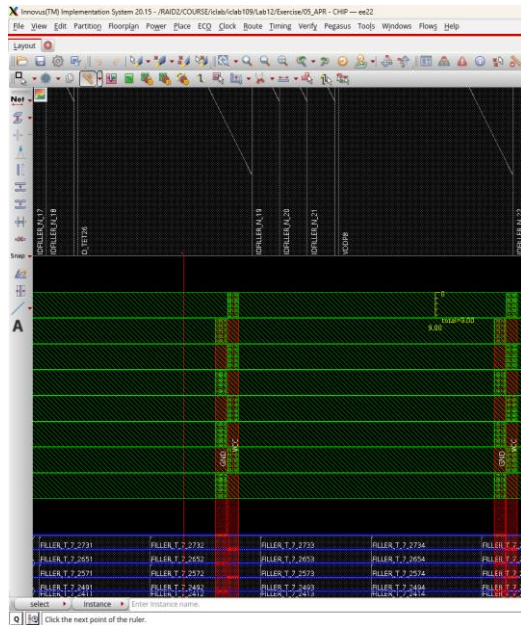
Report

1. Core to IO boundary :

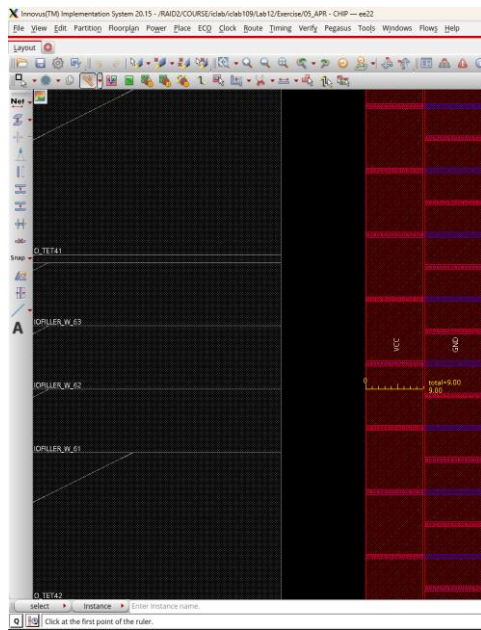


2. Core Ring :

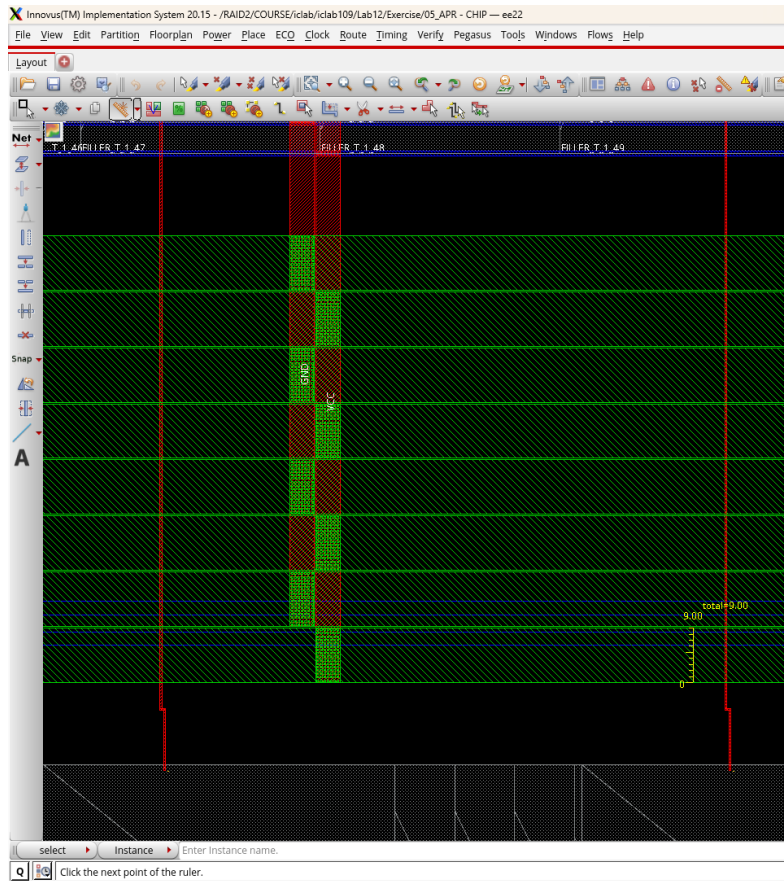




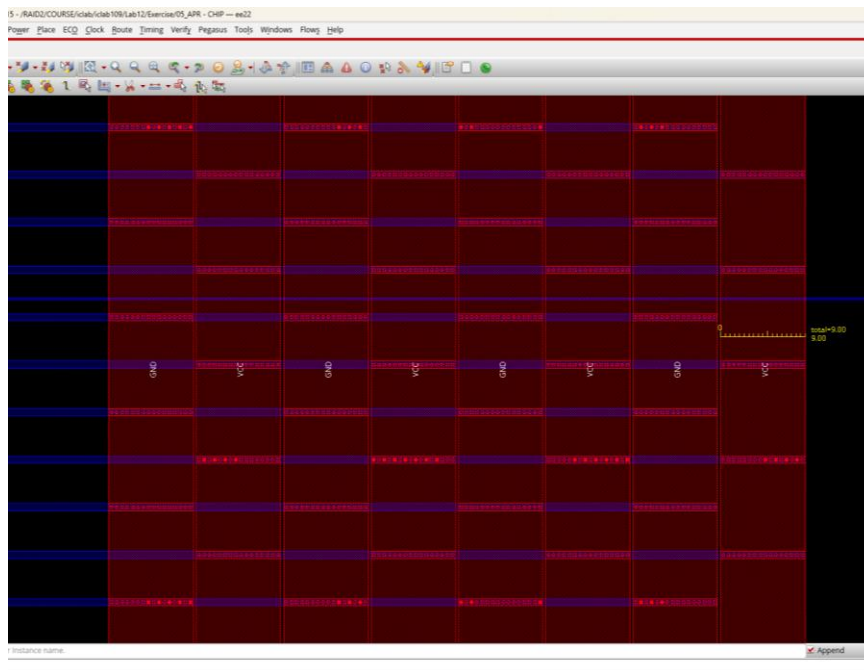
top core ring



left core ring

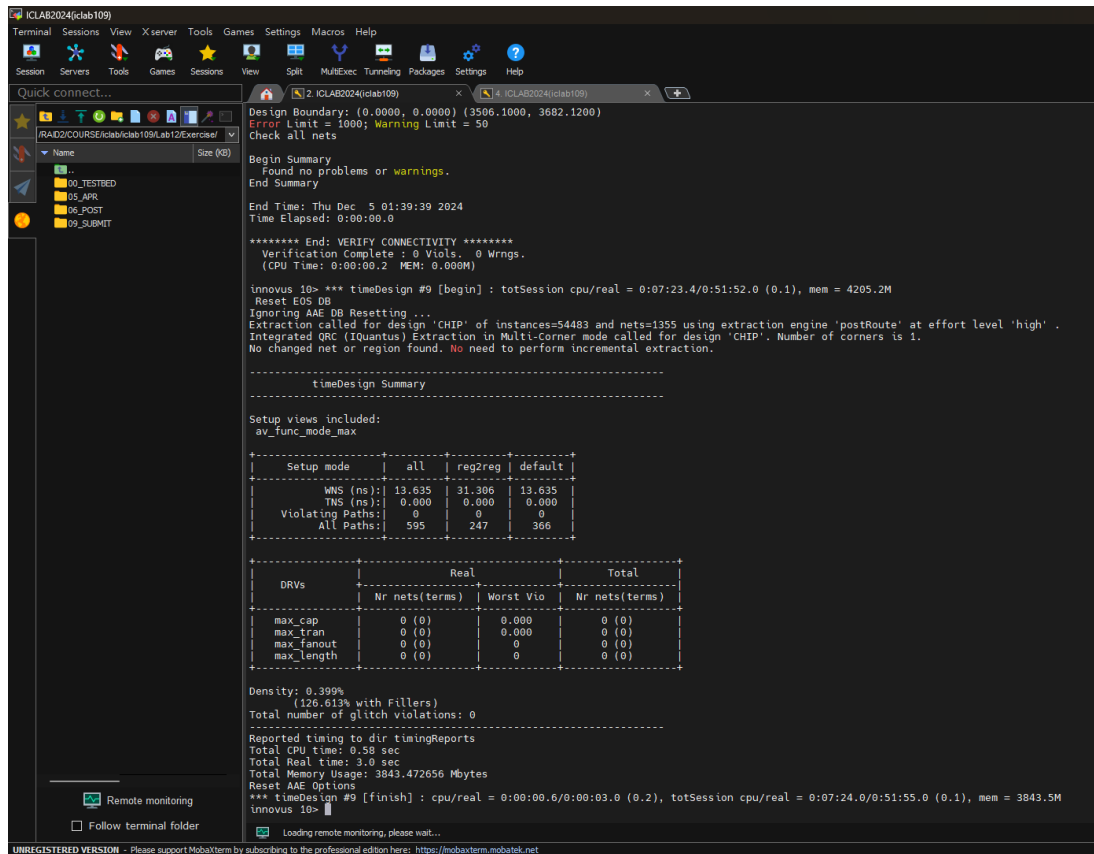


bottom core ring

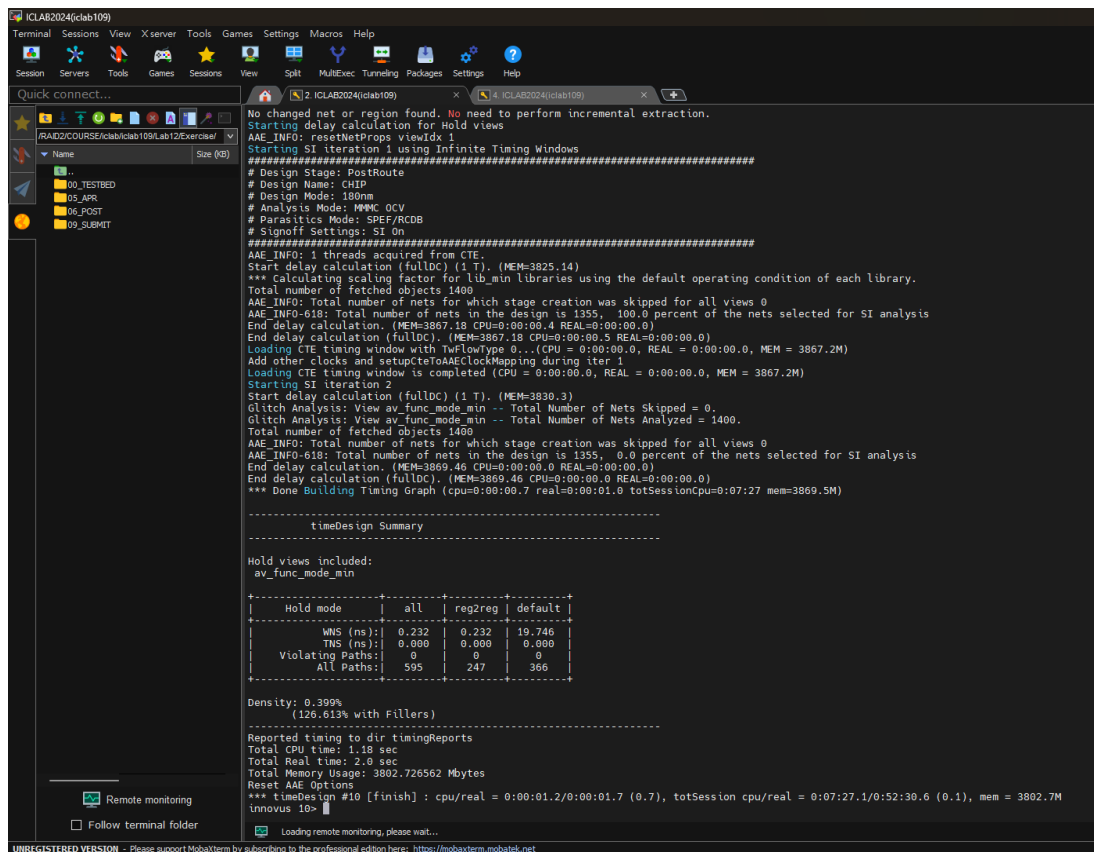


right core ring

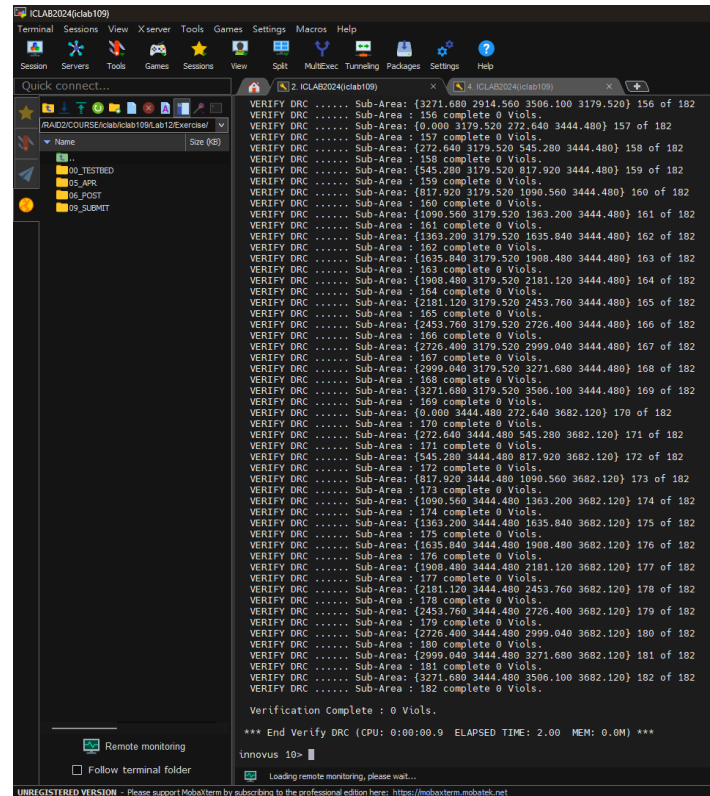
3. Post-Route setup time analysis :



4. Post-Route hold time analysis :



5. DRC result :



The screenshot shows the ICLAB2024 software interface with the DRC (Design Rule Check) results. The main window displays a list of violations, each with a sub-area and a count of violations. The results are as follows:

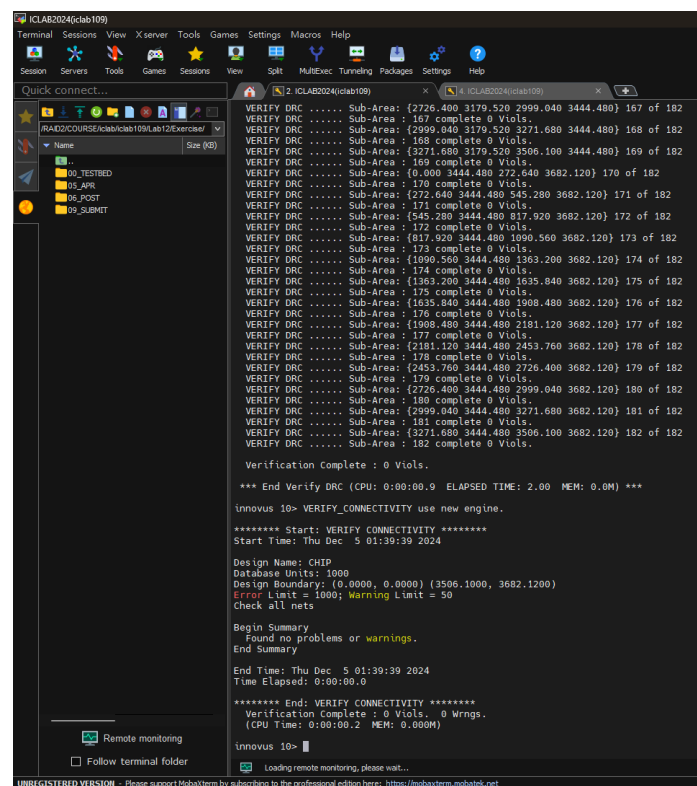
Sub-Area	Violations
Sub-Area : {3271.680 2914.560 3506.100 3179.520}	156 of 182
Sub-Area : 156 complete 0 Viols.	
Sub-Area : {0.000 3179.520 272.640 3444.480}	157 of 182
Sub-Area : 157 complete 0 Viols.	
Sub-Area : {272.640 3179.520 545.280 3444.480}	158 of 182
Sub-Area : 158 complete 0 Viols.	
Sub-Area : {545.280 3179.520 817.920 3444.480}	159 of 182
Sub-Area : 159 complete 0 Viols.	
Sub-Area : {817.920 3179.520 1090.560 3444.480}	160 of 182
Sub-Area : 160 complete 0 Viols.	
Sub-Area : {1090.560 3179.520 1363.200 3444.480}	161 of 182
Sub-Area : 161 complete 0 Viols.	
Sub-Area : {1363.200 3179.520 1635.840 3444.480}	162 of 182
Sub-Area : 162 complete 0 Viols.	
Sub-Area : {1635.840 3179.520 1908.480 3444.480}	163 of 182
Sub-Area : 163 complete 0 Viols.	
Sub-Area : {1908.480 3179.520 2181.120 3444.480}	164 of 182
Sub-Area : 164 complete 0 Viols.	
Sub-Area : {2181.120 3179.520 2453.760 3444.480}	165 of 182
Sub-Area : 165 complete 0 Viols.	
Sub-Area : {2453.760 3179.520 2726.400 3444.480}	166 of 182
Sub-Area : 166 complete 0 Viols.	
Sub-Area : {2726.400 3179.520 2999.040 3444.480}	167 of 182
Sub-Area : 167 complete 0 Viols.	
Sub-Area : {2999.040 3179.520 3271.680 3444.480}	168 of 182
Sub-Area : 168 complete 0 Viols.	
Sub-Area : {3271.680 3179.520 3506.100 3444.480}	169 of 182
Sub-Area : 169 complete 0 Viols.	
Sub-Area : {0.000 3444.480 272.640 3682.120}	170 of 182
Sub-Area : 170 complete 0 Viols.	
Sub-Area : {272.640 3444.480 545.280 3682.120}	171 of 182
Sub-Area : 171 complete 0 Viols.	
Sub-Area : {545.280 3444.480 817.920 3682.120}	172 of 182
Sub-Area : 172 complete 0 Viols.	
Sub-Area : {817.920 3444.480 1090.560 3682.120}	173 of 182
Sub-Area : 173 complete 0 Viols.	
Sub-Area : {1090.560 3444.480 1363.200 3682.120}	174 of 182
Sub-Area : 174 complete 0 Viols.	
Sub-Area : {1363.200 3444.480 1635.840 3682.120}	175 of 182
Sub-Area : 175 complete 0 Viols.	
Sub-Area : {1635.840 3444.480 1908.480 3682.120}	176 of 182
Sub-Area : 176 complete 0 Viols.	
Sub-Area : {1908.480 3444.480 2181.120 3682.120}	177 of 182
Sub-Area : 177 complete 0 Viols.	
Sub-Area : {2181.120 3444.480 2453.760 3682.120}	178 of 182
Sub-Area : 178 complete 0 Viols.	
Sub-Area : {2453.760 3444.480 2726.400 3682.120}	179 of 182
Sub-Area : 179 complete 0 Viols.	
Sub-Area : {2726.400 3444.480 2999.040 3682.120}	180 of 182
Sub-Area : 180 complete 0 Viols.	
Sub-Area : {2999.040 3444.480 3271.680 3682.120}	181 of 182
Sub-Area : 181 complete 0 Viols.	
Sub-Area : {3271.680 3444.480 3506.100 3682.120}	182 of 182
Sub-Area : 182 complete 0 Viols.	

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.9 ELAPSED TIME: 2.00 MEM: 0.0M) ***

innovus 10> Loading remote monitoring, please wait...

6. LVS result :



The screenshot shows the ICLAB2024 software interface with the LVS (Logic Verification Summary) results. The main window displays a list of violations, each with a sub-area and a count of violations. The results are as follows:

Sub-Area	Violations
Sub-Area : {2726.400 3179.520 2999.040 3444.480}	167 of 182
Sub-Area : 167 complete 0 Viols.	
Sub-Area : {2999.040 3179.520 3271.680 3444.480}	168 of 182
Sub-Area : 168 complete 0 Viols.	
Sub-Area : {3271.680 3179.520 3506.100 3444.480}	169 of 182
Sub-Area : 169 complete 0 Viols.	
Sub-Area : {0.000 3444.480 272.640 3682.120}	170 of 182
Sub-Area : 170 complete 0 Viols.	
Sub-Area : {272.640 3444.480 545.280 3682.120}	171 of 182
Sub-Area : 171 complete 0 Viols.	
Sub-Area : {545.280 3444.480 817.920 3682.120}	172 of 182
Sub-Area : 172 complete 0 Viols.	
Sub-Area : {817.920 3444.480 1090.560 3682.120}	173 of 182
Sub-Area : 173 complete 0 Viols.	
Sub-Area : {1090.560 3444.480 1363.200 3682.120}	174 of 182
Sub-Area : 174 complete 0 Viols.	
Sub-Area : {1363.200 3444.480 1635.840 3682.120}	175 of 182
Sub-Area : 175 complete 0 Viols.	
Sub-Area : {1635.840 3444.480 1908.480 3682.120}	176 of 182
Sub-Area : 176 complete 0 Viols.	
Sub-Area : {1908.480 3444.480 2181.120 3682.120}	177 of 182
Sub-Area : 177 complete 0 Viols.	
Sub-Area : {2181.120 3444.480 2453.760 3682.120}	178 of 182
Sub-Area : 178 complete 0 Viols.	
Sub-Area : {2453.760 3444.480 2726.400 3682.120}	179 of 182
Sub-Area : 179 complete 0 Viols.	
Sub-Area : {2726.400 3444.480 2999.040 3682.120}	180 of 182
Sub-Area : 180 complete 0 Viols.	
Sub-Area : {2999.040 3444.480 3271.680 3682.120}	181 of 182
Sub-Area : 181 complete 0 Viols.	
Sub-Area : {3271.680 3444.480 3506.100 3682.120}	182 of 182
Sub-Area : 182 complete 0 Viols.	

Verification Complete : 0 Viols.

*** End Verify DRC (CPU: 0:00:00.9 ELAPSED TIME: 2.00 MEM: 0.0M) ***

innovus 10> VERIFY CONNECTIVITY use new engine.

***** Start: VERIFY CONNECTIVITY *****

Start Time: Thu Dec 5 01:39:39 2024

Design Name: CHIP

Database Units: 1000

Design Boundary: (0.0000, 0.0000) (3506.1000, 3682.1200)

Error Limit = 1000; Warning Limit = 50

Check all nets

Begin Summary

Found no problems or warnings.

End Summary

End Time: Thu Dec 5 01:39:39 2024

Time Elapsed: 0:00:00.0

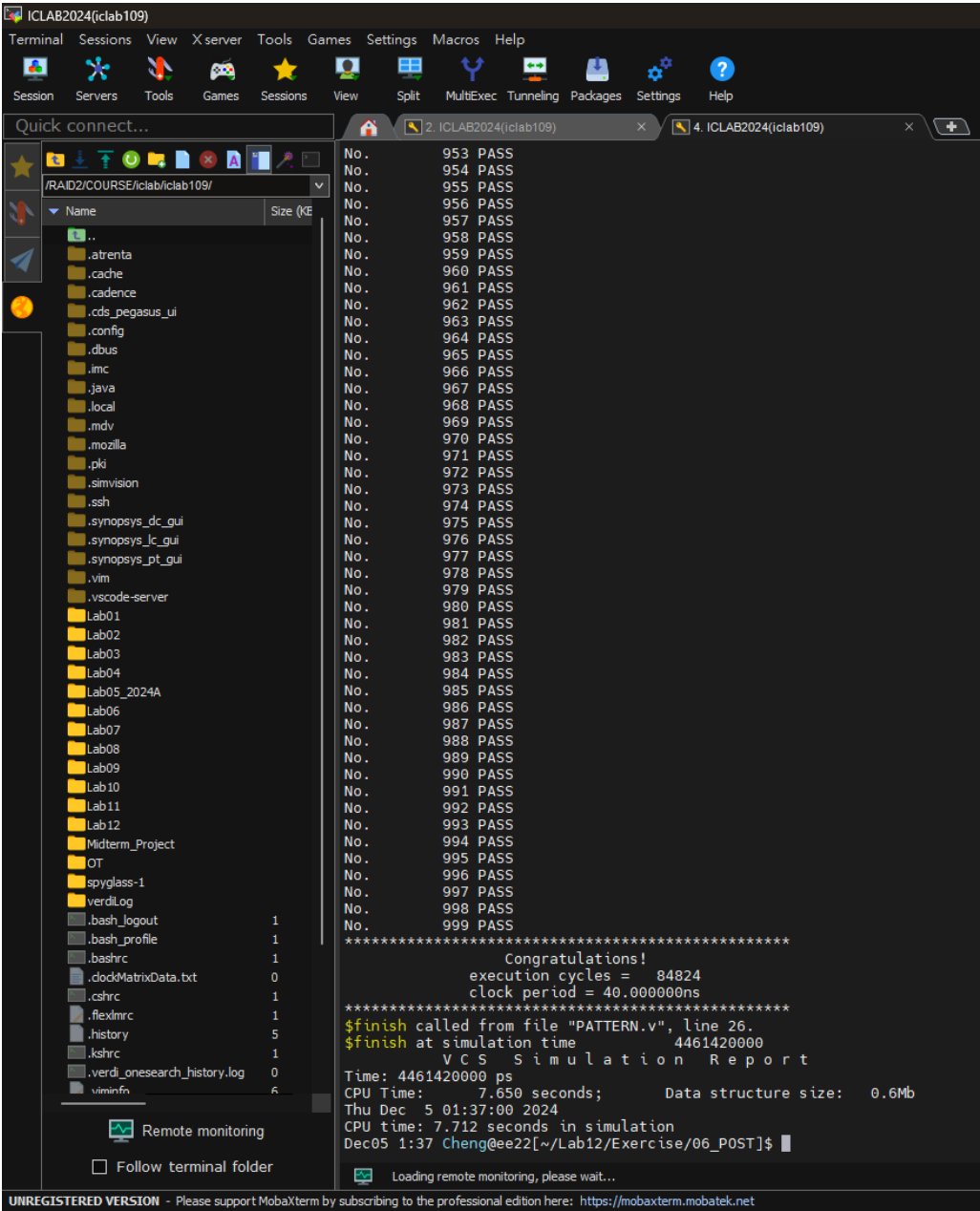
***** End: VERIFY CONNECTIVITY *****

Verification Complete : 0 Viols. 0 Wrngs.

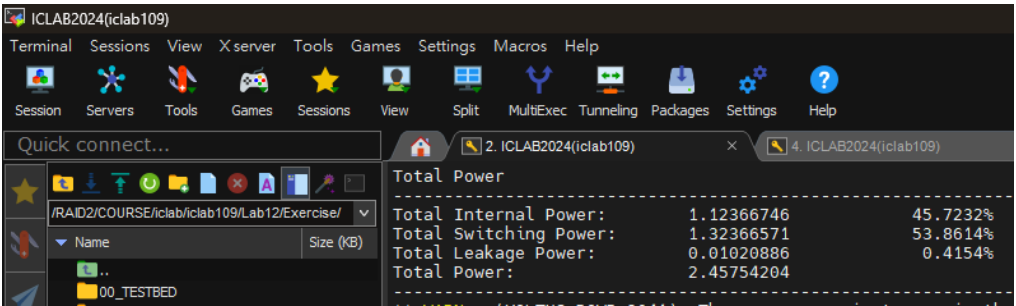
(CPU Time: 0:00:00.2 MEM: 0.000M)

innovus 10> Loading remote monitoring, please wait...

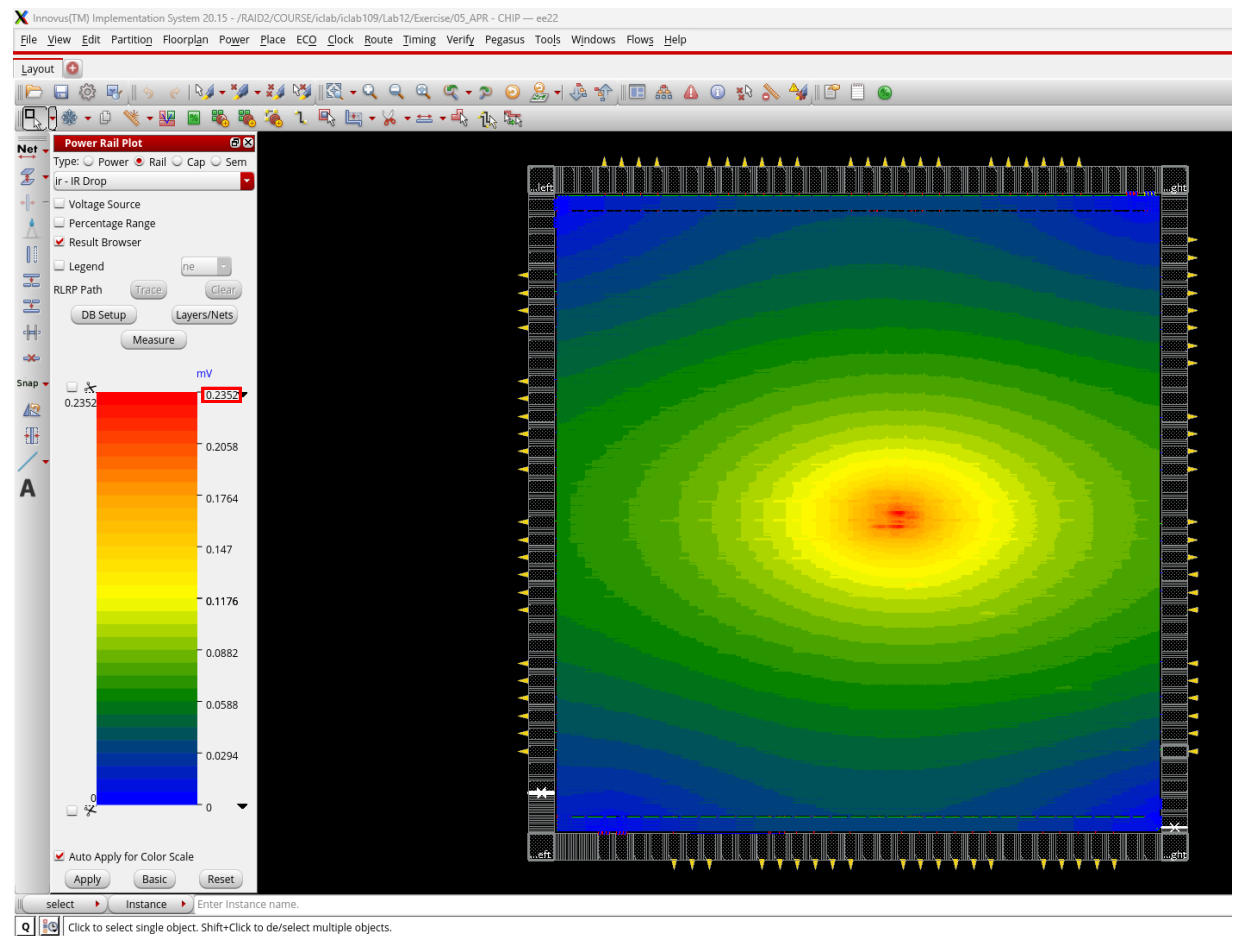
7. Post Layout simulation result :



8. Power result :



9. IR Drop Results :



減少 IR drop :

1. 在 I/O pad 的安排上，我使用了多組 I/O power pad，確保每兩組 I/O power pad 之間不超過 8 組 I/O pad，避免過長的 power line。
2. 比起 Lab11 使用 width 5 的 stripe，這次我嘗試使用 width 4 的 stripe，減少 cells 到 power 的距離。

以上兩個方法背後的想法都是減少 power line 的長度以及可能產生的 buffer，以此減少 IR drop。