TENTATIVE Lecture and Lab Schedule for ECE 241F, 2016

Week	Topics covered	Textbook Sections	Lab Exercises
Sept 5 1	Overview of the course: topics covered, mark breakdown (midterm test, labs, final exam), overview of how the lab exercises are organized (students work in groups of two), marks assigned for preparation and lab performance); Quick overview of digital systems and Moore's law, examples of digital systems; Transistors as simple on-off switches	Chapter 1	
Sept 12 2	Project intro, videos Binary numbers, hex numbers Introduction to logic expressions; AND, OR, NOT circuits built using switches; AND, OR, NOT gate symbols; truth tables; simple example of logic circuit with AND, OR, NOT gates Boolean algebra: duality, axioms, rules, identities; proof of identities using perfect induction (i.e., truth tables); algebraic manipulation of Boolean expressions; timing diagrams; Venn Diagrams and their use to prove some identities Simple synthesis of logic circuits; sum-of-products (SOP) form; minterms; canonical SOP; product-of-sums form (POS); maxterms; canonical POS; examples of algebraic manipulation Intro to Lab 1	 3.1 2.1 – 2.4 2.5 2.6 B.5	
Sept 19 5	Example logic functions: 2-to-1 multiplexer, XOR gate, full-adder, ripple-carry adder, 7-seg; NAND and NOR logic networks; convert SOP to NAND-NAND, POS to NOR-NOR. Verilog introduction, including hierarchy	2.7, 2.8, 3.2 2.10, Appendix A	Lab 1: Building Circuits Using 7400-Series Chips Lab tutorial: Read on your own time the tutorial: Quartus Introduction (you must at least do the version that uses Verilog, and can consider also doing the Schematic design version). Download tutorials from https://www.altera.com/support/training/university/materials-tutorials.html; perform tutorial steps outside of the lab using simulation only
Sept 26 8	Introduction to Field Programmable Gate Arrays (FPGAs), lookup tables; Introduction to CAD tools Introduction to cost of a logic circuit; terminology: implicant, prime implicant (PI), essential PI, cover, minimum-cost cover; introduction to K-maps (2, 3, 4 variables) More examples of K-maps use, including as a guide to algebraic manipulation	B.6.5, 2.9 2.11 – 2.14	 Lab 2: Multiplexers, Hierarchy, and HEX Displays
Oct 3 11	5-variable K-maps; don't cares, examples, including 7-seg with don't cares Storage elements: introduction, RS latches, timing diagrams, gated RS latch. Gated D latch, D flip-flops, Flip-flop reset/preset, setup and hold times	2.8.3 5.1 - 5.4, 5.7	 Lab 3: The case statement, Adders, and ALUs
Oct 10 14	Verilog latches in if-else, case statements Registers, shift registers, Verilog for registers, blocking vs non-blocking FFs in FPGAs	A.11.1 – A.11.4 5.8, 5.12, 5.13, A.11.7	**Midterm on Wednesday, Oct. 12, 2016 in EX 100 and EX 300 from 6-8pm.**
Oct 17 17	T FF Counters; ripple and synchronous counters; Verilog for counters, enable inputs Timing, skew	5.5 5.9, 5.10, 5.13 5.15	Lab 4: Latches, Flip-flops, and Registers
Oct 24 20	Finite state machines intro FSM state assignment, binary encoding, one-hot, Verilog code for FSMs	6.1 6.2, 6.4, 6.5	Lab 5: Clocks and Counters
Oct 31 23	FSM timing issues (Moore vs Mealy models) RAM and ROM, including FPGA embedded memory Discussion of course project, incl VGA and videos	6.3 B.9	Lab 6: Finite State Machines
Nov 7 26	Signed numbers; 2's complement; adders/subtractors, arithmetic overflow Carry lookahead adders, multipliers	3.3 3.4, 3.6	Lab 7: Memory and VGA Display
Nov 14 29	Arithmetic coding with Verilog Combinational circuits: implementing logic functions using only multiplexers, Shannon's Expansion Logic Synthesis using LUTs	3.5 4.1 B.6.5	 Project 1
Nov 21 32	Decoders, other combinational circuits; Verilog code FSM State Minimization Design example: Introduction to processors	4.2 – 4.6 6.6 7.1 – 7.2	Project 2
Nov 28 35	More simple processor Transistors and gates, structure Passing 1's and 0's, transmission gates, fan-in	 B.1 – B.3, B.8.1 B.8.7 – B.8.9	Project 3
Dec 5 38	Clock skew, clock synchronization, switch debouncing	7.8	

Informal tutorials will be held every Thursday, 2 to 3pm in BA 3008 starting September 15, 2016 every week before Labs 1 to 7.