



1. Description

1.1. Project

Project Name	PDCL_MCU_V1
Board Name	custom
Generated with:	STM32CubeMX 6.14.1
Date	05/05/2025

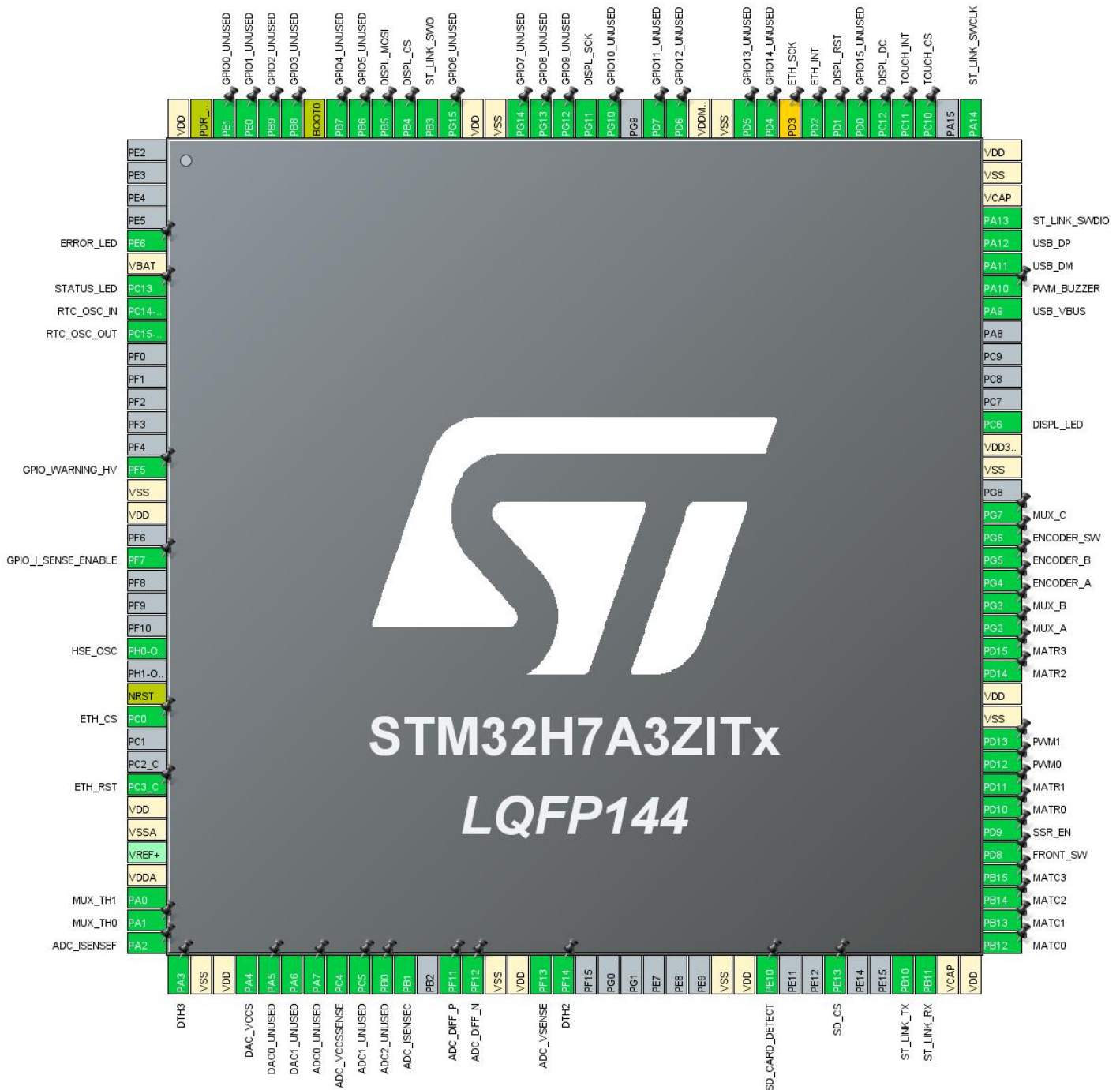
1.2. MCU

MCU Series	STM32H7
MCU Line	STM32H7A3/7B3
MCU name	STM32H7A3ZITx
MCU Package	LQFP144
MCU Pin number	144

1.3. Core(s) information

Core(s)	Arm Cortex-M7
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2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
5	PE6 *	I/O	GPIO_Output	ERROR_LED
6	VBAT	Power		
7	PC13 *	I/O	GPIO_Output	STATUS_LED
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	RTC_OSC_IN
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	RTC_OSC_OUT
15	PF5 *	I/O	GPIO_Output	GPIO_WARNING_HV
16	VSS	Power		
17	VDD	Power		
19	PF7 *	I/O	GPIO_Input	GPIO_I_SENSE_ENABLE
23	PH0-OSC_IN	I/O	RCC_OSC_IN	HSE_OSC
25	NRST	Reset		
26	PC0 *	I/O	GPIO_Output	ETH_CS
29	PC3_C *	I/O	GPIO_Output	ETH_RST
30	VDD	Power		
31	VSSA	Power		
33	VDDA	Power		
34	PA0	I/O	ADC1_INP16	MUX_TH1
35	PA1	I/O	ADC1_INP17	MUX_TH0
36	PA2	I/O	ADC1_INP14	ADC_ISENSEF
37	PA3	I/O	ADC1_INP15	DTH3
38	VSS	Power		
39	VDD	Power		
40	PA4	I/O	DAC1_OUT1	DAC_VCCS
41	PA5	I/O	ADC1_INP19, DAC1_OUT2	DAC0_UNUSED
42	PA6	I/O	DAC2_OUT1	DAC1_UNUSED
43	PA7	I/O	ADC2_INP7	ADC0_UNUSED
44	PC4	I/O	ADC1_INP4, ADC2_INP4	ADC_VCCSSENSE
45	PC5	I/O	ADC2_INP8	ADC1_UNUSED
46	PB0	I/O	ADC1_INP9	ADC2_UNUSED
47	PB1	I/O	ADC1_INP5	ADC_ISENSEC
49	PF11	I/O	ADC1_INP2	ADC_DIFF_P
50	PF12	I/O	ADC1_INN2, ADC1_INP6	ADC_DIFF_N
51	VSS	Power		
52	VDD	Power		
53	PF13	I/O	ADC2_INP2	ADC_VSENSE
54	PF14	I/O	ADC2_INP6	DTH2

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
61	VSS	Power		
62	VDD	Power		
63	PE10	I/O	GPIO_EXTI10	SD_CARD_DETECT
66	PE13 *	I/O	GPIO_Output	SD_CS
69	PB10	I/O	USART3_TX	ST_LINK_TX
70	PB11	I/O	USART3_RX	ST_LINK_RX
71	VCAP	Power		
72	VDD	Power		
73	PB12 *	I/O	GPIO_Output	MATC0
74	PB13 *	I/O	GPIO_Output	MATC1
75	PB14 *	I/O	GPIO_Output	MATC2
76	PB15 *	I/O	GPIO_Output	MATC3
77	PD8	I/O	GPIO_EXTI8	FRONT_SW
78	PD9 *	I/O	GPIO_Output	SSR_EN
79	PD10 *	I/O	GPIO_Input	MATR0
80	PD11 *	I/O	GPIO_Input	MATR1
81	PD12	I/O	TIM4_CH1	PWM0
82	PD13	I/O	TIM4_CH2	PWM1
83	VSS	Power		
84	VDD	Power		
85	PD14 *	I/O	GPIO_Input	MATR2
86	PD15 *	I/O	GPIO_Input	MATR3
87	PG2 *	I/O	GPIO_Output	MUX_A
88	PG3 *	I/O	GPIO_Output	MUX_B
89	PG4 *	I/O	GPIO_Input	ENCODER_A
90	PG5 *	I/O	GPIO_Input	ENCODER_B
91	PG6	I/O	GPIO_EXTI6	ENCODER_SW
92	PG7 *	I/O	GPIO_Output	MUX_C
94	VSS	Power		
95	VDD33_USB	Power		
96	PC6	I/O	TIM8_CH1	DISPL_LED
101	PA9	I/O	USB_OTG_HS_VBUS	USB_VBUS
102	PA10	I/O	TIM1_CH3	PWM_BUZZER
103	PA11	I/O	USB_OTG_HS_DM	USB_DM
104	PA12	I/O	USB_OTG_HS_DP	USB_DP
105	PA13	I/O	DEBUG_JTMS-SWDIO	ST_LINK_SWDIO
106	VCAP	Power		
107	VSS	Power		
108	VDD	Power		

Pin Number LQFP144	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
109	PA14	I/O	DEBUG_JTCK-SWCLK	ST_LINK_SWCLK
111	PC10 *	I/O	GPIO_Output	TOUCH_CS
112	PC11	I/O	GPIO_EXTI11	TOUCH_INT
113	PC12 *	I/O	GPIO_Output	DISPL_DC
114	PD0 *	I/O	GPIO_Output	GPIO15_UNUSED
115	PD1 *	I/O	GPIO_Output	DISPL_RST
116	PD2	I/O	GPIO_EXTI2	ETH_INT
117	PD3 **	I/O	SPI2_SCK	ETH_SCK
118	PD4 *	I/O	GPIO_Output	GPIO14_UNUSED
119	PD5 *	I/O	GPIO_Output	GPIO13_UNUSED
120	VSS	Power		
121	VDDMMC	Power		
122	PD6 *	I/O	GPIO_Output	GPIO12_UNUSED
123	PD7 *	I/O	GPIO_Output	GPIO11_UNUSED
125	PG10 *	I/O	GPIO_Output	GPIO10_UNUSED
126	PG11	I/O	SPI1_SCK	DISPL_SCK
127	PG12 *	I/O	GPIO_Output	GPIO9_UNUSED
128	PG13 *	I/O	GPIO_Output	GPIO8_UNUSED
129	PG14 *	I/O	GPIO_Output	GPIO7_UNUSED
130	VSS	Power		
131	VDD	Power		
132	PG15 *	I/O	GPIO_Output	GPIO6_UNUSED
133	PB3	I/O	DEBUG_JTDO-SWO	ST_LINK_SWO
134	PB4 *	I/O	GPIO_Output	DISPL_CS
135	PB5	I/O	SPI1_MOSI	DISPL_MOSI
136	PB6 *	I/O	GPIO_Output	GPIO5_UNUSED
137	PB7 *	I/O	GPIO_Output	GPIO4_UNUSED
138	BOOT0	Boot		
139	PB8 *	I/O	GPIO_Output	GPIO3_UNUSED
140	PB9 *	I/O	GPIO_Output	GPIO2_UNUSED
141	PE0 *	I/O	GPIO_Output	GPIO1_UNUSED
142	PE1 *	I/O	GPIO_Output	GPIO0_UNUSED
143	PDR_ON	Reset		
144	VDD	Power		

* The pin is affected with an I/O function

** The pin is affected with a peripheral function but no peripheral mode is activated



1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32H7
Line	STM32H7A3/7B3
MCU	STM32H7A3ZITx
Datasheet	DS13139_Rev0

1.2. Parameter Selection

Temperature	25
Vdd	3.0

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

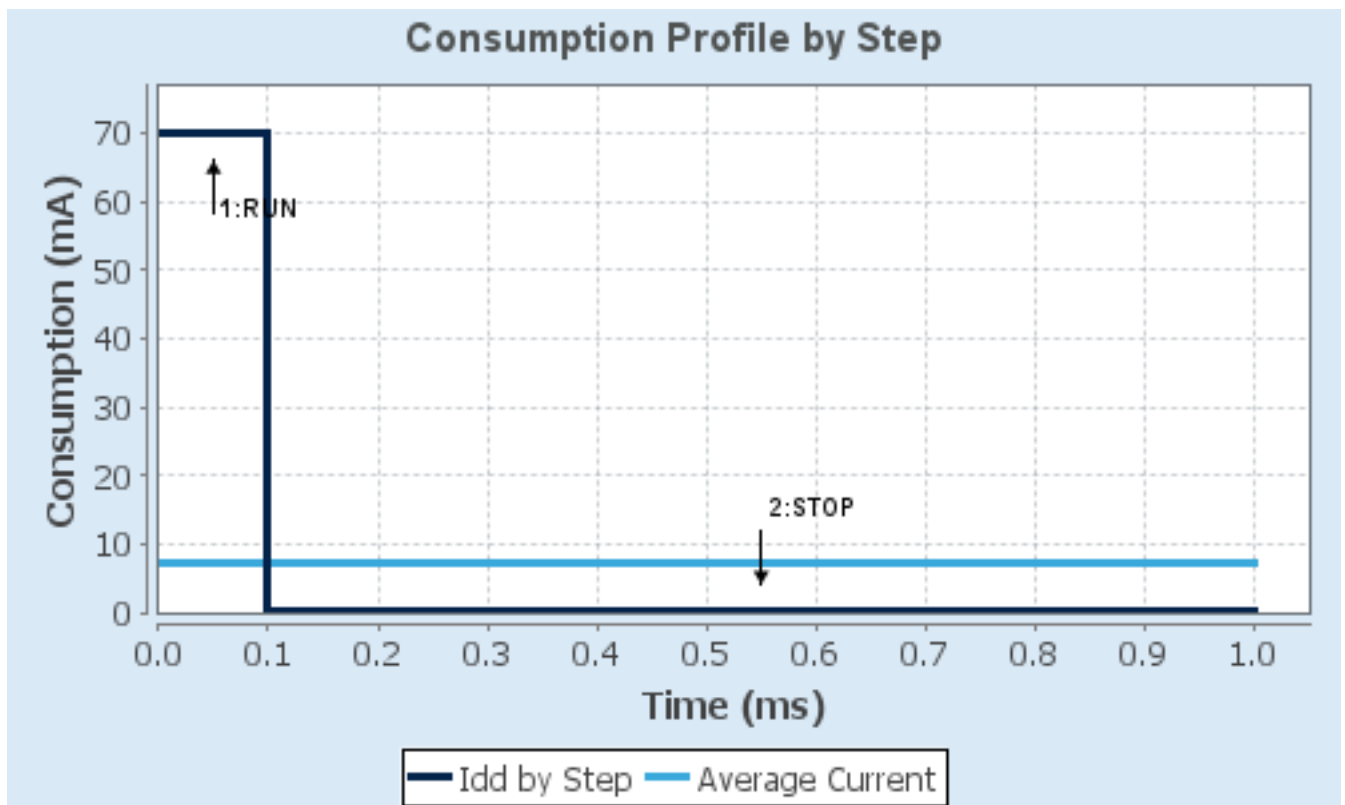
1.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.0	3.0
Voltage Source	Battery	Battery
Range	VOS0	SVOS5
SRDomain	DRUN	DSTOP
n/a	SRDRUN	SRDSTOP
Fetch Type	ITCM/DTCM/Cache	NA
CPU Frequency	280 MHz	64 MHz
Clock Configuration	HSE PLL	HSI Flash-ON
Clock Source Frequency	16 MHz	64 MHz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	69.92 mA	263.82 μ A
Duration	0.1 ms	0.9 ms
DMIPS	599.0	0.0
Ta Max	115.77	124.97
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	7.23 mA
Battery Life	19 days, 14 hours	Average DMIPS	599.2 DMIPS

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	PDCL_MCU_V1
Project Folder	D:\University_Work\STM32\STM32_CubeIDE_Projects\PDCL_V1
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_H7 V1.12.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_DMA_Init	DMA
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_DAC1_Init	DAC1
7	MX_DAC2_Init	DAC2
8	MX_RTC_Init	RTC
9	MX_SPI1_Init	SPI1
10	MX_TIM4_Init	TIM4
11	MX_TIM8_Init	TIM8

Rank	Function Name	Peripheral Instance Name
12	MX_USART3_UART_Init	USART3
13	MX_TIM1_Init	TIM1
14	MX_USB_DEVICE_Init	USB_DEVICE
15	MX_CRC_Init	CRC
16	MX_TIM3_Init	TIM3
17	MX_TIM12_Init	TIM12
18	MX_TIM15_Init	TIM15
20	MX_TouchGFX_Init	STMicroelectronics.X-CUBE-TOUCHGFX.4.25.0
21	MX_TouchGFX_Process	STMicroelectronics.X-CUBE-TOUCHGFX.4.25.0

3. *Peripherals and Middlewares Configuration*

3.1. ADC1

IN2: IN2 Single-ended

IN4: IN4 Single-ended

IN5: IN5 Single-ended

mode: IN6

mode: IN9

mode: IN14

mode: IN15

IN16: IN16 Single-ended

mode: IN17

mode: IN19

3.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler **Asynchronous clock mode divided by 4 ***

Resolution ADC 16-bit resolution

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Left Bit Shift No bit shift

Conversion Data Management Mode **DMA Circular Mode ***

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion **8 ***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 2

Sampling Time **387.5 Cycles ***

Offset Number No offset

Offset Signed Saturation Disable

<u>Rank</u>	2 *
Channel	Channel 6 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
<u>Rank</u>	3 *
Channel	Channel 5 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
<u>Rank</u>	4 *
Channel	Channel 14 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
<u>Rank</u>	5 *
Channel	Channel 15 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
<u>Rank</u>	6 *
Channel	Channel 16 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
<u>Rank</u>	7 *
Channel	Channel 17 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
<u>Rank</u>	8 *
Channel	Channel 4 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
ADC_Injected_ConversionMode:	
Enable Injected Conversions	Disable
Analog Watchdog 1:	

Enable Analog WatchDog1 Mode false

Analog Watchdog 2:

Enable Analog WatchDog2 Mode false

Analog Watchdog 3:

Enable Analog WatchDog3 Mode false

3.2. ADC2

IN2: IN2 Single-ended

IN4: IN4 Single-ended

mode: IN6

mode: IN7

mode: IN8

3.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler **Asynchronous clock mode divided by 4 ***

Resolution ADC 16-bit resolution

Scan Conversion Mode Enabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

End Of Conversion Selection End of single conversion

Overrun behaviour Overrun data preserved

Left Bit Shift No bit shift

Conversion Data Management Mode **DMA Circular Mode ***

Low Power Auto Wait Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable

Enable Regular Oversampling Disable

Number Of Conversion **3 ***

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 2

Sampling Time **387.5 Cycles ***

Offset Number No offset

Offset Signed Saturation Disable

Rank	2 *
Channel	Channel 6 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable
Rank	3 *
Channel	Channel 4 *
Sampling Time	387.5 Cycles *
Offset Number	No offset
Offset Signed Saturation	Disable

ADC_Injected_ConversionMode:

Enable Injected Conversions	Disable
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Analog Watchdog 1:

Enable Analog WatchDog1 Mode	false
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Analog Watchdog 2:

Enable Analog WatchDog2 Mode	false
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Analog Watchdog 3:

Enable Analog WatchDog3 Mode	false
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3.3. CORTEX_M7

3.3.1. Parameter Settings:

Speculation default mode Settings:

Speculation default mode	Enabled *
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Cortex Interface Settings:

CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	Background Region Privileged accesses only + MPU Disabled during hard fault, NMI and FAULTMASK handlers
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Cortex Memory Protection Unit Region 0 Settings:

MPU Region	Enabled
MPU Region Base Address	0x0 *
MPU Region Size	4GB
MPU SubRegion Disable	0x87 *
MPU TEX field level	level 0
MPU Access Permission	ALL ACCESS NOT PERMITTED
MPU Instruction Access	DISABLE

MPU Shareability Permission	ENABLE
MPU Cacheable Permission	DISABLE
MPU Bufferable Permission	DISABLE

Cortex Memory Protection Unit Region 1 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 2 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 3 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 4 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 5 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 6 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 7 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 8 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 9 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 10 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 11 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 12 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 13 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 14 Settings:

MPU Region	Disabled
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Cortex Memory Protection Unit Region 15 Settings:

MPU Region	Disabled
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3.4. CRC

mode: Activated

3.4.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

3.5. DAC1

OUT1 connected to: only external pin

OUT2 connected to: only external pin

3.5.1. Parameter Settings:

DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Disable *
Trigger	None
User Trimming	Factory trimming

DAC Out2 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

3.6. DAC2

OUT1 connected to: only external pin

3.6.1. Parameter Settings:

DAC Out1 Settings:

Mode selected	Normal Mode
Output Buffer	Enable
Trigger	None
User Trimming	Factory trimming

3.7. DEBUG

Debug: Trace Asynchronous Sw

3.8. MEMORYMAP

mode: Activated

3.9. RCC

High Speed Clock (HSE): BYPASS Clock Source

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

3.9.1. Parameter Settings:

Power Parameters:

SupplySource	PWR_LDO_SUPPLY
Power Regulator Voltage Scale	Power Regulator Voltage Scale 0

RCC Parameters:

TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
CSI Calibration Value	16
HSI Calibration Value	64

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	6 WS (7 CPU cycle)

PLL range Parameters:

PLL1 input frequency range	Between 4 and 8 MHz
PLL2 input frequency range	Between 8 and 16 MHz
PLL1 clock Output range	Wide VCO range
PLL2 clock Output range	Wide VCO range

3.10. RTC

mode: Activate Clock Source

3.10.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127

Synchronous Predivider value

255

3.11. SPI1

Mode: Transmit Only Master

3.11.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits *
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	23.333332 MBits/s *
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Disabled *
NSS Signal Type	Software
Fifo Threshold	Fifo Threshold 04 Data *
Tx Crc Initialization Pattern	All Zero Pattern
Rx Crc Initialization Pattern	All Zero Pattern
Nss Polarity	Nss Polarity Low
Master Ss Idleness	00 Cycle
Master Inter Data Idleness	00 Cycle
Master Receiver Auto Susp	Disable
Master Keep Io State	Master Keep Io State Disable
IO Swap	Disabled

3.12. SYS

Timebase Source: TIM6

3.13. TIM1

Clock Source : Internal Clock

Channel3: PWM Generation CH3

3.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	65535
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0

Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

3.14. TIM3

Clock Source : Internal Clock

3.14.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	31 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	33332 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

3.15. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

3.15.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	10000 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	100 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

3.16. TIM8

Clock Source : Internal Clock

Channel1: PWM Generation CH1

3.16.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	10000 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	100 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 16 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)
Trigger Event Selection TRGO2	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High
BRK Filter (4 bits value)	0
BRK Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - BRK2 Configuration:

BRK2 State	Disable
BRK2 Polarity	High
BRK2 Filter (4 bits value)	0
BRK2 Sources Configuration	
- Digital Input	Disable
- COMP1	Disable
- COMP2	Disable
- DFSDM	Disable

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

Clear Input:

Clear Input Source	Disable
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PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

3.17. TIM12

mode: Clock Source

3.17.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	15 *
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	39999 *
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

3.18. TIM15

mode: Clock Source

3.18.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	63999 *
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

3.19. USART3

Mode: Asynchronous

3.19.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable
ClockPrescaler	1
Fifo Mode	Disable
Txfifo Threshold	1 eighth full configuration
Rxfifo Threshold	1 eighth full configuration

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable

DMA on RX Error	Enable
MSB First	Disable

3.20. USB_OTG_HS

Internal FS Phy: Device_Only

Activate_VBUS: Activate-VBUS

3.20.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Enable internal IP DMA	Disabled
Physical interface	Internal Phy
Low power	Disabled
Link Power Management	Disabled
Use dedicated end point 1 interrupt	Enabled *
VBUS sensing	Enabled

3.21. STMicroelectronics.X-CUBE-TOUCHGFX.4.25.0

mode: GraphicsJjApplication

3.21.1. TouchGFX Generator:

Display:

Interface	Custom
Framebuffer Pixel Format	RGB565
Width	320 *
Height	480 *
Framebuffer Strategy	Partial Buffer - GRAM display *
Number of Blocks	3
Block Size	2048

Driver:

Application Tick Source	Custom
Use DMA2D Accelerator (ChromART)	No
Real-Time Operating System	No OS

Additional Features:

Partial Framebuffer VSync	Disabled
External Data Reader	Disabled
Vector Rendering	Disabled

Video Decoding:

Type

Disabled

3.22. USB_DEVICE

Class For HS IP: Human Interface Device Class (HID)

3.22.1. Parameter Settings:

Class Parameters:

HID_HS_BINTERVAL

0x7 *

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)

1

USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)

1

USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)

512

USBD_SELF_POWERED (Enabled self power)

Enabled

USBD_DEBUG_LEVEL (USBD Debug Level)

0: No debug message

USBD_LPM_ENABLED (Link Power Management)

1: Link Power Management supported

3.22.2. Device Descriptor:

Device Descriptor:

VID (Vendor Identifier)

1155

LANGID_STRING (Language Identifier)

English(United States)

MANUFACTURER_STRING (Manufacturer Identifier)

Warhurst *

Device Descriptor HS:

PID (Product Identifier)

22315

PRODUCT_STRING (Product Identifier)

STM32 Human interface

CONFIGURATION_STRING (Configuration Identifier)

HID Config

INTERFACE_STRING (Interface Identifier)

HID Interface

* User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_INP16	Analog mode	No pull-up and no pull-down	n/a	MUX_TH1
	PA1	ADC1_INP17	Analog mode	No pull-up and no pull-down	n/a	MUX_TH0
	PA2	ADC1_INP14	Analog mode	No pull-up and no pull-down	n/a	ADC_ISENSEF
	PA3	ADC1_INP15	Analog mode	No pull-up and no pull-down	n/a	DTH3
	PA5	ADC1_INP19	Analog mode	No pull-up and no pull-down	n/a	DAC0_UNUSED
	PC4	ADC1_INP4	Analog mode	No pull-up and no pull-down	n/a	ADC_VCCSSENSE
	PB0	ADC1_INP9	Analog mode	No pull-up and no pull-down	n/a	ADC2_UNUSED
	PB1	ADC1_INP5	Analog mode	No pull-up and no pull-down	n/a	ADC_ISENSEC
	PF11	ADC1_INP2	Analog mode	No pull-up and no pull-down	n/a	ADC_DIFF_P
	PF12	ADC1_INN2	Analog mode	No pull-up and no pull-down	n/a	ADC_DIFF_N
ADC2	PA7	ADC2_INP7	Analog mode	No pull-up and no pull-down	n/a	ADC0_UNUSED
	PC4	ADC2_INP4	Analog mode	No pull-up and no pull-down	n/a	ADC_VCCSSENSE
	PC5	ADC2_INP8	Analog mode	No pull-up and no pull-down	n/a	ADC1_UNUSED
	PF13	ADC2_INP2	Analog mode	No pull-up and no pull-down	n/a	ADC_VSENSE
	PF14	ADC2_INP6	Analog mode	No pull-up and no pull-down	n/a	DTH2
DAC1	PA4	DAC1_OUT1	Analog mode	No pull-up and no pull-down	n/a	DAC_VCCS
	PA5	DAC1_OUT2	Analog mode	No pull-up and no pull-down	n/a	DAC0_UNUSED
DAC2	PA6	DAC2_OUT1	Analog mode	No pull-up and no pull-down	n/a	DAC1_UNUSED
DEBUG	PA13	DEBUG_JTMS-SWDIO	n/a	n/a	n/a	ST_LINK_SWDIO
	PA14	DEBUG_JTCK-SWCLK	n/a	n/a	n/a	ST_LINK_SWCLK
	PB3	DEBUG_JTDO-SWO	n/a	n/a	n/a	ST_LINK_SWO
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	RTC_OSC_IN
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	RTC_OSC_OUT
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	HSE_OSC
SPI1	PG11	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	DISPL_SCK
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	DISPL_MOSI
TIM1	PA10	TIM1_CH3	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM_BUZZER
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM0

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PD13	TIM4_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	PWM1
TIM8	PC6	TIM8_CH1	Alternate Function Push Pull	No pull-up and no pull-down	Low	DISPL_LED
USART3	PB10	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	Low	ST_LINK_TX
	PB11	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	Low	ST_LINK_RX
USB_OTG_HS	PA9	USB_OTG_HS_VBUS	Input mode	No pull-up and no pull-down	n/a	USB_VBUS
	PA11	USB_OTG_HS_DM	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_DM
	PA12	USB_OTG_HS_DP	Alternate Function Push Pull	No pull-up and no pull-down	Low	USB_DP
Single Mapped Signals	PD3	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	Low	ETH_SCK
GPIO	PE6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ERROR_LED
	PC13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	STATUS_LED
	PF5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO_WARNING_HV
	PF7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPIO_I_SENSE_ENABLE
	PC0	GPIO_Output	Output Push Pull	Pull-up *	Low	ETH_CS
	PC3_C	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	ETH_RST
	PE10	GPIO_EXTI10	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	SD_CARD_DETECT
	PE13	GPIO_Output	Output Push Pull	Pull-up *	Low	SD_CS
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MATC0
	PB13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MATC1
	PB14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MATC2
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MATC3
	PD8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	FRONT_SW
	PD9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SSR_EN
	PD10	GPIO_Input	Input mode	Pull-up *	n/a	MATR0
	PD11	GPIO_Input	Input mode	Pull-up *	n/a	MATR1
	PD14	GPIO_Input	Input mode	Pull-up *	n/a	MATR2
	PD15	GPIO_Input	Input mode	Pull-up *	n/a	MATR3
	PG2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MUX_A
	PG3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MUX_B
	PG4	GPIO_Input	Input mode	Pull-up *	n/a	ENCODER_A
	PG5	GPIO_Input	Input mode	Pull-up *	n/a	ENCODER_B
	PG6	GPIO_EXTI6	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	ENCODER_SW
	PG7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	MUX_C

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TOUCH_CS
	PC11	GPIO_EXTI11	External Interrupt Mode with Falling edge trigger detection	Pull-up *	n/a	TOUCH_INT
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISPL_DC
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO15_UNUSED
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISPL_RST
	PD2	GPIO_EXTI2	External Interrupt Mode with Rising edge trigger detection	Pull-up *	n/a	ETH_INT
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO14_UNUSED
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO13_UNUSED
	PD6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO12_UNUSED
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO11_UNUSED
	PG10	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO10_UNUSED
	PG12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO9_UNUSED
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO8_UNUSED
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO7_UNUSED
	PG15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO6_UNUSED
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	DISPL_CS
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO5_UNUSED
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO4_UNUSED
	PB8	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO3_UNUSED
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO2_UNUSED
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO1_UNUSED
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPIO0_UNUSED

4.2. DMA configuration

DMA request	Stream	Direction	Priority
ADC1	DMA1_Stream0	Peripheral To Memory	High *
ADC2	DMA1_Stream1	Peripheral To Memory	High *

ADC1: DMA1_Stream0 DMA request Settings:

Mode: **Circular ***
 Use fifo: **Enable ***
 FIFO Threshold: Full
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Half Word
 Memory Data Width: Half Word
 Peripheral Burst Size: Single
 Memory Burst Size: Single

ADC2: DMA1_Stream1 DMA request Settings:

Mode: **Circular ***
 Use fifo: **Enable ***
 FIFO Threshold: Full
 Peripheral Increment: Disable
 Memory Increment: **Enable ***
 Peripheral Data Width: Half Word
 Memory Data Width: Half Word
 Peripheral Burst Size: Single
 Memory Burst Size: Single

4.3. BDMA1 configuration

nothing configured in DMA service

4.4. BDMA2 configuration

nothing configured in DMA service

4.5. MDMA configuration

nothing configured in DMA service

4.6. NVIC configuration

4.6.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
EXTI line2 interrupt	true	0	0
DMA1 stream0 global interrupt	true	0	0
DMA1 stream1 global interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
TIM3 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	0	0
TIM8 break interrupt and TIM12 global interrupt	true	0	0
TIM8 update interrupt and TIM13 global interrupt	true	0	0
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	true	15	0
USB On The Go HS End Point 1 Out global interrupt	true	0	0
USB On The Go HS End Point 1 In global interrupt	true	0	0
USB On The Go HS global interrupt	true	0	0
TIM15 global interrupt	true	0	0
PVD and PVM interrupts through EXTI line	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM4 global interrupt	unused		
SPI1 global interrupt	unused		
USART3 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM8 capture compare interrupt		unused	
FPU global interrupt		unused	
HSEM1 global interrupt		unused	
DAC2 global interrupt		unused	

4.6.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
EXTI line2 interrupt	false	true	true
DMA1 stream0 global interrupt	false	true	true
DMA1 stream1 global interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM3 global interrupt	false	true	true
EXTI line[15:10] interrupts	false	true	true
TIM8 break interrupt and TIM12 global interrupt	false	true	true
TIM8 update interrupt and TIM13 global interrupt	false	true	true
TIM6 global interrupt, DAC1_CH1 and DAC1_CH2 underrun error interrupts	false	true	true
USB On The Go HS End Point 1 Out global interrupt	false	true	true
USB On The Go HS End Point 1 In global interrupt	false	true	true
USB On The Go HS global interrupt	false	true	true
TIM15 global interrupt	false	true	true

* User modified value

5. System Views

5.1. Category view

5.1.1. Current

Middlew...

USB_DEVICE ✓

Software Pa...

X-CUBE-TOUCHGFX ✓

System C...	Anal...	Tim...	Connectiv...	Multime...	Secur...	Computi...	Trace and Deb...	Power and Ther...	Oth...
BDMA1	ADC1 ✓	RTC ✓	SP1 ✓			CRC ✓	DEBUG ✓		
BDMA2	ADC2 ✓	TIM1 ✓	USART3 ✓						
CORTEX_M7 ✓	DAC1 ✓	TIM3 ✓	USB_HS ✓						
DMA ✓	DAC2 ✓	TIM4 ✓							
GPIO ⚠		TIM8 ✓							
MDMA		TIM12 ✓							
NVIC ✓		TIM15 ✓							
RCC ✓									
SYS ✓									

6. Software Pack Report

6.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	X-CUBE-TOUCHGFX	4.25.0	Class : Graphics Group : Application Variant : TouchGFX Generator Version : 4.25.0

7. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32h7_bsd1.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32h7_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32h7-svd.zip
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7_series_product_overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_embedded_software_solutions.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_eval-tools_portfolio.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32_stm8_functional-safety-packages.pdf
Presentations	https://www.st.com/resource/en/product_presentation/stm32-stm8_software_development_tools.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers_stm32h7a3-b3_line_product-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32-family-overview.pdf
Presentations	https://www.st.com/resource/en/product_presentation/microcontrollers-stm32h7rs-lines-overview.pdf
Brochures	https://www.st.com/resource/en/brochure/brstm32h7.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32nucleo.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32trust.pdf
Flyers	https://www.st.com/resource/en/flyer/flstm32h7rs.pdf
Security Bulletin	https://www.st.com/resource/en/security_bulletin/sb0023-eucleak-protection-statement-for-stmicroelectronics-certified-products-stmicroelectronics.pdf
Application Notes	https://www.st.com/resource/en/application_note/an1709-emc-design-guide-for-stm8-stm32-and-legacy-mcus-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an2606-stm32-microcontroller-system-memory-boot-mode-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an3126-audio-and-waveform-generation-using-the-dac-in-stm32-products-stmicroelectronics.pdf

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Application Notes https://www.st.com/resource/en/application_note/an3156-usb-dfu-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4221-i2c-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4286-spi-protocol-used-in-the-stm32-bootloader-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4566-extending-the-dac-performance-of-stm32-microcontrollers-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4655-virtually-increasing-the-number-of-serial-communication-peripherals-in-stm32-applications-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4750-handling-of-soft-errors-in-stm32-applications-stmicroelectronics.pdf

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digital-microphones-using-stm32-mcus-and-mpus-stmicroelectronics.pdf

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Application Notes https://www.st.com/resource/en/application_note/an5073-receiving-spdif-audio-stream-with-the-stm32f4f7h7-series-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5307-getting-started-with-stm32h7a37b3-line-and-stm32h7b0-value-line-microcontroller-hardware-development-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an4899-stm32-microcontroller-gpio-hardware-settings-and-lowpower-consumption-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5450-stm32h7a37b3-lines-and-stm32h7b0-value-line-smart-power-management-expansion-package-for-stm32cube-stmicroelectronics.pdf

Application Notes https://www.st.com/resource/en/application_note/an5612-esd-protection-of-stm32-mcus-and-mpus-stmicroelectronics.pdf

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Application Notes https://www.st.com/resource/en/application_note/an5342--how-to-use-error-correction-code-ecc-management-for-internal-memories-protection-on-stm32-mcus-stmicroelectronics.pdf

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- Application Notes https://www.st.com/resource/en/application_note/an5036-guidelines-for-thermal-management-on-stm32-applications-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an5405-how-to-use-fdcan-bootloader-protocol-on-stm32-mcus-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4230-introduction-to-random-number-generation-validation-using-the-nist-statistical-test-suite-for-stm32-mcus-and-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an2867-guidelines-for-oscillator-design-on-stm8afals-and-stm32-mcus-mpus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4013-introduction-to-timers-for-stm32-mcus-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4635-how-to-optimize-lpuart-power-consumption-on-stm32-mcus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4759-introduction-to-using-the-hardware-realtime-clock-rtc-and-the-tamper-management-unit-tamp-with-stm32-mcus-stmicroelectronics.pdf
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- Application Notes https://www.st.com/resource/en/application_note/an4908-getting-started-with-uart-automatic-baud-rate-detection-for-stm32-mcus-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4943-how-to-use-chromart-accelerator-to-refresh-an-lcd-tft-display-on-stm32-mcus-stmicroelectronics.pdf

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