







LM393B, LM2903B, LM193, LM293, LM293A, LM393, LM393A, LM2903, LM2903V SLCS005AF - OCTOBER 1979 - REVISED AUGUST 2023

LM393B, LM2903B, LM193, LM293, LM393 and LM2903 Dual Comparators

1 Features

- NEW LM393B and LM2903B
- Improved specifications of B-version
 - Maximum rating: up to 38 V
 - ESD rating (HBM): 2k V
 - Low input offset: 0.37 mV
 - Low input bias current: 3.5 nA
 - Low supply-current: 200 μA per comparator
 - Faster response time of 1 µsec
 - Extended temperature range for LM393B
 - Available in tiny 2 x 2mm WSON package
- B-version is drop-in replacement for LM293, LM393 and LM2903, A and V versions
- · Common-mode input voltage range includes
- Differential input voltage range equal to maximumrated supply voltage: ±38 V
- Low output saturation voltage
- Output compatible with TTL, MOS, and CMOS

2 Applications

- Vacuum robot
- Single phase UPS
- Server PSU
- Cordless power tool
- Wireless infrastructure
- **Applicances**
- **Building automation**
- Factory automation & control
- Motor drives
- Infotainment & cluster

3 Description

The LM393B and LM2903B devices are the next generation versions of the industry-standard LM393 and LM2903 comparator family. These next generation B-version comparators feature lower offset voltage, higher supply voltage capability, lower supply current, lower input bias current, lower propagation delay, and improved 2 kV ESD performance and input ruggedness through dedicated ESD clamps. The LM393B and LM2903B can drop-in replace the LM293, LM393 and LM2903, for both "A" and "V" grades.

All devices consist of two independent voltage comparators that are designed to operate from a single power supply over a wide range of voltages. Quiescent current is independent of the supply voltage.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)						
LM393B, LM2903B, LM193, LM293, LM293A, LM393, LM393A, LM2903, LM2903V, LM2903AV	SOIC (8)	4.90 mm x 3.91 mm						
LM393B, LM2903B, LM293, LM293A, LM393, LM393A, LM2903	VSSOP (8)	3.00 mm x 3.00 mm						
LM293, LM393, LM393A, LM2903	PDIP (8)	9.81 mm × 6.35 mm						
LM393, LM393A, LM2903	SO (8)	6.20 mm x 5.30 mm						
LM393B, LM2903B, LM393, LM393A, LM2903, LM2903V, LM2903AV	TSSOP (8)	3.00 mm x 4.40 mm						
LM393B, LM2903B	SOT-23 (8)	2.90 mm x 1.60 mm						
LM393B, LM2903B	WSON (8)	2.00 mm × 2.00 mm						

For all available packages, see the orderable addendum at the end of the data sheet.

Family Comparison Table

Specification	LM393B	LM2903B	LM393 LM393A	LM2903	LM2903V LM2903AV	LM193	LM293 LM293A	Units
Supply Voltage	2 to 36	2 to 36	2 to 30	2 to 30	2 to 32	2 to 30	2 to 30	V
Total Supply Current (5V to 36V max)	0.6 to 0.8	0.6 to 0.8	1 to 2.5	1 to 2.5	1 to 2.5	1 to 2.5	1 to 2.5	mA
Temperature Range	-40 to 85	-40 to 125	0 to 70	-40 to 125	-40 to 125	-55 to 125	-25 to 85	°C
ESD (HBM)	2000	2000	1000	1000	1000	1000	1000	V
Offset Voltage (Max over temp)	± 4	± 4	± 9 ± 4	± 15	± 15 ± 4	± 9	± 9 ± 4	mV
Input Bias Current (typ / max)	3.5 / 25	3.5 / 25	25 / 250	25 / 250	25 / 250	25 / 100	25 / 250	nA
Response Time (typ)	1	1	1.3	1.3	1.3	1.3	1.3	µsec



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C	hanges from Revision Z (October 2017) to Revision AA (September 2019)	Page
•	Added "B" devices with various text changes throughout datasheet	1
	Deleted from Device Information old LM193 CDIP and LCCC package references and drawings. These	
	on the LM139-MIL data sheet	1
•	Added "B" devices Thermal Information table	6
•	Added "B" device electrical tables	6
	Added "B" device graphs	



5 Pin Configuration and Functions

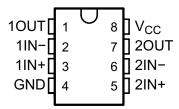
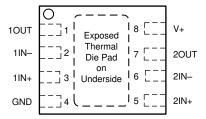


Figure 5-1. D, DGK, JG, P, PS, DDF or PW Package 8-Pin SOIC, VSSOP, PDIP, SO, or TSSOP Top View



Connect thermal pad directly to GND pin.

Figure 5-2. DSG Package 8-Pin WSON With Exposed Pad Top View

PIN SOIC, VSSOP, **DESCRIPTION** I/O NAME PDIP, SO, DDF and DSG TSSOP **10UT** 1 1 Output Output pin of comparator 1 1IN-2 2 Input Negative input pin of comparator 1 1IN+ 3 3 Input Positive input pin of comparator 1 GND 4 4 Ground 2IN+ 5 5 Positive input pin of comparator 2 Input 2IN-6 6 Input Negative input pin of comparator 2 2OUT 7 7 Output pin of comparator 2 Output V_{CC} 8 8 Positive Supply Thermal PAD Connect directly to GND pin Pad

Table 5-1. Pin Functions



6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	1 3 1	,	MIN	MAX	UNIT
.,	V _{CC} Supply voltage ⁽²⁾	Non-B Versions	-0.3	36	V
V _{CC}	Supply voltage	B Versions Only	-0.3	38	v
.,	Differential input voltage(3)	Non-B Versions	-36	36	V
V _{ID}	Differential input voltage ⁽³⁾	B Versions Only -38	38	v	
.,	Innut valtage (either innut)	ut voltage (either input) Non-B Versions -0.3	36	V	
VI	input voltage (either input)		38	v	
I _{IK}	Input current ⁽⁵⁾	,		-50	mA
.,	Outrot wells as	Non-B Versions	0.0	36	V
Vo	Output voltage	B Versions Only	-0.3	38	v
	Outside summer	Non-B Versions		20	4
lo	Output current	B Versions Only		25	mA
I _{SC}	Duration of output short circuit to ground ⁽⁴⁾		Unli	mited	
TJ	Operating virtual-junction temperature			150	°C
T _{stg}	Storage temperature		-65	150	°C

⁽¹⁾ Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Production Processing Does Not Necessarily Include Testing of All Parameters.

- (2) All voltage values, except differential voltages, are with respect to network ground.
- (3) Differential voltages are at IN+ with respect to IN-.
- (4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.
- (5) Input current flows thorough parasitic diode to ground and turns on parasitic transistors that increases I_{CC} and may cause output to be incorrect. Normal operation resumes when input current is removed.

6.2 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
	non-V devices	2	30	
Supply voltage, $V_S = (V+) - (V-)$	V devices	2	32	V
	"B" version devices	2	36	
Input voltage range V	non-B devices	0	(V+) - 2.0	V
Input voltage range, V _{IVR}	"B" version devices	-0.1	(V+) - 2.0	V
	LM193	-55	125	
	LM2903, LM2903V, LM2903AV, LM2903B	-40	125	
Ambient temperature, T _A	LM393B	-40	85	°C
	LM293, LM293A	-25	85	
	LM393, LM393A	0	70	



6.3 Thermal Information: LM193

	THERMAL METRIC ⁽¹⁾				
			UNIT		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.4	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	70	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	64.9	°C/W		
ΨЈТ	Junction-to-top characterization parameter	20.3	°C/W		
ΨЈВ	Junction-to-board characterization parameter	64.5	°C/W		
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W		

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.4 Thermal Information: LM293, LM393, LM2903 (all 'V' and 'A' suffixes)

	THERMAL METRIC ⁽¹⁾		DGK (VSSOP)	P (PDIP)	PS (SO)	PW (TSSOP)	UNIT
		8 pin	8 pin	8 pin	8 pin	8 pin	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	131.8	199.4	73.7	139	194.1	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	78.4	90.2	62.6	98.9	77.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.2	120.8	50.8	83.7	123.0	°C/W
ΨЈТ	Junction-to-top characterization parameter	26.5	21.5	39.2	47.4	13.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	71.1	119.1	50.7	83	121.3	°C/W

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.5 Thermal Information: LM393B and LM2903B

				LM393B, LM2903B					
	THERMAL METRIC ⁽¹⁾		PW (TSSOP)	DGK (VSSOP)	DDF (SOT-23)	DSG (WSON)	UNIT		
			8 pin	8 pin	8 pin	8 pins			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	148.5	200.6	193.7	197.9	96.9	°C/W		
R _{0JC(top)}	Junction-to-case (top) thermal resistance	90.2	89.6	82.9	119.2	119.0	°C/W		
$R_{\theta JB}$	Junction-to-board thermal resistance	91.8	131.3	115.5	115.4	63.1	°C/W		
ΨЈТ	Junction-to-top characterization parameter	38.5	22.1	20.8	19.4	12.4	°C/W		
Ψ_{JB}	Junction-to-board characterization parameter	91.1	129.6	113.9	113.7	63.0	°C/W		
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	-	-	37.8	°C/W		

⁽¹⁾ For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.

6.6 ESD Ratings

			VALUE	UNIT					
LM393B	LM393B and LM2903B Only								
.,	/	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	.,					
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	\ \ \					
All Othe	All Other Versions								
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1000	V					
V _(ESD)	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±750						

⁽¹⁾ JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

⁽²⁾ JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.



6.7 Electrical Characteristics LM393B

 $V_S = 5 \text{ V}$, $V_{CM} = (V_-)$; $T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Innut offeet voltage	V _S = 5 to 36V	-2.5	±0.37	2.5	
V	Input offset voltage	$V_S = 5 \text{ to } 36V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	-4		4	mV
V_{IO}	Input offset voltage, DGK	V _S = 5 to 36V	-3.5	±0.37	3.5	IIIV
	package only	$V_S = 5 \text{ to } 36V, T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	-5		5	
ı	Input bias current			-3.5	-25	nA
I _B	input bias current	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$			-50	nA
ı	Input offset current		-10	±0.5	10	nA
los	input onset current	$T_A = -40^{\circ}C \text{ to } +85^{\circ}C$	-25		25	nA
.,	Common mode range (1)	V _S = 3 to 36V	(V-)		(V+) – 1.5	V
V_{CM}	Common mode range V	$V_S = 3 \text{ to } 36V, T_A = -40^{\circ}\text{C to } +85^{\circ}\text{C}$	(V-)		(V+) - 2.0	V
A _{VD}	Large signal differential voltage amplification	$V_S = 15V$, $V_O = 1.4V$ to 11.4V; $R_L \ge 15k$ to $(V+)$	50	200		V/mV
	Low level output Voltage	I _{SINK} ≤ 4mA, V _{ID} = -1V		110	400	mV
V _{OL}	{swing from (V–)}	$I_{SINK} \le 4mA, V_{ID} = -1V$ $T_A = -40$ °C to +85°C			550	mV
	High-level output leakage	(V+) = V _O = 5 V; V _{ID} = 1V		0.1	20	nA
I _{OH-LKG}	current	(V+) = V _O = 36V; V _{ID} = 1V		0.3	50	nA
I _{OL}	Low level output current	$V_{OL} = 1.5V; V_{ID} = -1V; V_{S} = 5V$	6	21		mA
	Quiescent current (all	V _S = 5 V, no load		400	600	μA
IQ	comparators)	V _S = 36 V, no load, T _A = -40°C to +85°C		550	800	μA

⁽¹⁾ The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.



6.8 Electrical Characteristics LM2903B

 $V_S = 5 \text{ V}, V_{CM} = (V_-); T_A = 25^{\circ}\text{C}$ (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input offset voltage	V _S = 5 to 36V	-2.5	±0.37	2.5	
V	Input offset voltage	$V_S = 5 \text{ to } 36V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C$	-4		4	mV
V_{IO}	Input offset voltage, DGK	V _S = 5 to 36V	-3.5	±0.37	3.5	IIIV
	package only	$V_S = 5 \text{ to } 36V, T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	-5		5	
	Input bias current			-3.5	-25	nA
I _B	input bias current	$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$			-50	nA
ı	Input offset current		-10	±0.5	10	nA
los	input onset current	$T_A = -40^{\circ}C \text{ to } +125^{\circ}C$	-25		25	nA
.,	Common mode range (1)	V _S = 3 to 36V	(V-)		(V+) – 1.5	V
V_{CM}	Common mode range (**)	$V_S = 3 \text{ to } 36V, T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$	(V-)		(V+) - 2.0	V
A _{VD}	Large signal differential voltage amplification	$V_S = 15V$, $V_O = 1.4V$ to 11.4V; $R_L \ge 15k$ to (V+)	50	200		V/mV
	Low level output Voltage	I _{SINK} ≤ 4mA, V _{ID} = -1V		110	400	mV
V _{OL}	{swing from (V–)}	$I_{SINK} \le 4\text{mA}, V_{ID} = -1V$ $T_A = -40^{\circ}\text{C to } +125^{\circ}\text{C}$			550	mV
1	High-level output leakage	(V+) = V _O = 5 V; V _{ID} = 1V		0.1	20	nA
I _{OH-LKG}	current	(V+) = V _O = 36V; V _{ID} = 1V		0.3	50	nA
I _{OL}	Low level output current	V _{OL} = 1.5V; V _{ID} = -1V; V _S = 5V	6	21		mA
	Quiescent current (all	V _S = 5 V, no load		400	600	μA
IQ	comparators)	V _S = 36 V, no load, T _A = -40°C to +125°C		550	800	μA

⁽¹⁾ The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2V$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

6.9 Switching Characteristics LM393B and LM2903B

 V_S = 5V, $V_{OPULLUP}$ = 5V, V_{CM} = $V_S/2$, C_L = 15pF, R_L = 5.1k Ohm, T_A = 25°C (unless otherwise noted).

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{response}	Propagation delay time, high-to-low; TTL input signal ⁽¹⁾	TTL input with V _{ref} = 1.4V		300		ns
t _{response}	Propagation delay time, high-to-low; Small scale input signal ⁽¹⁾	Input overdrive = 5mV, Input step = 100mV		1000		ns

(1) High-to-low and low-to-high refers to the transition at the input.



6.10 Electrical Characteristics for LM193, LM293, and LM393 (without A suffix)

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

	PARAMETER	TEST CO	ONDITIONS	T _A ⁽¹⁾	LM1	193			293 393		UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
		$V_{CC} = 5 \text{ V to } 3$		25°C		2	5		2	5	
V _{IO}	Input offset voltage	$V_{IC} = V_{ICR} min$ $V_{O} = 1.4 V$,	Full range			9			9	mV
1	Input offset current	V _O = 1.4 V		25°C		3	25		5	50	nA
I _{IO}	input onset current	V ₀ - 1.4 V		Full range			100			250	IIA
	Input bias current	V _O = 1.4 V		25°C		-25	-100		-25	-250	nA
I _{IB}	iliput bias current	V ₀ - 1.4 V		Full range			-300			-400	IIA
	Common-mode input-voltage			25°C	0 to V _{CC} – 1.5			0 to V _{CC} – 1.5			V
V _{ICR}	range ⁽²⁾			Full range	0 to V _{CC} – 2			0 to V _{CC} – 2			v
A _{VD}	Large-signal differential-voltage amplification	V_{CC} = 15 V, V_{O} = 1.4 V to R_{L} ≥ 15 k Ω to		25°C	50	200		50	200		V/mV
	High level output ourrent	V _{OH} = 5 V	V _{ID} = 1 V	25°C		0.1			0.1	50	nA
Іон	High-level output current	V _{OH} = 30 V	V _{ID} = 1 V	Full range			1			1	μA
.,	Low-level output voltage	I _{OL} = 4 mA,	V _{ID} = -1 V	25°C		150	400		130	400	mV
V _{OL}	Low-level output voltage	I _{OL} = 4 mA,	v _{ID} = -1 v	Full range			700			700	mv
I _{OL}	Low-level output current	V _{OL} = 1.5 V,	V _{ID} = -1 V	25°C	6			6			mA
1	Cumply ourrent	R ₁ = ∞	V _{CC} = 5 V	25°C		0.8	1		0.45	1	mA
Icc	Supply current	I'L	V _{CC} = 30 V	Full range			2.5		0.55	2.5	IIIA

⁽¹⁾ Full range (minimum or maximum) for LM193 is -55°C to 125°C, for LM293 is -25°C to 85°C, and for LM393 is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

⁽²⁾ The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.



6.11 Electrical Characteristics for LM293A and LM393A

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

	PARAMETER	TEST	CONDITIONS	T _A ⁽¹⁾	LM29 LM39		UNIT	
					MIN	TYP	MAX	
\/	Innut offect veltage	V _{CC} = 5 V to 30 V,	V _O = 1.4 V	25°C		1	2	mV
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR(min)}$	-	Full range			4	IIIV
	Input offset current	V _O = 1.4 V		25°C		5	50	nA
I _{IO}	input onset current	V ₀ - 1.4 V		Full range			150	IIA
	Input bias current	V _O = 1.4 V		25°C		-25	-250	nA
I _{IB}	input bias current	V ₀ - 1.4 V		Full range			-400	IIA
.,	O(2)			25°C	0 to V _{CC} – 1.5			
V _{ICR}	Common-mode input-voltage range ⁽²⁾			Full range	0 to V _{CC} – 2			V
A _{VD}	Large-signal differential-voltage amplification	$V_{CC} = 15 \text{ V}, V_{O} = 100 \text{ R}_{L} \ge 15 \text{ k}\Omega \text{ to } V_{CC}$		25°C	50	200		V/mV
	High-level output current	V _{OH} = 5 V,	V _{ID} = 1 V	25°C		0.1	50	nA
I _{OH}	righ-level output current	V _{OH} = 30 V,	V _{ID} = 1 V	Full range			1	μA
1/	Low-level output voltage	l = 4 mΛ	V _{ID} = -1 V	25°C		110	400	mV
V_{OL}	Low-level output voltage	$I_{OL} = 4 \text{ mA},$	v _{ID} – – 1 v	Full range			700	liiv
I _{OL}	Low-level output current	V _{OL} = 1.5 V,	$V_{ID} = -1 V$,	25°C	6			mA
	Cumply augment	D	V _{CC} = 5 V	25°C		0.60	1	A
I _{CC}	Supply current	R _L = ∞	V _{CC} = 30 V	Full range		0.72	2.5	mA

⁽¹⁾ Full range (minimum or maximum) for LM293A is -25°C to 85°C, and for LM393A is 0°C to 70°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

⁽²⁾ The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by $V_{CC} - 2V$. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.



6.12 Electrical Characteristics for LM2903, LM2903V, and LM2903AV

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

	DADAMETED	TEST COL	IDITIONS	- (1)	LM2903, L	M2903	3V	LM290	UNIT		
	PARAMETER	TEST CON	IDITIONS	T _A (1)	MIN	TYP	MAX	MIN	TYP	MAX	UNII
		$V_{CC} = 5 \text{ V to MAX}^{(2)}$,		25°C		2	7		1	2	.,
V _{IO}	Input offset voltage	$V_O = 1.4 \text{ V},$ $V_{IC} = V_{ICR(min)},$		Full range			15			4	mV
l. a	Input offset current	V _O = 1.4 V		25°C		5	50		5	50	nA
I _{IO}	input onset current	VO - 1.4 V		Full range			200			200	ПА
I _{IB}	Input bias current	V _O = 1.4 V		25°C		-25	-250		-25	-250	nA
ııB	input bias current	VO - 1.4 V		Full range			-500			-500	ША
V	Common-mode input-			25°C	0 to V _{CC} – 1.5			0 to V _{CC} – 1.5			V
V _{ICR}	voltage range ⁽³⁾			Full range	0 to V _{CC} – 2			0 to V _{CC} - 2			V
A _{VD}	Large-signal differential- voltage amplification	V_{CC} = 15 V, V_{O} = 1.4 V R_{L} ≥ 15 kΩ to V_{CC}	V to 11.4 V,	25°C	25	100		25	100		V/mV
1	High-level output current	V _{OH} = 5 V,	V_{ID} = 1 V	25°C		0.1	50		0.1	50	nA
I _{OH}	r ligh-level output current	$V_{OH} = V_{CC} MAX^{(2)}$,	V _{ID} = 1 V	Full range			1			1	μΑ
V-	Low-level output voltage	I _{OL} = 4 mA,	V _{ID} = -1 V,	25°C		150	400		150	400	mV
V _{OL}	Low-level output voltage	I _{OL} – 4 IIIA,	ν _{ID} – – ι ν,	Full range			700			700	IIIV
I _{OL}	Low-level output current	V _{OL} = 1.5 V,	V _{ID} = -1 V	25°C	6			6			mA
	Cupply ourrant	R _L = ∞	V _{CC} = 5 V	25°C		0.8	1		0.8	1	mA
I _{CC}	Supply current	NL - w	V _{CC} = MAX	Full range			2.5			2.5	IIIA

⁽¹⁾ Full range (minimum or maximum) for LM2903 is -40°C to 125°C. All characteristics are measured with zero common-mode input voltage, unless otherwise specified.

6.13 Switching Characteristics: LM193, LM239, LM393, LM2903, all 'A' and 'V' versions

 $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST COND	ITIONS	TYP	UNIT
Pagnanaa tima	R _L connected to 5 V through 5.1 kΩ,	100-mV input step with 5-mV overdrive	1.3	
Response time	$C_L = 15 \text{ pF}^{(1) (2)}$	TTL-level input step	0.3	μs

⁽¹⁾ C_L includes probe and jig capacitance.

⁽²⁾ V_{CC} MAX = 30 V for non-V devices and 32 V for V-suffix devices.

⁽³⁾ The voltage at either input should not be allowed to go negative by more than 0.3 V otherwise output may be incorrect and excessive input current can flow. The upper end of the common-mode voltage range is limited by V_{CC} – 2V. However only one input needs to be in the valid common mode range, the other input can go up the maximum V_{CC} level and the comparator provides a proper output state. Either or both inputs can go to maximum V_{CC} level without damage.

⁽²⁾ The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.



6.14 Typical Characteristics, LMx93, LM2903 (all 'V' and 'A' suffixes)

 T_A = 25°C, V_S = 5V, R_{PULLUP} =5.1k, C_L = 15 pF, V_{CM} =0V unless otherwise noted.

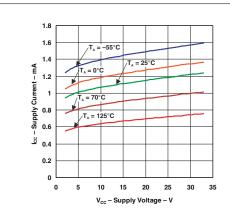


Figure 6-1. Supply Current vs Supply Voltage

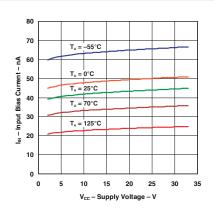


Figure 6-2. Input Bias Current vs Supply Voltage

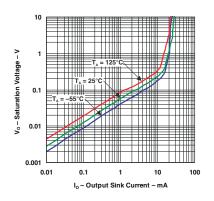


Figure 6-3. Output Saturation Voltage

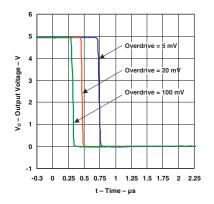


Figure 6-4. Response Time for Various Overdrives Negative Transition

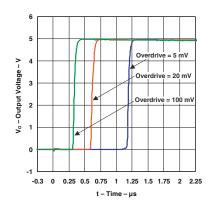
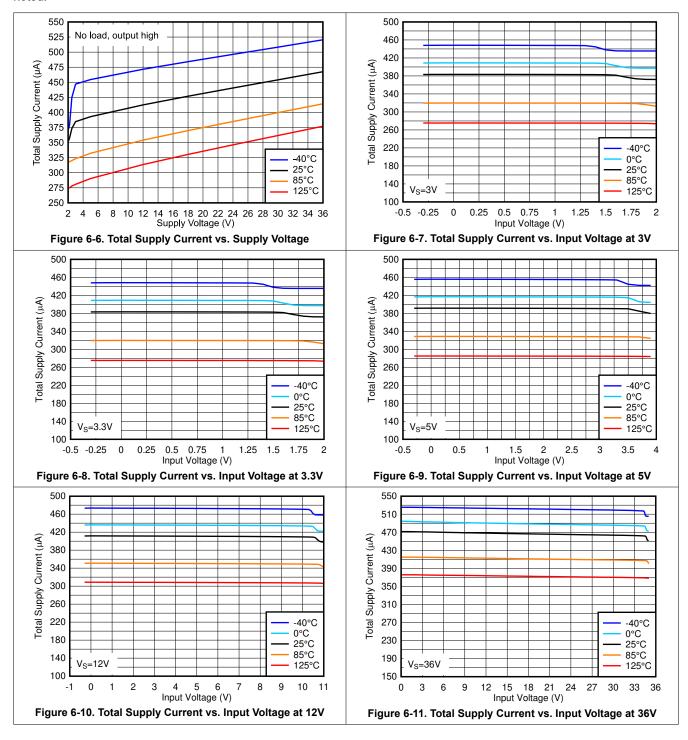


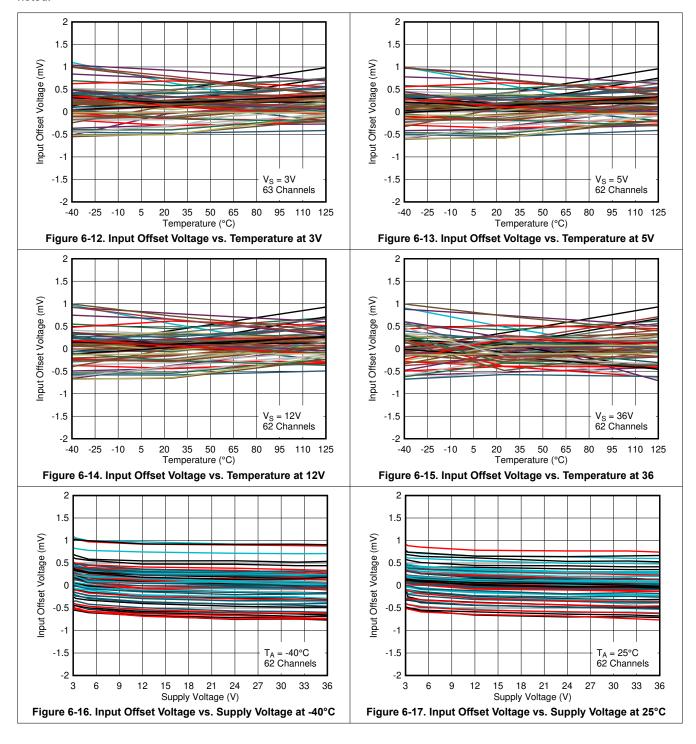
Figure 6-5. Response Time for Various Overdrives Positive Transition



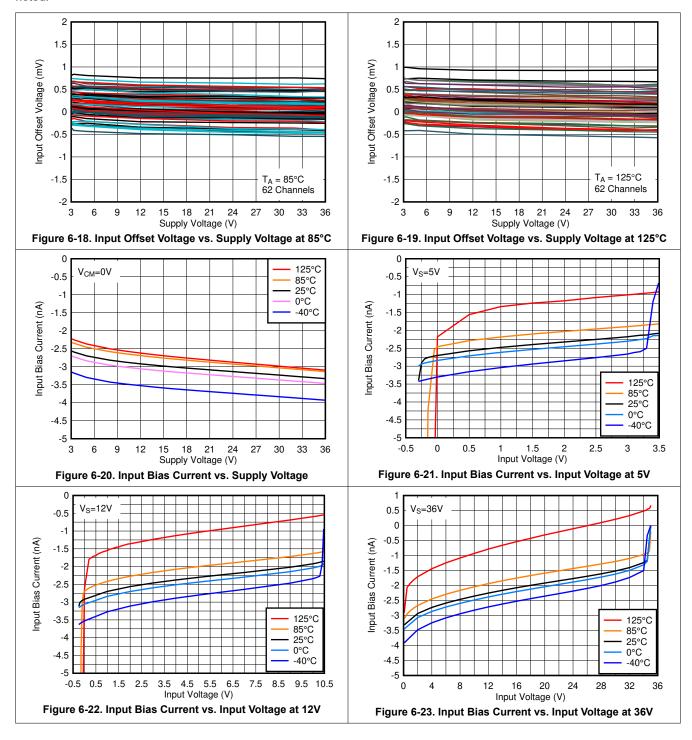
6.15 Typical Characteristics, LM393B and LM2903B



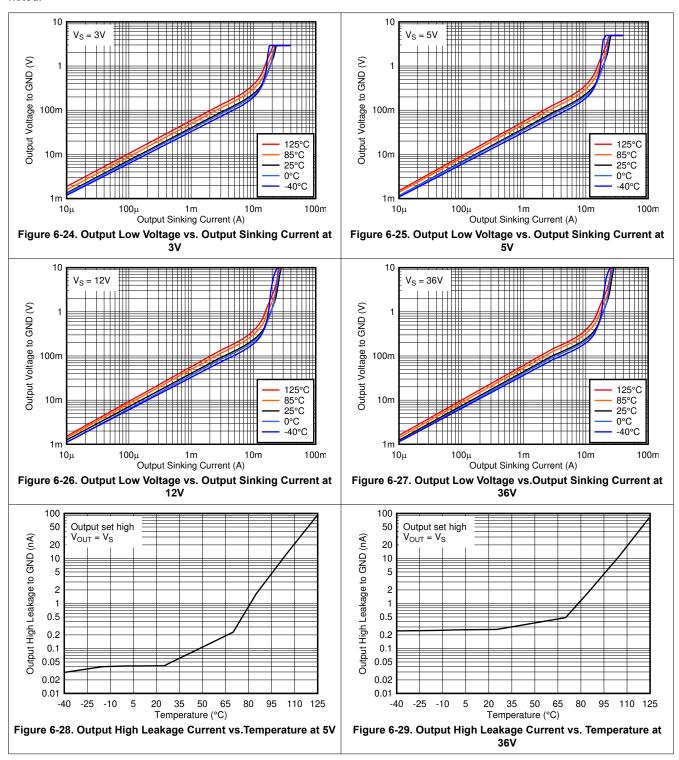




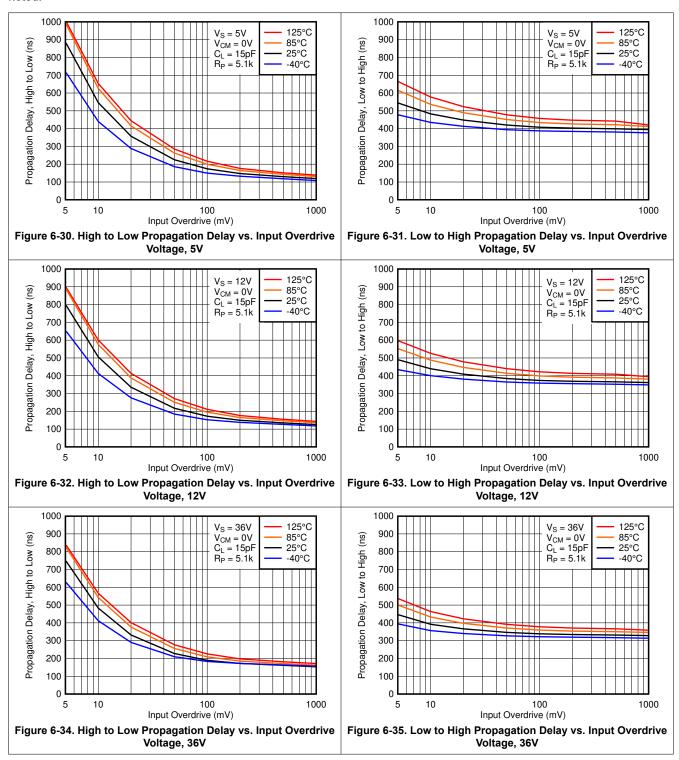














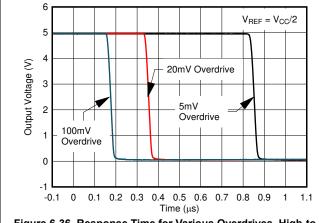


Figure 6-36. Response Time for Various Overdrives, High-to-Low Transition

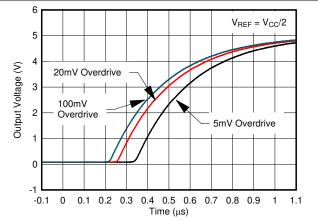


Figure 6-37. Response Time for Various Overdrives, Low-to-High Transition



7 Detailed Description

7.1 Overview

These dual comparators have the ability to operate up to absolute maximum of 36 V (38 V for the "B" version) on the supply pin. This device has proven ubiquity and versatility across a wide range of applications. This is due to very wide supply voltages range, low Iq and fast response of the devices.

The open-drain output allows the user to configure the output's logic high voltage (V_{OH}) and can be used to enable the comparator to be used in AND functionality.

7.2 Functional Block Diagram

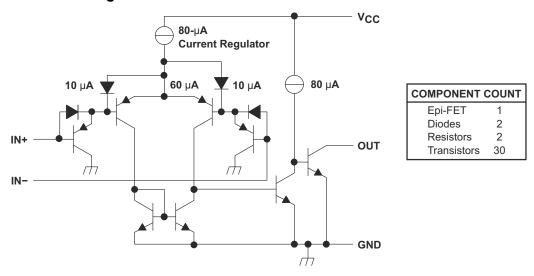


Figure 7-1. Schematic (Each Comparator)

7.3 Feature Description

The comparator consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing the comparator to accurately function from ground to V_{CC} – 1.5 V input. Allow for V_{CC} – 2 V at cold temperature.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN sinks current when the negative input voltage is higher than the positive input voltage and the offset voltage. The V_{OL} is resistive and scales with the output current. See Figure 6-3 for V_{OL} values with respect to the output current.

7.4 Device Functional Modes

7.4.1 Voltage Comparison

The device operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pullup) based on the input differential polarity.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is typically used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes this comaprator optimal for level shifting to a higher or lower voltage.

8.2 Typical Application

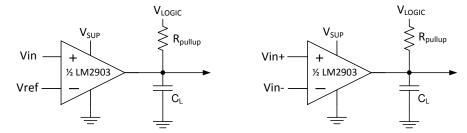


Figure 8-1. Single-Ended and Differential Comparator Configurations

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

EXAMPLE VALUE DESIGN PARAMETER Input Voltage Range 0 V to Vsup-2 V Supply Voltage 4.5 V to V_{CC} maximum Logic Supply Voltage 0 V to V_{CC} maximum Output Current (RPULLUP) 1 µA to 4 mA 100 mV Input Overdrive Voltage 2.5 V Reference Voltage Load Capacitance (C_L) 15 pF

Table 8-1. Design Parameters

8.2.2 Detailed Design Procedure

When using the device in a general comparator application, determine the following:

- Input Voltage Range
- Minimum Overdrive Voltage
- · Output and Drive Current
- Response Time

8.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is below 25°C the V_{ICR} can range from 0 V to V_{CC} – 2.0 V. This limits the input



voltage range to as high as V_{CC} - 2.0 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

The following is a list of input voltage situation and their outcomes:

- 1. When both IN- and IN+ are both within the common-mode range:
 - a. If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
 - b. If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
- 2. When IN- is higher than common-mode and IN+ is within common-mode, the output is low and the output transistor is sinking current
- 3. When IN+ is higher than common-mode and IN- is within common-mode, the output is high impedance and the output transistor is not conducting
- 4. When IN- and IN+ are both higher than common-mode, see Section 2 of Application Design Guidelines for LM339, LM393, TL331 Family Comparators Including the New B-versions.

8.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). To make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 8-2 and Figure 8-3 show positive and negative response times with respect to overdrive voltage.

8.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pullup voltage. The output current produces a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use *Section* 6.14 to determine V_{OL} based on the output current.

The output current can also effect the transient response. See Section 8.2.2.4 for more information.

8.2.2.4 Response Time

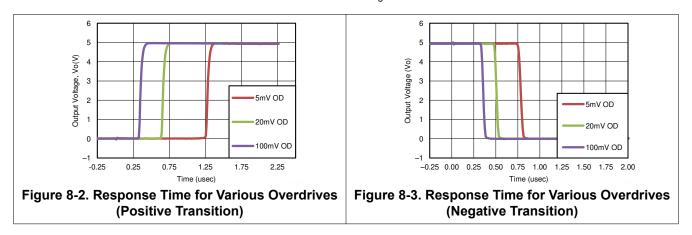
Response time is a function of input over drive. See Section 8.2.3 for typical response times. The rise and falls times can be determined by the load capacitance (C_L), load/pullup resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The rise time (τ_R) is approximately τ_R ~ R_{PULLUP} × C_L
- The fall time (τ_F) is approximately τ_F ~ R_{CE} × C_L
 - R_{CE} can be determine by taking the slope of Section 6.14 in its linear region at the desired temperature, or by dividing the V_{OL} by I_{out}



8.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic} , R_{PULLUP} = 5.1 k Ω , and 50 pF scope probe.



8.2.4 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, TI recommends to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the input common-mode range of the comparator and create an inaccurate comparison.

8.2.5 Layout

8.2.5.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches. To achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

Minimize coupling between outputs and inverting inputs to prevent output oscillations. Do not run output and inverting input traces in parallel unless there is a V_{CC} or GND trace between output and inverting input traces to reduce coupling. When series resistance is added to inputs, place resistor close to the device.

8.2.5.2 Layout Example

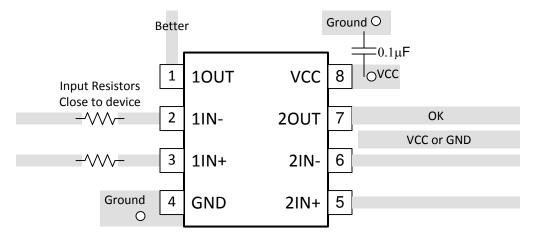


Figure 8-4. LM2903 Layout Example



9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.





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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM193DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM193DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LM193	Samples
LM2903AVQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903AVQPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903AV	Samples
LM2903BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903B	Samples
LM2903BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903B	Samples
LM2903BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903B	Samples
LM2903BIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	903B	Samples
LM2903BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903B	Samples
LM2903DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG SN	Level-1-260C-UNLIM	-40 to 125	(MAP, MAS, MAU)	Samples
LM2903DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM2903	Samples
LM2903P	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	LM2903P	Samples
LM2903PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903	Samples
LM2903QD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2903Q	Samples





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM2903VQDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM2903VQPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L2903V	Samples
LM293ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	(MDP, MDS, MDU)	Samples
LM293ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-25 to 85		Samples
LM293ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	Samples
LM293ADRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-25 to 85	LM293A	
LM293D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-25 to 85	LM293	
LM293DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	(MCP, MCS, MCU)	Samples
LM293DGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-25 to 85		Samples
LM293DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-25 to 85	LM293	Samples
LM293P	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	-25 to 85	LM293P	Samples
LM293PE4	ACTIVE	PDIP	Р	8	50	TBD	Call TI	Call TI	-25 to 85		Samples
LM393ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU NIPDAUAG	Level-1-260C-UNLIM	0 to 70	(M8P, M8S, M8U)	Samples
LM393ADGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
LM393ADR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM393A	Samples
LM393AP	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM393AP	Samples
LM393APE4	ACTIVE	PDIP	Р	8	50	TBD	Call TI	Call TI	0 to 70		Samples
LM393APSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393APWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L393A	Samples
LM393BIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	393B	Samples
LM393BIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	393B	Samples

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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
LM393BIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM393B	Samples
LM393BIDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	393B	Samples
LM393BIPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LM393B	Samples
LM393D	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	LM393	
LM393DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	(M9P, M9S, M9U)	Samples
LM393DGKRG4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
LM393DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393DRG3	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	LM393	Samples
LM393P	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE3	ACTIVE	PDIP	Р	8	50	RoHS & Non-Green	SN	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PE4	ACTIVE	PDIP	Р	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	LM393P	Samples
LM393PS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG3	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 70	L393	Samples
LM393PWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	L393	Samples

⁽¹⁾ The marketing status values are defined as follows: **ACTIVE:** Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available. **OBSOLETE:** TI has discontinued the production of the device.

PACKAGE OPTION ADDENDUM

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(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LM2903, LM2903B, LM293:

Automotive: LM2903-Q1, LM2903B-Q1

Enhanced Product : LM293-EP

NOTE: Qualified Version Definitions:

- Automotive Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product Supports Defense, Aerospace and Medical Applications



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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM193DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903AVQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903AVQPWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903BIDDFR	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2903BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903BIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM2903BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2903DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903PSR	so	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
LM2903VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM2903VQPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM293DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM293DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393APSR	so	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1



PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM393BIDDFR	SOT-23- THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM393BIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393BIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393BIDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
LM393BIPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM393DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG3	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM393PSR	so	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
LM393PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG3	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
LM393PWRG4	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1





*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM193DR	SOIC	D	8	2500	350.0	350.0	43.0
LM2903AVQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQDRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2903AVQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903AVQPWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM2903BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903BIDR	SOIC	D	8	2500	356.0	356.0	35.0
LM2903BIDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903BIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
LM2903BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM2903DR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903DR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM2903DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM2903DRG4	SOIC	D	8	2500	340.5	338.1	20.6



PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm
LM2903PSR	so	PS	8	2000	356.0	356.0	35.0
LM2903PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM2903PWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903VQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQDR	SOIC	D	8	2500	340.5	338.1	20.6
LM2903VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM2903VQPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM293ADGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM293ADGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM293ADGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LM293ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM293ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM293ADRG4	SOIC	D	8	2500	356.0	356.0	35.0
LM293DGKR	VSSOP	DGK	8	2500	370.0	355.0	55.0
LM293DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM293DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM293DR	SOIC	D	8	2500	356.0	356.0	35.0
LM293DR	SOIC	D	8	2500	356.0	356.0	35.0
LM293DR	SOIC	D	8	2500	340.5	338.1	20.6
LM293DR	SOIC	D	8	2500	340.5	338.1	20.6
LM293DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM393ADGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
LM393ADGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
LM393ADGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM393ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM393ADR	SOIC	D	8	2500	340.5	338.1	20.6
LM393ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM393ADR	SOIC	D	8	2500	356.0	356.0	35.0
LM393ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393ADRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393APSR	so	PS	8	2000	356.0	356.0	35.0
LM393APWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393APWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393BIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
LM393BIDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM393BIDR	SOIC	D	8	2500	356.0	356.0	35.0
LM393BIDR	SOIC	D	8	2500	340.5	338.1	20.6
LM393BIDSGR	WSON	DSG	8	3000	210.0	185.0	35.0



PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM393BIPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
LM393DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
LM393DGKR	VSSOP	DGK	8	2500	346.0	346.0	35.0
LM393DR	SOIC	D	8	2500	340.5	338.1	20.6
LM393DR	SOIC	D	8	2500	340.5	338.1	20.6
LM393DRG3	SOIC	D	8	2500	364.0	364.0	27.0
LM393DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393DRG4	SOIC	D	8	2500	340.5	338.1	20.6
LM393PSR	so	PS	8	2000	356.0	356.0	35.0
LM393PWR	TSSOP	PW	8	2000	356.0	356.0	35.0
LM393PWRG3	TSSOP	PW	8	2000	364.0	364.0	27.0
LM393PWRG4	TSSOP	PW	8	2000	356.0	356.0	35.0

INSTRUMENTS

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM2903P	Р	PDIP	8	50	506	13.97	11230	4.32
LM2903P	Р	PDIP	8	50	506	13.97	11230	4.32
LM2903QD	D	SOIC	8	75	505.46	6.76	3810	4
LM293P	Р	PDIP	8	50	506	13.97	11230	4.32
LM293P	Р	PDIP	8	50	506.1	9	600	5.4
LM393AP	Р	PDIP	8	50	506.1	9	600	5.4
LM393AP	Р	PDIP	8	50	506	13.97	11230	4.32
LM393P	Р	PDIP	8	50	506	13.97	11230	4.32
LM393P	Р	PDIP	8	50	506.1	9	600	5.4
LM393P	Р	PDIP	8	50	506	13.97	11230	4.32
LM393PE3	Р	PDIP	8	50	506.1	9	600	5.4
LM393PE4	Р	PDIP	8	50	506	13.97	11230	4.32
LM393PS	PS	SOP	8	80	530	10.5	4000	4.1



SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-187.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
- 8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
- 9. Size of metal pad may vary due to creepage requirement.





- 11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 12. Board assembly site may have different recommendations for stencil design.





PLASTIC SMALL OUTLINE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.



PLASTIC SMALL OUTLINE



- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



PLASTIC SMALL OUTLINE



- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 7. Board assembly site may have different recommendations for stencil design.





SMALL OUTLINE INTEGRATED CIRCUIT



- 1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- 4. This dimension does not include interlead flash.
- 5. Reference JEDEC registration MS-012, variation AA.



SMALL OUTLINE INTEGRATED CIRCUIT



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE INTEGRATED CIRCUIT



- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.





NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-001 variation BA.



2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.





PLASTIC SMALL OUTLINE - NO LEAD



- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



PLASTIC SMALL OUTLINE - NO LEAD



- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.







- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-153, variation AA.





NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.





- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



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