Jialin Zheng, Ph.D. Candidate

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Areas of Interest: Real-time simulation, Power electronics modeling, Embedded digital twins, Reinforcement Learning.

Education

Ph.D. in PERET Lab of Prof. Zhengming Zhao, in Electrical Engineering — Aug. 2019 − Jun. 2024 (Expected)
Tsinghua University, Beijing, China
Dissertation: A Comprehensive Study on Real-Time Heterogeneous Hardware-in-the-Loop Simulation Methods for Power Electronic Systems

Bachelor of Engineering, Electrical Engineering — Sept. 2015 − Jun. 2019
Beijing Jiao Tong University, Beijing, China
Overall GPA: 4.42/5.00 Ranking 2/308. Outstanding Graduate

Publications

Published SCI Paper:

[1]. **J. Zheng**, et al., "An Event-Driven Parallel Acceleration Real-Time Simulation for Power Electronic Systems Without Simulation Distortion in Circuit Partitioning," in *IEEE Transactions on Power Electronics*, vol. 37, no. 12, pp. 15626-15640, Dec. 2022.

[2]. **J. Zheng**, et al., "An Event-Driven Real-Time Simulation for Power Electronics Systems Based on Discrete Hybrid Time-Step Algorithm," in *IEEE Transactions on Industrial Electronics*, vol. 70, no. 5, pp. 4809-4819, May 2023.

[3]. **J. Zheng**, et al., "A Semi-implicit Parallel Leapfrog Solver with Half-Step Sampling Technique for FPGA-based Real-time HIL Simulation of Power Converters," in *IEEE Transactions on Industrial Electronics*.

[4]. **J. Zheng**, et al., "An Event Driven Synchronization Framework for Physical Controller Co-Simulation of Megawatt-level Power Electronic Systems," in *IEEE Transactions on Industrial Electronics*.

[5]. **J. Zheng**, et al., "MPSoC-Based Dynamic Adjustable Time-Stepping Scheme with Switch Event Oversampling Technique for Real-time HIL Simulation of Power Converters," in *IEEE Transactions on Transportation Electrification*.

[6]. Y. Zeng, **J. Zheng***, et al., "Real-Time Digital Mapped Method for Sensorless Multi-Timescale Operation Condition Monitoring of Power Electronics Systems," in *IEEE Transactions on Industrial Electronics*.

[7]. Y. Zeng, **J. Zheng***, et al., "Event-Synchronous Time-Asynchronous Method for Controller HIL Simulation of 10 kVA Modular Multilevel Converters," in *IEEE Transactions on Power Electronics*, vol. 38, no. 8, pp. 9351-9357, Aug. 2023.

[8]. Y. Zeng, Z. Zhao, **J. Zheng***, et al., "Extended Discrete-State Event-Driven Hardware-in-the-Loop Simulation for Power Electronic Systems Based on Virtual-Time-Ratio Regulation," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 11, no. 3, pp. 2428-2440, June 2023.

[9]. Y. Zeng, Z. Zhao, **J. Zheng***, et al., "A Self-Restoring Fault-Tolerant Method for Controller Cooperation Simulation of Power Electronics Systems," in *IEEE Transactions on Industrial Electronics*, vol. 71, no. 1, pp. 572-582, Jan. 2024.

[10]. H. Xu, **J. Zheng***, et al., "Topology-Aware Matrix Partitioning Method for FPGA Real-Time Simulation of Power Electronics Systems," in *IEEE Transactions on Industrial Electronics*.

[11]. H. Wang, J. Shi, L. Yuan, Y. Zeng, **J. Zheng**, et al., "Universal Phase-Shift Modulation Scheme and Efficiency Optimization for Modular Multi Active Bridge Converter, " in *IEEE Transactions on Industrial Electronics*. Accept.

[12]. D. Mou, L. Yuan, Q. Luo, Y. Li, C. Liu, **J. Zheng**, et al., "Overview of Multi-Degree-of-Freedom Modulation Techniques for Dual Active Bridge Converter," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*.

Submitted SCI Paper:

[1]. **J. Zheng**, et al., " FPGA-based Real-Time X-in-the-loop Simulation Testbench for Dynamic Power Electronics System with Stochastic and Nonlinear Behaviors," in *IEEE Transactions on Industrial Electronics*. Under Review.

[2]. **J. Zheng**, et al., " Embedded Real-time Digital Twins for Power Converters Enhancement through Model-based Edge Computing," in *IEEE Transactions on Industrial Informatics*. Under Review.

[3]. **J. Zheng**, et al., "HILGym: A HIL-Driven Controller Training Scheme for Hybrid Microgrid Clusters Decentralized Power Regulation via Multi-Agent Reinforcement Learning," in *IEEE Transactions on Smart Grid*. Under Review.

[4]. H. Xu, Y. Zeng, **J. Zheng**, et al., "FPGA-Based Implicit-Explicit Real-time Simulation Solver for Railway Wireless Power Transfer with Nonlinear Magnetic Coupling Components," in *IEEE TTE,* Under Review.

[5]. H. Xu, B. Shi, Z. Yu, **J. Zheng**, et al., "Numerical Derivative-based Flexible Integration Algorithm for Power Electronic Systems Simulation Considering Nonlinear Components, " in *IEEE TIE* Under Review.

[6]. W. Liu, Z. Zhao, Y. Zeng, **J. Zheng,** et al., "Key-Frame Prediction Algorithm based Adaptive Synchronization Mechanism for Power Electronics System Co-Simulation" in *IEEE TIE*. Under Review.

[7]. H. Wang, S. Ji, Y, Zhang, **J. Zheng**, et al., "High-Frequency-Link-based Reactive-Power Optimal Control for Modular Multi Active Bridge Converter" in *IEEE JESTIE*. Under Review.

Research Experiences

Project 1: *RL-based Optimization for Microgrid Real Controllers in RT-HIL Environment* Apr. 2023 - Present

- Integrated a GPU with CUDA capabilities into our real-time simulator through PCIe, subsequently deploying a multi-agent reinforcement learning algorithm on it.
- Established a learning loop and a hardware loop. The hardware loop was employed to assess the impact of control strategies implemented by the controllers. Simultaneously, the hardware loop also functioned as the environment for the learning loop, facilitating the training of multiple agents.
- Targeted training objectives such as overall microgrid stability and load flow optimization.

Project 3: *MPSoC-based Oversampling technique for Ultra High Frequency Applications* Aug. 2022 - Feb. 2023

- Proposed a dynamic adjust time-step simulation scheme for applications involving ultra-high switching frequencies, sampling was executed at the FPGA's maximum capacity and transformed into switch event information. The CPU utilized this switch data to flexibly arrange the step size, while the FPGA conducted matrix computation in a highly parallel fashion according to the arranged step size.
- Given adequate computational capabilities, a fixed iteration process was also incorporated to confront the natural commutation issue of diodes.

Project 5: *FPGA-based Semi-step Leapfrog Parallel Solver for Multi-timescale Monitoring* Apr. 2022 - Jun. 2022

- Proposed a pioneering open-tube bridge arm model, specifically optimized for FPGA's hardware computational characteristics. This model ensures the system matrix remains unaltered, eliminating the necessity for matrix updates.
- Introduced a semi-implicit leapfrog parallel solver. This solver partitions the system into two variable groups and conducts computations in a leapfrog fashion, thus alleviating the computational load. Each variable group achieves the stability of semi-implicit computations with the computational quantity of explicit computations, facilitating parallel processing on FPGA.

Project 6: *Multi-CPUs Parallel Acceleration of Event-driven Real-time (RT) simulator* Sep. 2021 - Apr. 2022

- Put forward a circuit partitioning method that prevents distortion by heightening the numerical order of decoupled variables, breaking down large-scale circuits into more manageable ones.
- Constructed a synchronization framework for multiple simulation cores, scheduling simulation processes to enable multi-core parallel computation.
- By engaging eight CPUs for parallel computation, a simulation scale thrice as large as the most sophisticated commercial real-time simulator available presently can be attained at 1/16th of the hardware cost.

Project 8: *Power electronic simulation software (DSIM) development* Sep. 2019 - Mar. 2021

- Served as a key developer for the 2019b, 2020a, and 2020b updates of DSIM, a software product of our laboratory aimed at expedited power electronic system simulation.
- Tasked with the creation of transient models for SiC MOSFERT, and their integration into the overall simulation.
- Authored over 1500 lines of C++ code to implement the developed functions.

Honors and Awards

Siyuan Electric Scholarship, Tsinghua University (Top 10%) 2022
Outstanding Graduate, Beijing Municipal Education Commission (Top 5%) 2019
Outstanding Graduate, Beijing Jiaotong University (Top 5%) 2019
National Scholarship, Ministry of Education of the People's Republic of China (Top 1%) 2017, 2018
First-Class Academic Scholarship, Beijing Jiaotong University (Top 5%) 2016, 2017, 2018

Skills & Languages

- **Programming:** Python, C/C++, m, and Verilog HDL
- **Proficient Software:** MATLAB, Anaconda, Plecs, LTSpice, Xilinx Vivado, PyCharm, Clion, Xilinx Vitis
- **Language:** Mandarin / English