IEEE802.11b/g

- IEEE802.11b
- IEEE802.11g

Review

- **OFDM**
  - **Orthogonal carriers**
  - **IFFT/FFT**
- **IEEE 802.11a**
  - **Variable data rates**

PLCP Frame Formats in IEEE 802.11b

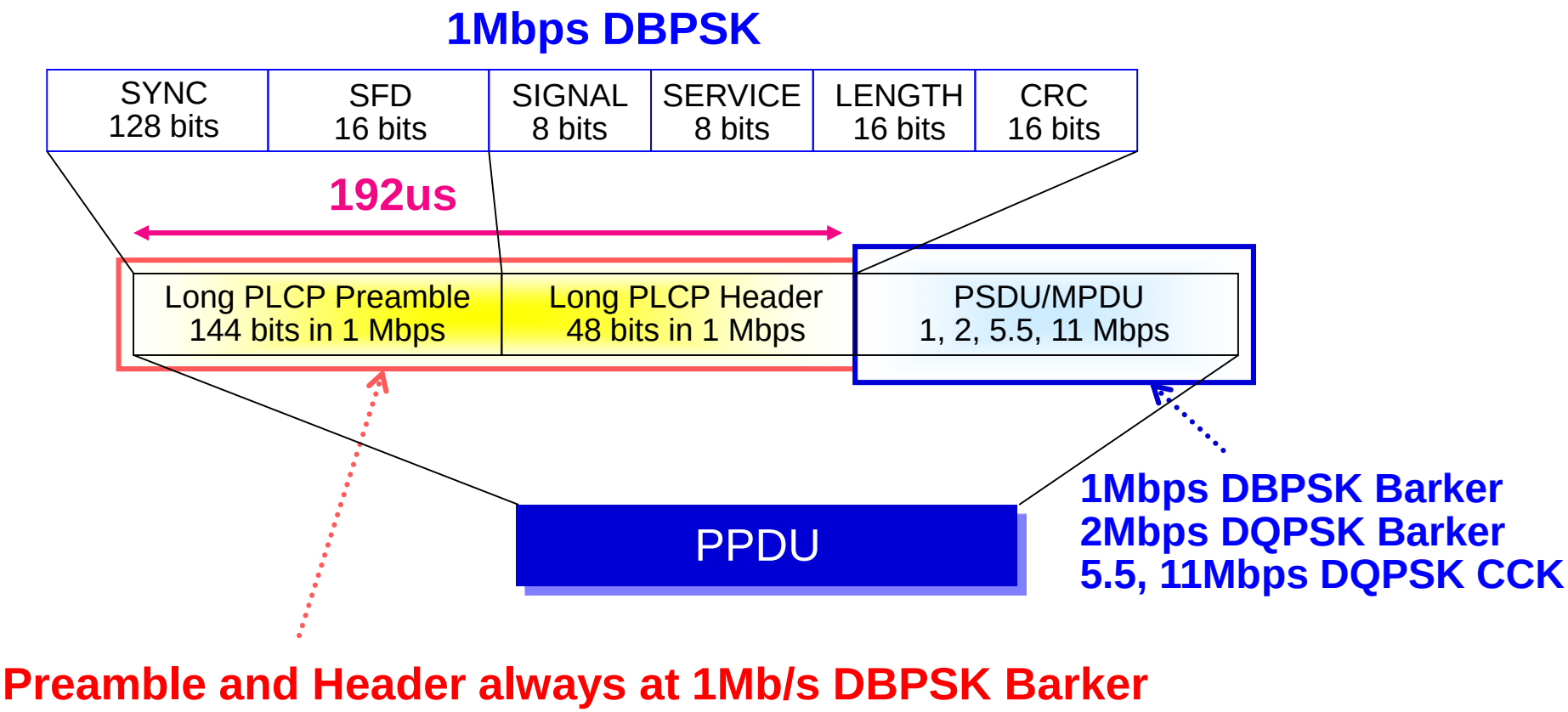
- **Two different preamble and header formats**

  - **Long PLCP PPDU format (Mandatory in 802.11b)**
    - » **144-bit preamble : 1Mbps DBPSK**
    - » **48-bit header : 1Mbps DBPSK**
    - » **Spend 192us**
    - » **PSDU : 1, 2, 5.5, 11Mbps**
    - » **Compatible with 1 and 2 Mbps**

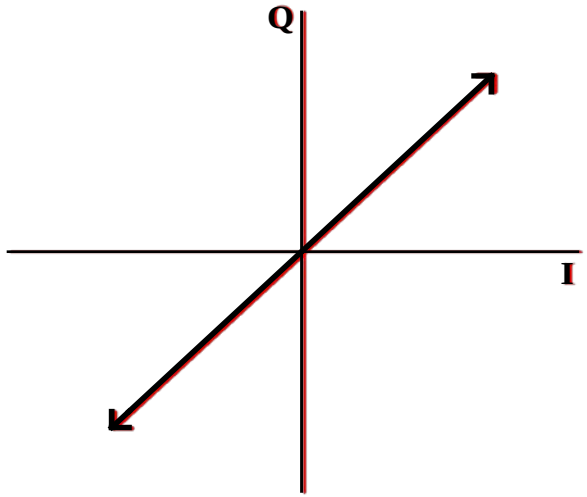
  - **Short PLCP PPDU format (Optional in 802.11b)**
    - » **Minimize overhead, maximize data throughput**
    - » **72-bit preamble : 1Mbps DBPSK**
    - » **48-bit header : 2Mbps DQPSK**
    - » **Spend 96us**
    - » **PSDU : 2, 5.5, 11 Mbps**

Long PLCP Frame Format

- **Mandatory in 802.11b**



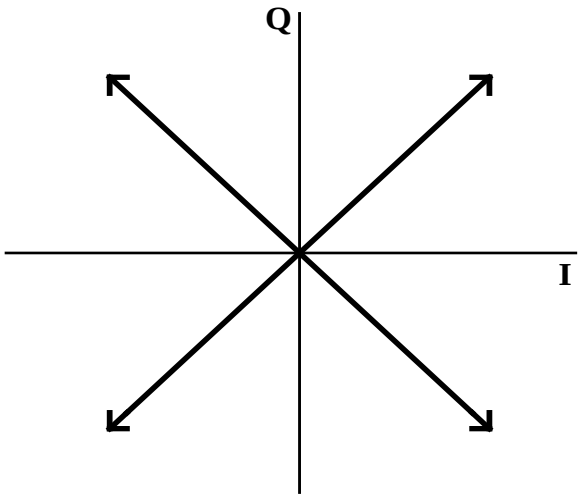
DBPSK Modulation



Bit Input	Phase Change (+jω)
0	0
1	π

Table 1, 1 Mb/s DBPSK Encoding Table.

DQPSK Modulation

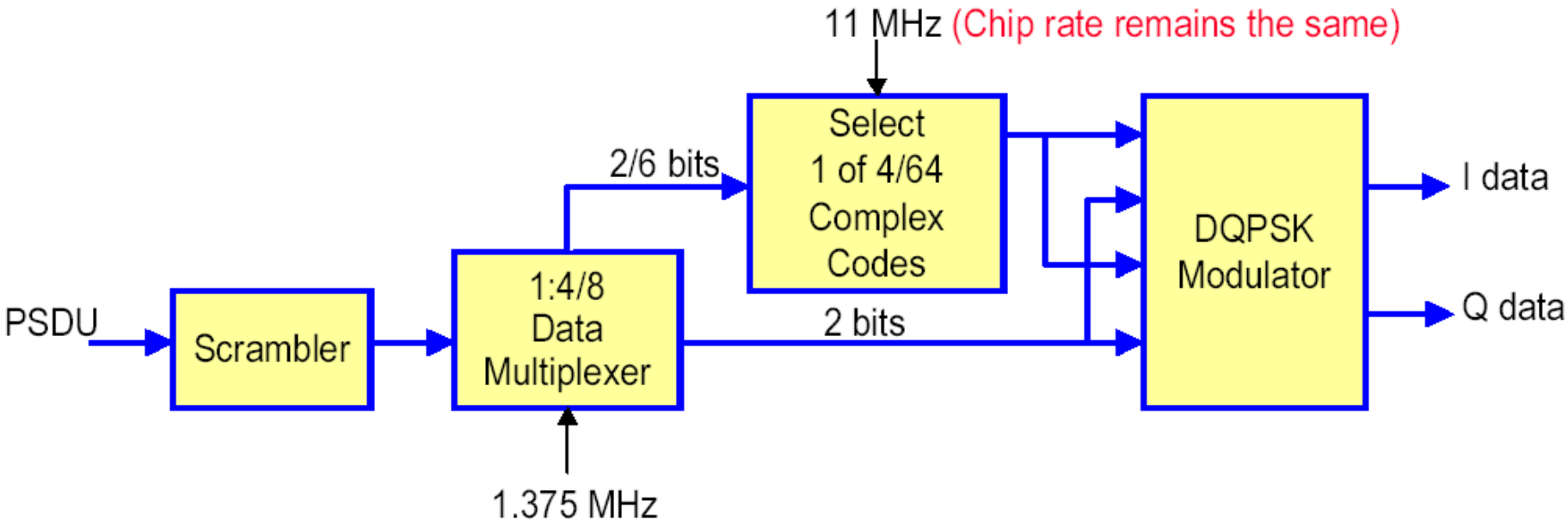


Dibit pattern (d0,d1) d0 is first in time	Phase Change (+jω)
00	0
01	π/2
11	π
10	3π/2 (-π/2)

Table 1, 2 Mb/s DQPSK Encoding Table

Complementary Code Keying (CCK)

- **HR/DSSS adopts 8-chip CCK as the modulation scheme with 11MHz chipping rate**
- **It provides a path for interoperability with existing 1,2 Mbps Spec.**



8-chip*1.375MHz = 11MHz chipping rate

Complementary Code Keying (CCK)

- **Spreading code length = 8, c={c0-c7} and**

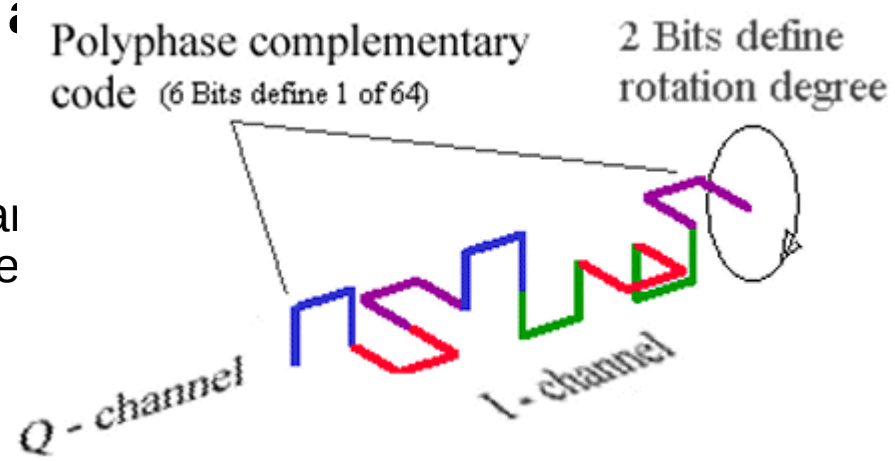
$$c = \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)},$$
$$-e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1}\}$$

where φ_1 is added to all code chips,

φ_2 is added to all odd code chips,

φ_3 is added to all odd pairs of code chips, and

φ_4 is a[illegible] chips.



Cover code : c4 a[illegible] over sequence to optimize the seque[illegible] offsets in the codes.

Complementary Code Keying (CCK) 5.5Mbps

- **At 5.5Mbps CCK, 4 data bits (d0,d1,d2,d3) are transmitted per symbol**
  - **Chip Rate: 11 Mcps, with CCK, 8 chips form a CCK symbol. Therefore, symbol rate is:**

    11 Mcps / 8 chips/symbol = 1.375 Msps

    which leads to the data rate in this case:

    1.375 Msps * 4 bits/sym = 5.5 Mbps
- **(d0,d1) is DQPSK modulated to yield φ_1, (d2,d3) encodes the basic symbol, where**

$$\begin{cases} \varphi_2 = d_2 \times \pi + \pi/2; \\ \phi_3 = 0; \\ \phi_4 = d_3 \times \pi; \end{cases}$$

Table 108—DQPSK encoding table

Dibit pattern (d0, d1) (d0 is first in time)	Even symbols phase change (+jω)	Odd symbols phase change (+jω)
00	0	π
01	π/2	3π/2 (–π/2)
11	π	0
10	3π/2 (–π/2)	π/2

Complementary Code Keying (CCK) 5.5Mbps

- Take (d0, d1, d2, d3) = (0010) and even symbol for example
  - $\varphi_1 = 0$. $\varphi_2 = 1*\pi + \pi/2 = 3\pi/2$, $\varphi_3 = 0$, $\varphi_4 = 0*\pi = 0$

c =

$$\{e^{j(0+\frac{3\pi}{2}+0+0)}, e^{j(0+0+0)}, e^{j(0+\frac{3\pi}{2}+0)}, -e^{j(0+0)}, e^{j(0+\frac{3\pi}{2}+0)}, e^{j(0+0)}, -e^{j(0+\frac{3\pi}{2})}, e^{j(}$$

By Euler's formula we have:

$$e^{j(\theta)} = cos\theta + jsin\theta$$

$$c = \{e^{j(\frac{3\pi}{2})}, e^{j(0)}, e^{j(\frac{3\pi}{2})}, -e^{j(0)}, e^{j(\frac{3\pi}{2})}, e^{j(0)}, -e^{j(\frac{3\pi}{2})}, e^{j(0)}\}$$

$$= \{-j, 1, -j, -1, -j, 1, j, 1\}$$

Table 109—5.5 Mbit/s CCK encoding table

d2, d3	c1	c2	c3	c4	c5	c6	c7	c8
00	1j	1	1j	−1	1j	1	−1j	1
01	−1j	−1	−1j	1	1j	1	−1j	1
10	−1j	1	−1j	−1	−1j	1	1j	1
11	1j	−1	1j	1	−1j	1	1j	1

□φ1=0

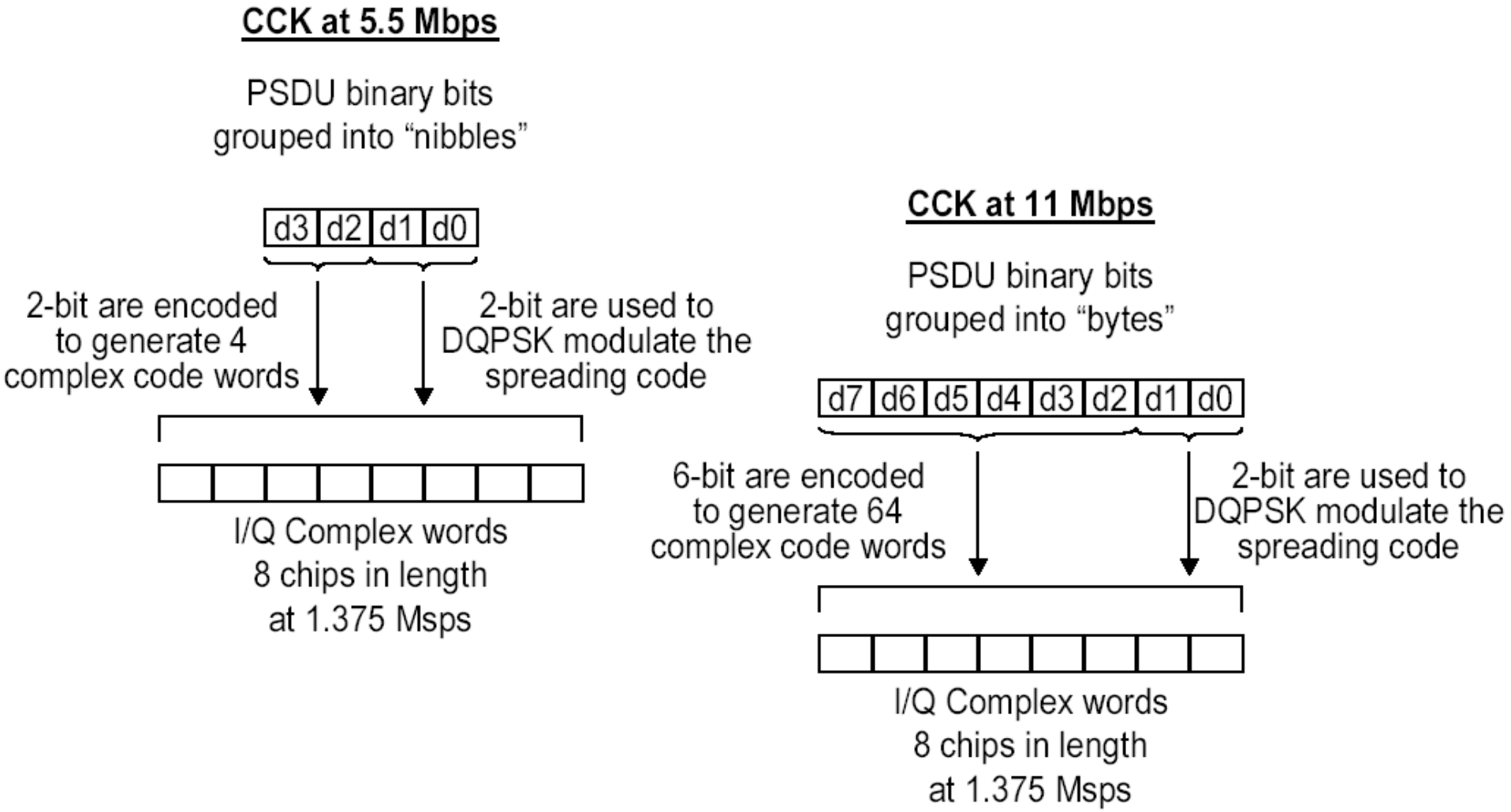
Complementary Code Keying (CCK) 11Mbps

- At 11Mbps CCK, 8 data bits (d0-d7) are transmitted per symbol
  - (d0,d1) is DQPSK modulated to yield φ1, which the information is bear on the "phase change" between two adjacent symbols
  - (d2,d3),(d4,d5),(d6,d7) encode φ2, φ3, φ4, respectively, based on QPSK
  - (11/8)*(8 data bits per symbol)*1Mbps = 11Mbps

Table 110—QPSK encoding table

Dibit pattern [di, d(i+1)] (di is first in time)	Phase
00	0
01	π/2
10	π
11	3π/2 (–π/2)

Complementary Code Keying (CCK)



DSSS Specification Summary

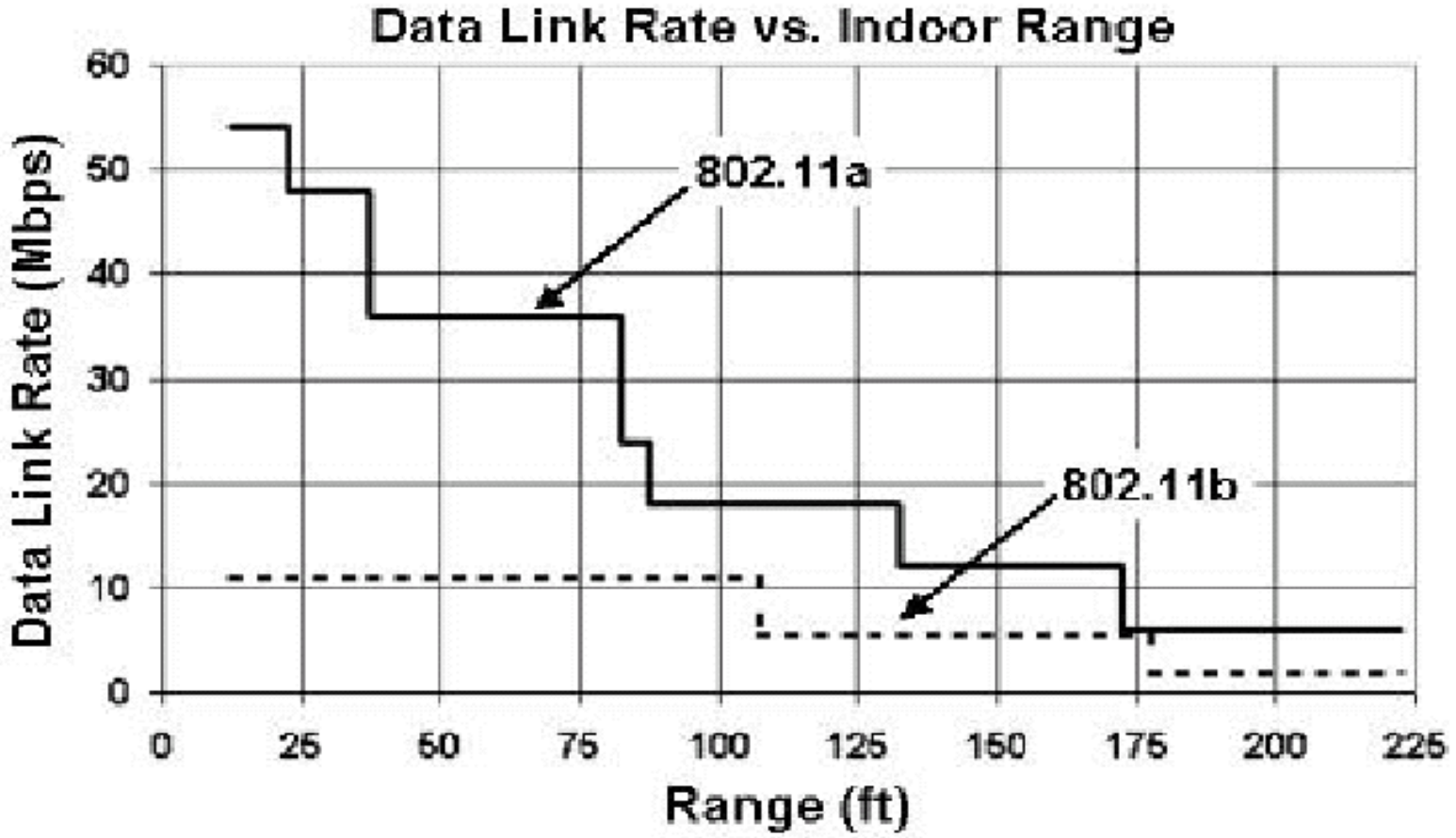
- **Slottime** **20 us**
- **TX to Rx turnaround time** **10** us
- **Rx to Tx turnaround time** **5** us
- **Operating temperature range**
  - » **type 1: 0 - 40 °C**
  - » **type 2: -30 - 70 °C**
- **Tx Power Levels**
  - » **1000 mW** **USA (FCC 15.274)**
  - » **100 mW** **Europe (ETS 300-328) (=20dbm)**
  - » **10 mW/MHz** **Japan (MPT ordinance 49-20)**
- **Minimum Transmitted Power 1 mW**
- **Tx power level control required above 100 mW**
  - – **four power levels**

DSSS Specification Summary (cont)

• Tx Center Frequency Tolerance	+/- 25 ppm
• Chip Clock Frequency Tolerance	+/- 25 ppm
• Tx Power On Ramp	2 μs
• Tx Power Down Ramp	2 μs
• RF Carrier suppression	15 dB
• Transmit modulation accuracy	test procedure
• Rx sensitivity	-80 dB @ 0.08FER (1024 Bytes)
• Rx max input level	-4 dB
• Rx adjacent channel rejection	>35 dB @ > 30(25) MHz separation between channels

IEEE 802.11a vs IEEE 802.11b (max.)

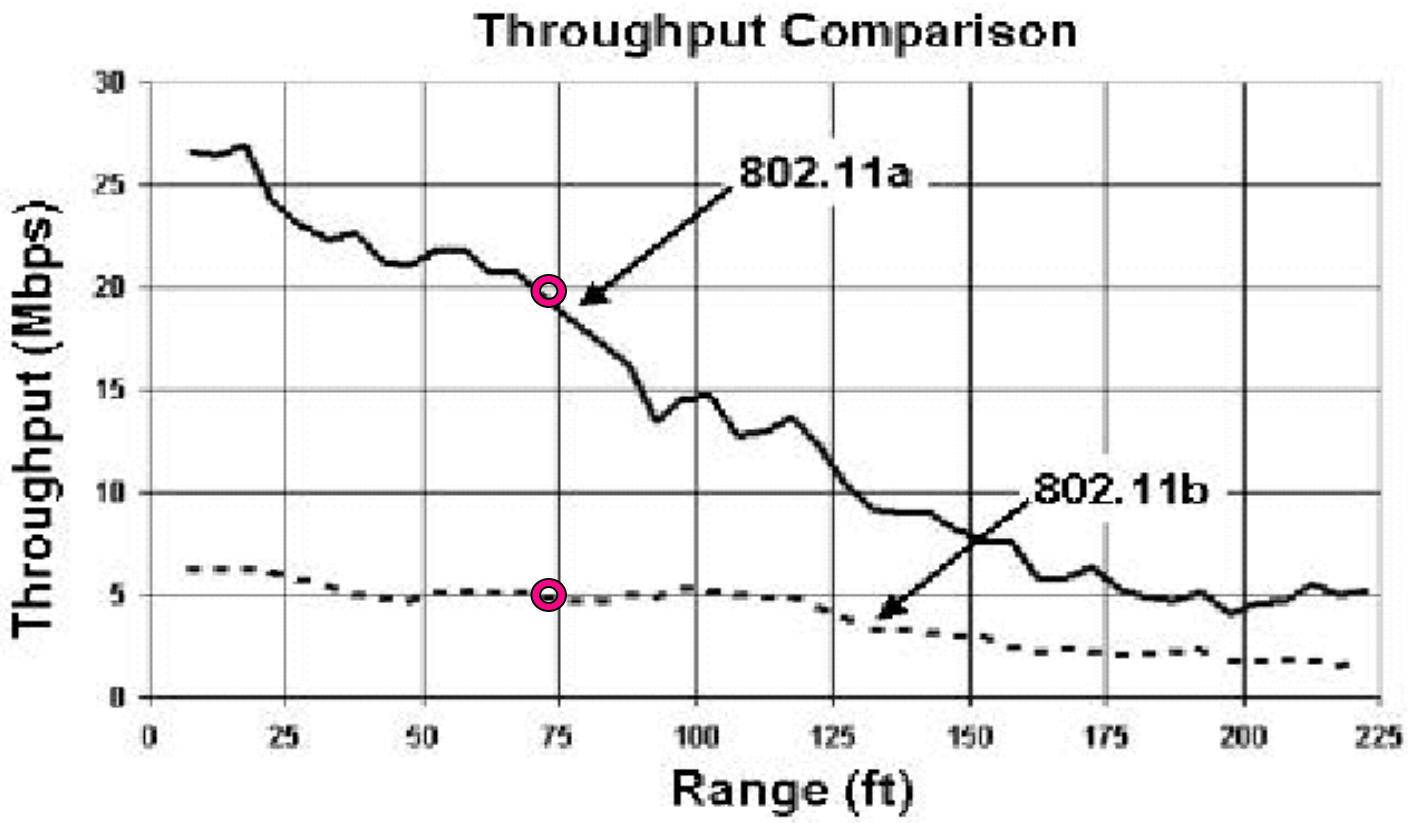
1500 bytes per frame



Refer from "AtherosRangeCapacityPaper.pdf"

IEEE 802.11a vs IEEE 802.11b (average)

1500 bytes per frame



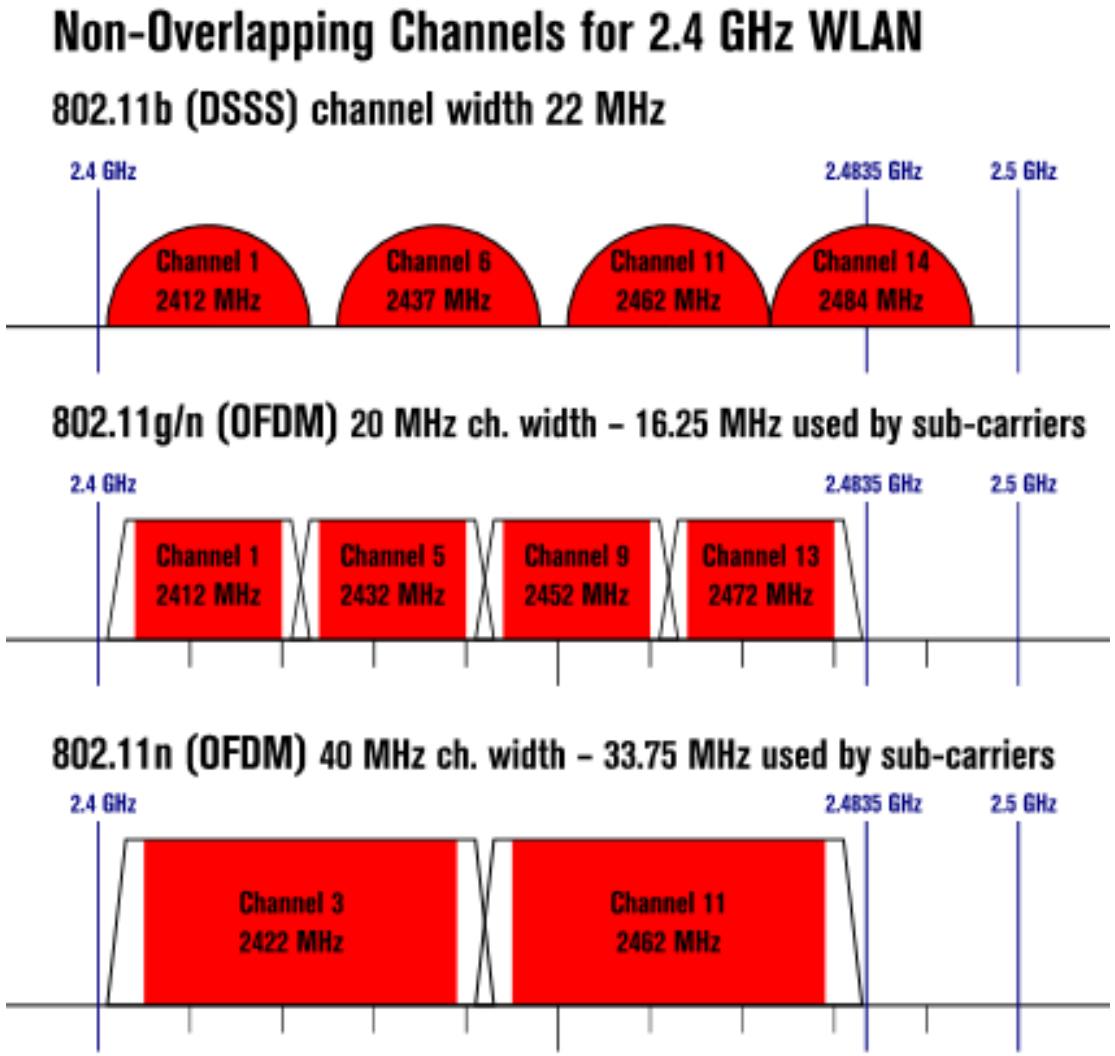
Refer from "AtherosRangeCapacityPaper.pdf"

IEEE 802.11g Extended Rate PHY (ERP) Specification

Wireless Physical Layer

- **802.11g *OFDM(Orthogonal Frequency Division Multiplexing*)**
  - **An attempt to combine the best of both 802.11a and 802.11b.**
  - **Supports bandwidths up to 54 Mbps.**
  - **Uses 2.4 GHz frequency for greater range.**
  - **Is backward compatible with 802.11b.**
  - **Rectified in June, 2003.**

Overview of IEEE802.11 Channels



IEEE 802.11g

- **Extended Rate PHY (ERP) Goal :**
  - **coexists with 802.11b**
  - **enhances the ability of interference protection**
- **ERP-DSSS/CCK (Mandatory) (1,2,5.5,11 Mbps)**
  - **short PLCP PPDU is mandatory**
  - **transmit center frequency and symbol clock frequency shall refer the same oscillator (locked oscillator, mandatory)**
- **ERP-OFDM (Mandatory) (6,9,12,18,24,36,48,54 Mbps)**
  - **Optional 9 us slot time when the BSS consists of only ERP devices**
- **ERP-PBCC (Optional) (5.5,11,22,33 Mbps)**
  - **256-state binary convolutional code**
- **DSSS-OFDM (Optional) (6,9,12,18,24,36,48,54 Mbps)**
  - **Hybrid modulation**
  - **DSSS : for preamble and header**
  - **OFDM : for data payload**

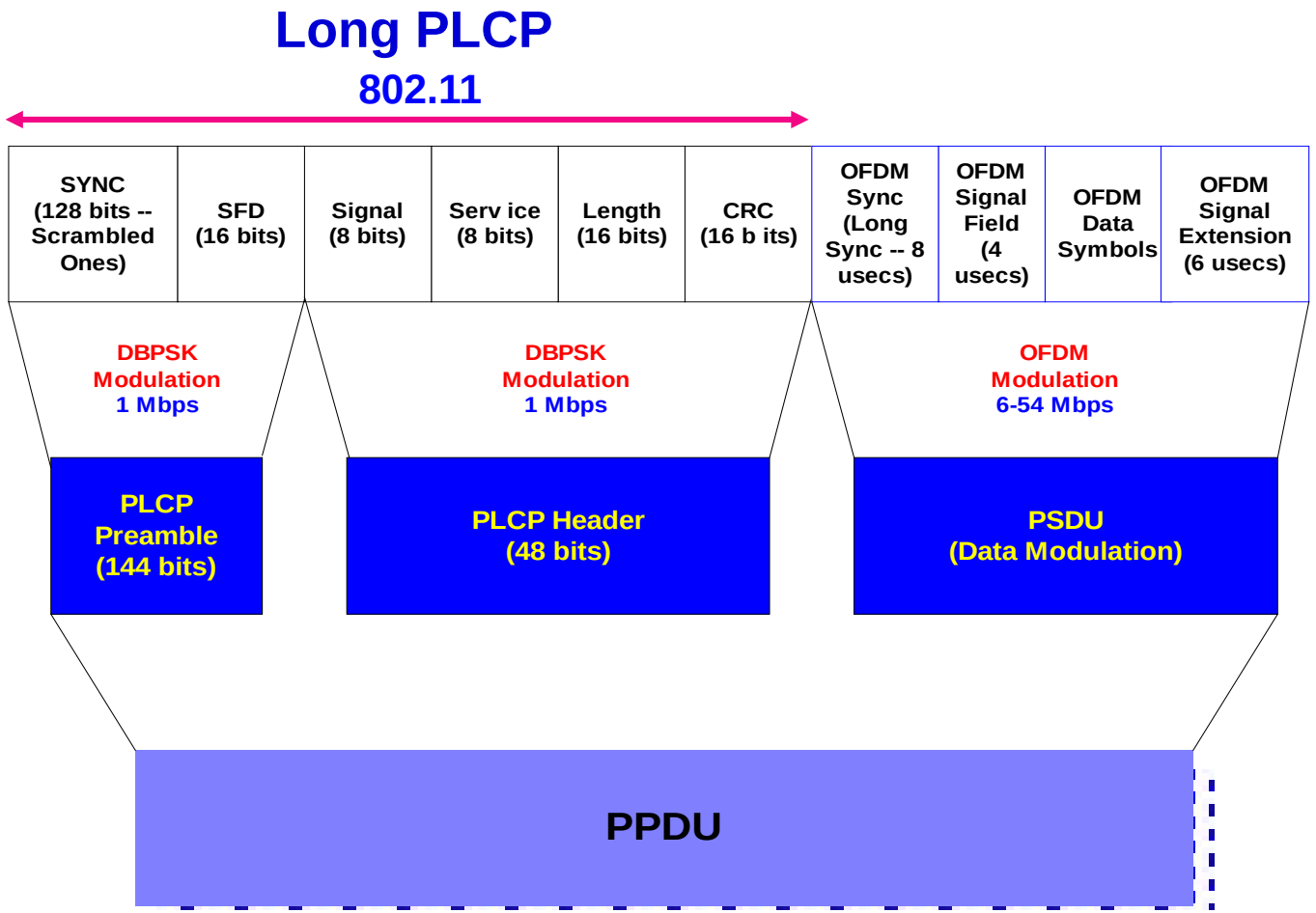
IEEE 802.11g PCLP

- **Three different mandatory PLCP PPDU format**
  - **Long Preamble and header (same as 11b) (for DSSS-OFDM)**
  - **Short Preamble and header (same as 11b) (for DSSS-CCK)**
    - » **Differences in SERVICE field**
      - **Diff 1 : a bit in SERVICE field is used to indicate DSSS-OFDM**
      - **Diff 2 : two bits in SERVICE field are used to resolve the length ambiguity for PBCC-22 and PBCC-33**

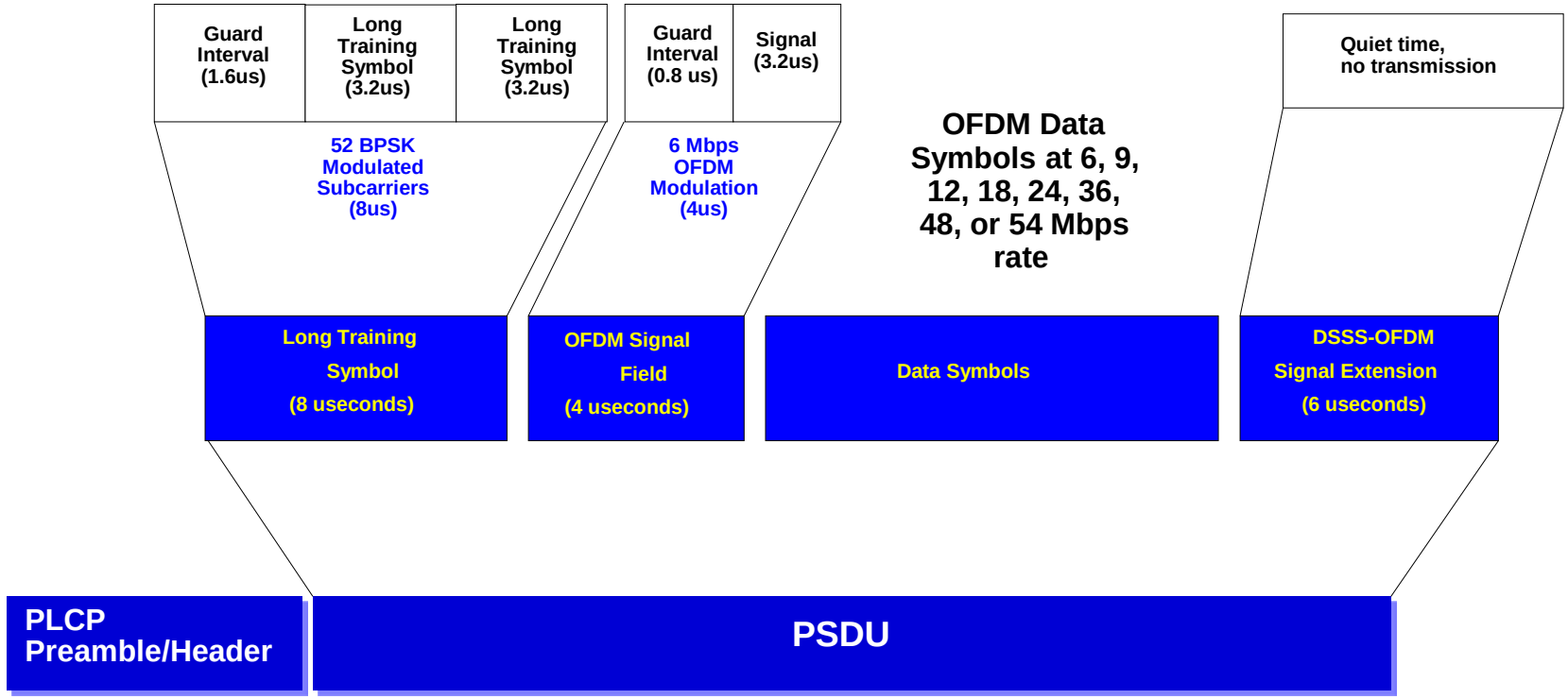
b0	B1	b2	b3	b4	b5	b6	b7
Modulation selection 0 = Not DSSS-OFDM 1 = DSSS-OFDM	Reserved	Locked Clock Bit 0 = not locked 1 = locked	Modulation Selection 0 = CCK 1 = PBCC	Reserved	Length Extension Bit (PBCC)	Length Extension Bit (PBCC)	Length Extension Bit

  - **OFDM preamble and header (similar as 11a) (for ERP-OFDM)**

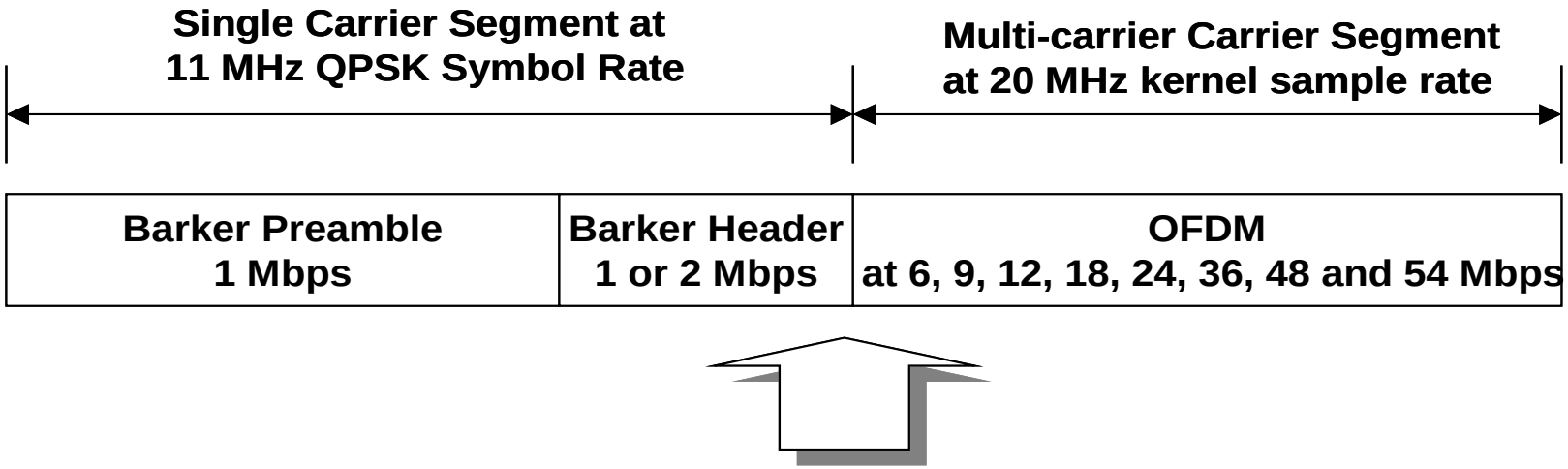
Long PLCP for 802.11g DSSS-OFDM



DSSS-OFDM PLCP PSDU Encoding



Single-Carrier to Multi-carrier transition

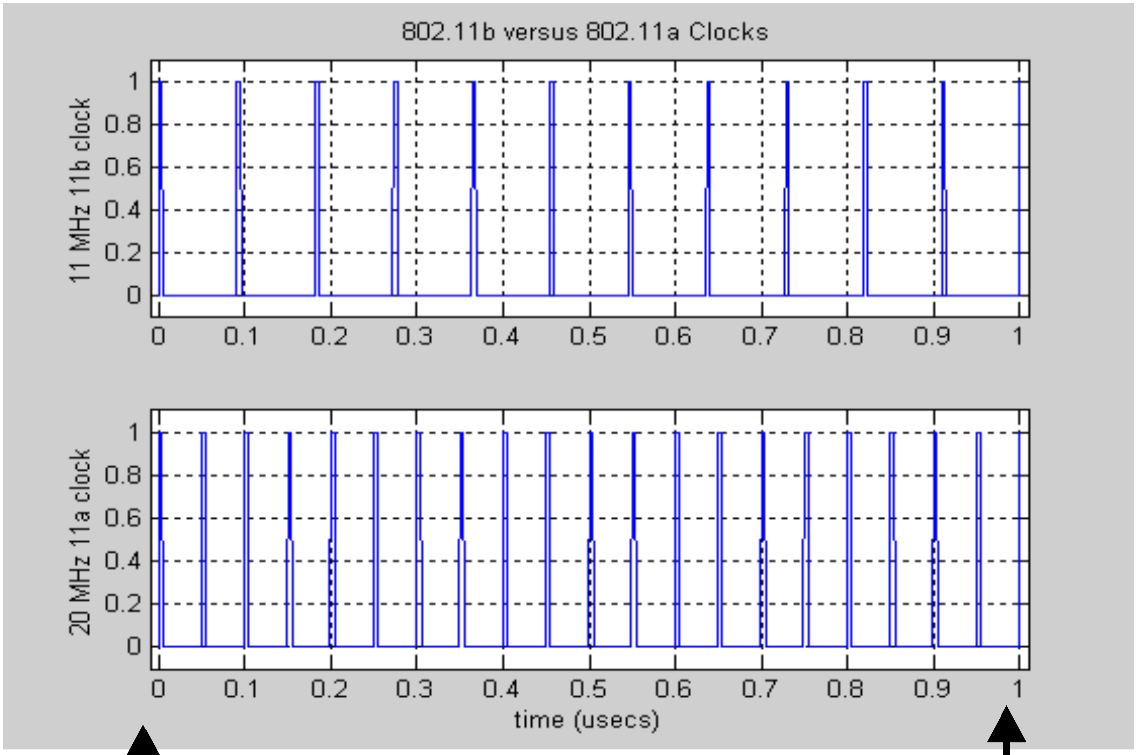


Ideal Transition Specification

- **Constant Power**
- **Constant Spectrum**
- **Constant Frequency and Phase**
- **Constant Timing**

Single-Carrier to Multi-carrier transition

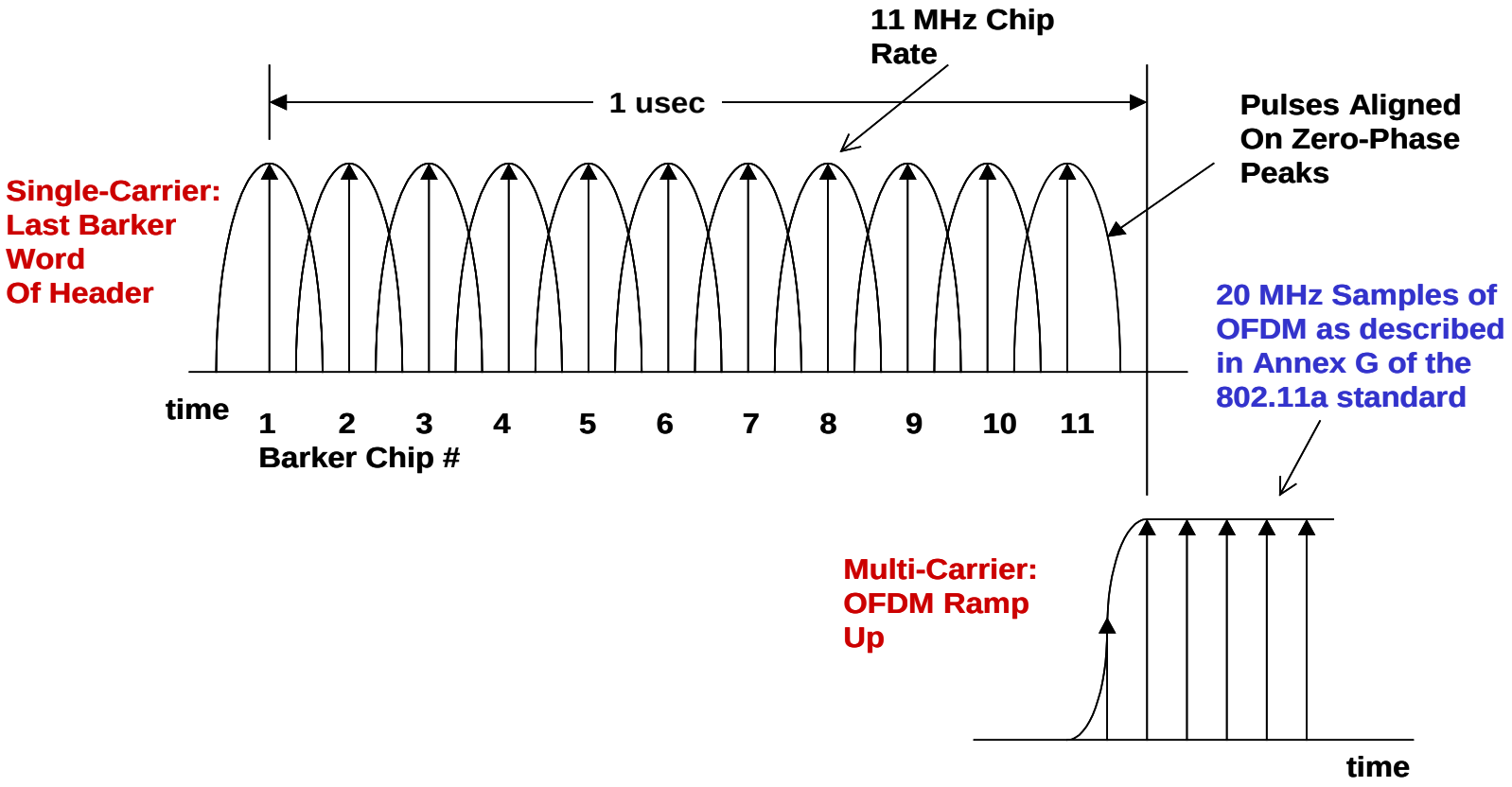
- The signals are easily aligned by first aligning the 11 MHz clock and the 20 MHz clock on 1 us boundaries



1/11 vs. 1/20

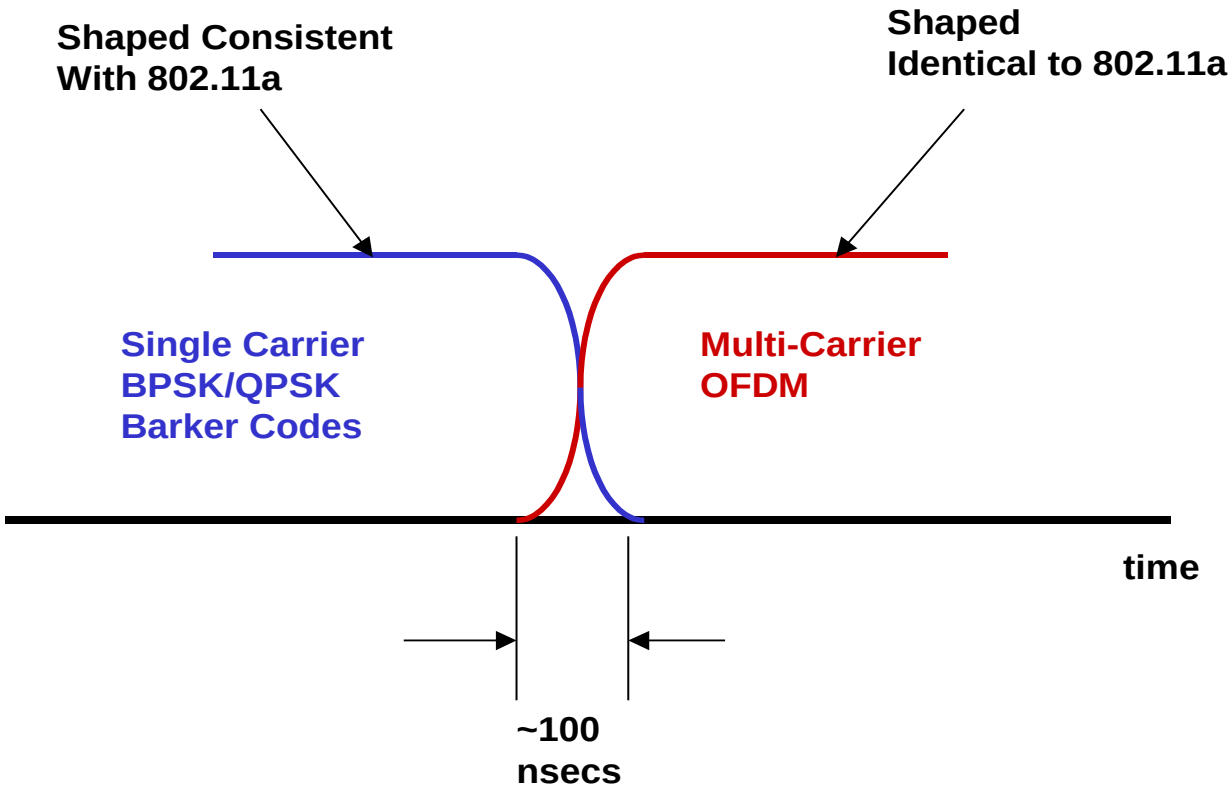
Single-Carrier to Multi-carrier transition

- The signals are easily aligned by first aligning the 11 MHz clock and the 20 MHz clock on 1 us boundaries



Single-Carrier to Multi-carrier transition

- The single carrier segment of a packet should terminate in nominally 0.1 us (100ns)



Class Quiz

- What is CCK coding?
- What are the data rates in IEEE802.11g?
- What is the main feature in PHY in IEEE802.11g?