FULL ADDER(1BIT) DATAFLOW STYLE

```
module full_adder(a,b,cin,sum,cout);
 input a,b,cin;
 output sum,cout;
 wire sum,cout;
 assign sum=a^b^cin;
 assign cout=(a&b)|((a^b)&cin);
endmodule
```

TESTBENCH

```
module full_adder_tb;
 reg a,b,cin;
 wire sum ,cout;
 full_adder DTU (a,b,cin,sum,cout);
 initial
  begin
   $dumpfile("design.vcd");
   $dumpvars;
   $monitor($time,"a=%b , b=%b , cin=%b ,sum=%h,cout=
%b",a,b,cin,sum,cout);
   #5 a=1'b0;b=1'b1;cin=1'b1;
   #5 a=1'b0;b=1'b0;cin=1'b0;
   #5 $finish;
  end
endmodule
```