FULL ADDER(1BIT) STRUCTURAL STYLE

```
module fulladder (a,b,c,sum,cout);
 input a,b,c;
 output sum,cout;
 wire t1,t2,t3;
 xor g1(t1,a,b) , g4(sum,t1,c);
 or g5(cout,t3,t2);
 and g2(t2,a,b), g3(t3,c,t1);
endmodule
```

TESTBENCH

```
module fulladder_tb;
 reg a,b,c;
 wire sum ,cout;
 fulladder DTU (a,b,c,sum,cout);
 initial
  begin
   $dumpfile("design.vcd");
   $dumpvars;
   $monitor($time,"a=%b , b=%b , c=%b ,sum=%h ,cout=%b",a,b,c,sum,cout);
   #5 a=1'b0;b=1'b1;c=1'b1;
   #5 a=1'b0;b=1'b0;c=1'b0;
   #5 $finish;
  end
endmodule
```