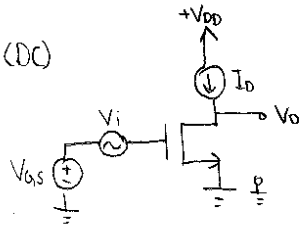
Wordy Notes (ECE 242)

Transistor's Intrinsic Gain (MOSFETs)

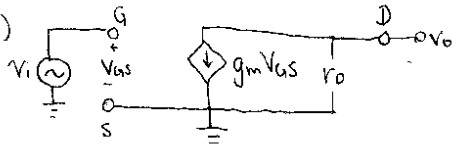
Given some MOSFET circuit

(DC)



and assuming it's in saturation, we can draw its small signal model as such:

(SS)



Note how all voltage sources are grounded and current sources are open

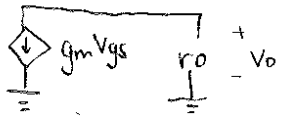
Both NMOS and PMOS small signal models are of this form. It is simply a matter of connecting external components to the gate/source/drain as required.

Now, how do we find the gain $A = v_o/v_i$ from this model?

The first thing to realize is that v_i is attached in parallel to the Gate-Source junction, meaning v_{gs} is the same voltage as v_i

This, in turn, means our dependent current source's current can be expressed as $g_m v_i$ instead

Since the drain is an open circuit, the resulting current can only flow through the source-resistance loop:



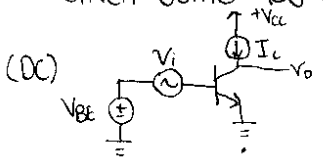
and the resulting voltage generated across r_o is the output voltage itself.

Through Ohm's Law, the voltage across r_o is $v_o = (-g_m v_i) r_o$, which can be rearranged to yield our gain:

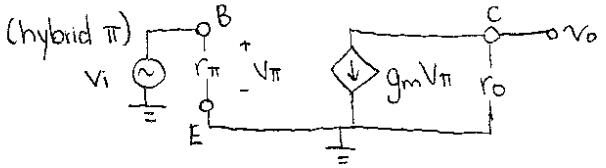
$$A = \frac{v_o}{v_i} = -g_m r_o$$

Transistor's Intrinsic Gain (BJT)

Given some BJT Circuit:



and assuming it's in active, we can draw its small signal model following the same shorting / open rules as before:



Notice that it looks remarkably like the MOSFET's small signal model, with the exception of r_π where the empty v_{GS} node would be. Of course, again this model works for both NPN and PNP BJTs

Again, how do we find the gain $A = v_o/v_i$?

Notice once again v_i is in parallel with r_π, thereby imparting the entirety of its voltage to r_π. As such, $v_\pi = v_i$.

There are a variety of ways that g_m can be calculated

$$g_m = \mu_n C_{ox} (W/L) [V_{as} - V_t]$$
$$= \frac{\partial I_D}{\partial v_{gs}}$$
$$= \frac{\partial I_D}{(V_{as} - V_t)}$$
$$= \frac{2 I_D}{V_{ov}}$$
$$= \sqrt{2 \mu_n C_{ox} (W/L) I_D}$$

However, μ_n, C_{ox}, width of the chips, and threshold voltage are all fairly stagnant values, and are rather difficult to manipulate transistor - by - transistor. Let's look at r_o.

$$r_o = \frac{1}{\lambda I_{DS}}$$
$$= \frac{V_{A\,mos}}{I_D}$$
$$= \frac{V_A' L}{I_D}$$

We can then combine the two as such:

$$A = \frac{2 I_D}{(V_{as} - V_t)} \quad \frac{V_A' L}{I_D}$$
$$= \frac{2 V_A' L}{(V_{as} - V_t)}$$

Leaving us with essentially the length being the only modifiable variable of the transistor.

Controlling Gain in BJTs

Again, we have the same expression for gain, however the two variables g_m and r_o vary in what they constitute.

$$g_m = \frac{I_c}{V_T} \qquad r_o = \frac{V_A}{I_c}$$

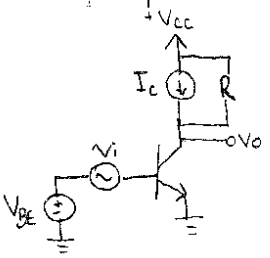
$$\therefore A = g_m r_o = \frac{V_A}{V_T}$$

With V_A being a material property and V_T being a constant 25 mV, we can't actually do much here to change the gain. V_A typically ranges from 5V to 50 V, so realistically the range of the gain is about 200 V/v (46 dB) to 2000 V/v (66 dB).

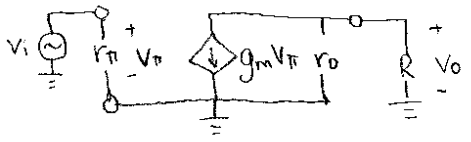
Practical Current Sources and Effects on Gain

Real sources tend to have a source resistance associated with them, and as such our gains may vary dependent on the source resistance's value.

For example:

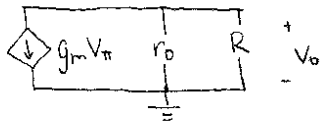


can be drawn in small signal as:



where R is some finite resistance of the source.

Again, assuming our base currents are negligible, we can reduce the circuit to:

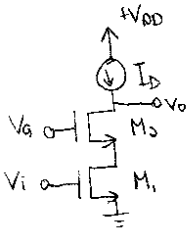


and as such the output voltage is the result of the current going through the parallel equivalent of r_o and R.

$$V_o = (-g_m V_\pi)(r_o // R)$$
$$A = \frac{V_o}{V_i} = -g_m (r_o // R)$$

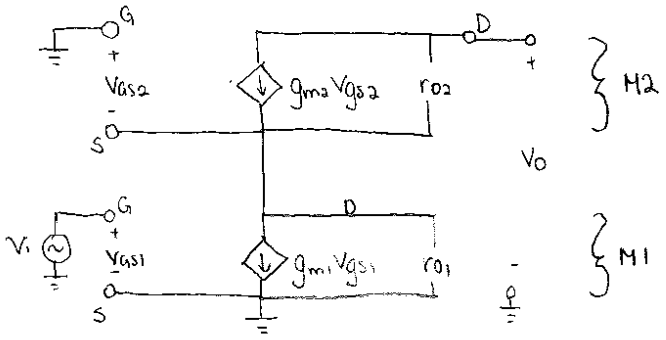
The MOSFET Cascode

So what if we want more gain than can be produced from one transistor? We now introduce the cascode configuration, which has another MOS connected to the first's source.



Just through inspection, it's fairly clear that the bias current I_D flows through both M_1 and M_2.

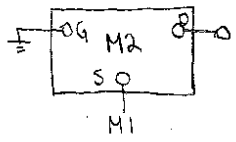
Generally, it's safe to assume each of the transistors have the same parameters, but we'll be deriving relationships generally. Let's draw the small signal model, and calculate our new gain



The first thing to notice is that V_o is measured all the way across r_{o2}, down to r_{o1}, down to ground, so we should be able to find V_o as the sum of voltages across r_{o2} and r_{o1}.

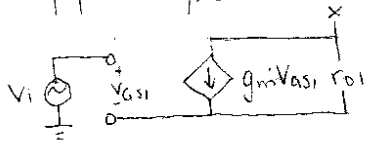
Let's start at M1 and move upwards. V_i is connected in parallel with V_{GS1}, and as such, $V_{GS1} = V_i$, which means the current generated must be $g_{m1}V_i$.

Then, let's take the entire M2 as one black box with three terminals for gate, drain, and source.



The gate, being disconnected from everything else, cannot have any current flowing through it. The drain, being an open circuit, also cannot conceivably have any current through it. By KCL, it follows that the last terminal, the source, must also not have any current, as only then will the net current be zero

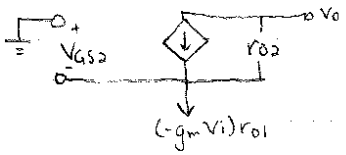
Since no current goes in/out from M1's drain, we can simply analyze M1 on its own.



As such, the voltage across r_{o1} simply evaluates to

$$V_{ro1} = (-g_{m1}V_i)r_{o1}$$

through Ohm's Law. Obviously, this means the voltage RISE across r_{o1} is $(-g_m V_i)\, r_{o1}$, meaning M1's drain / M2's source is at that voltage.



Since $V_{gs2} = V_{g2} - V_{s2}$, we can now provide their values, calculating

$$\begin{aligned} V_{gs2} &= 0 - (-g_m V_i r_{o1}) \\ &= g_m V_i r_{o1} \end{aligned}$$

Since we already know the gain of a MOS transistor is $A = -g_m r_o \rightarrow v_o = -g_m v_{gs} r_o$, we can, with confidence, say that the voltage across r_{o2} is given by that same equation:

$$\begin{aligned} V_{ro2} &= -g_{m2} V_{gs2} r_{o2} \\ &= -g_{m2}(g_{m1} V_i r_{o1}) r_{o2} \end{aligned}$$

Now, since we have both the voltage across r_{o1} and r_{o2}, we can calculate the resulting total r_o.

$$V_o = V_{ro1} + V_{ro2}$$
$$V_o = -g_{m1} v_i r_{o1} - g_{m1} g_{m2} v_i r_{o1} r_{o2}$$
$$V_o = v_i (-g_m r_{o1} - g_{m1} g_{m2} r_{o1} r_{o2})$$
$$A = \frac{V_o}{V_i} = -g_m r_{o1} (1 + g_{m2} r_{o2})$$

Which is neat, but is more interesting if we take the case where both MOSFETs are the same:

If $g_{m1} = g_{m2}$ and $r_{o1} = r_{o2}$:

$$\frac{V_o}{V_i} = -g_m r_o - (g_m r_o)^2$$

And, further, assuming $g_m r_o$ is large enough such that $\frac{g_m r_o}{g_m r_o^2}$ = very small, we can conclude

$$A_{cascode} \approx (A_{one\ mos})^2$$

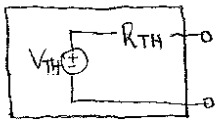
Thevenin Equivalents

Now, let's say we want to draw a thevenin equivalent circuit for our cascode. But what does that mean for a circuit that doesn't provide a constant voltage?

Recall: 

that some linear, two-terminal circuit can be re-drawn as:

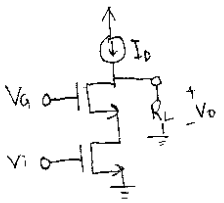
(open circuit)



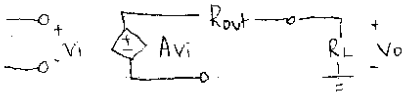
a thevenin voltage in series with a thevenin equivalent resistance looking into those same two terminals,

where R_{TH} simply represents the response to any changes in current

As such, it's not difficult to generalize that a cascode circuit



can be rewritten as a thevenin equivalent circuit that has a DEPENDENT voltage source:



where there is some gain A applied to the input voltage.

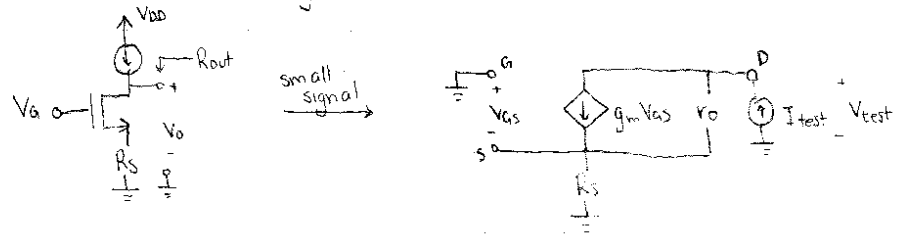
As such, through the voltage divider created by R_{out} and R_L, the resulting output is

$$v_o = Av_i\left(\frac{R_L}{R_{out}+R_L}\right)$$

But now the question is: how do we find the output resistance of the cascode circuit?

R_{out} of a Source-Degenerated MOSFET

To make things simpler, we'll explore the output resistance of a single-MOS circuit first

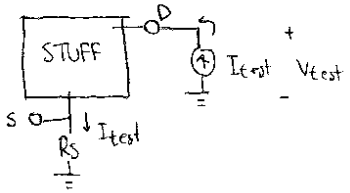


The process to find R_{out} is one that should be familiar from previous years.

① Set all independent sources to zero.
② Apply V_{test} or I_{test} to the terminal we want to find the output resistance of
③ Find open circuit voltage or short-circuit current
④ Calculate $R_{TH} = \frac{V_{test}}{I_{test}}$.

We've already done the first two steps in the small signal model we've already drawn.

Notice how we've attached I_{test} to the drain. Obviously this current can't go up from the source to the gate due to the open circuit, so it must go all down to R_S.



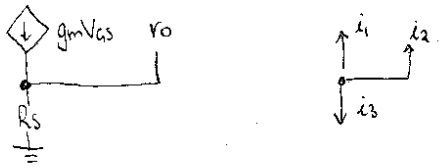
Current in, current out, that's just how life is Now, we can calculate what V_S is:

$$V_S = (I_{test})(R_S)$$

and consequently, $V_{GS} = V_G - V_S$
$= -I_{test} R_S$.

Now that we have V_{GS}, we can re-express the current source's current as $g_m(-I_{test} R_S)$. Remember we're trying to find the resulting test voltage, which is the combined drop across r_o and R_S.

But we don't know exactly how much current flows through r_o, so we can use KCL at the top of R_S to figure that out



Define currents leaving the node as positive.

$$\begin{aligned} 0 &= i_1 + i_2 + i_3 \quad \text{by KCL} \\ &= (-g_m I_{test} R_s) + (-I_{test}) + i_3 \\ i_3 &= g_m I_{test} R_s + I_{test} \end{aligned}$$

and by Ohm's Law it follows that

$$\begin{aligned} V_{r_o} &= i_3 r_o \\ &= g_m I_{test} R_s r_o + I_{test} r_o \end{aligned}$$

and finally, the total voltage drop

$$\begin{aligned} V_o &= V_{R_s} + V_{r_o} \\ &= R_s I_{test} + g_m R_s I_{test} r_o + r_o I_{test} \end{aligned}$$

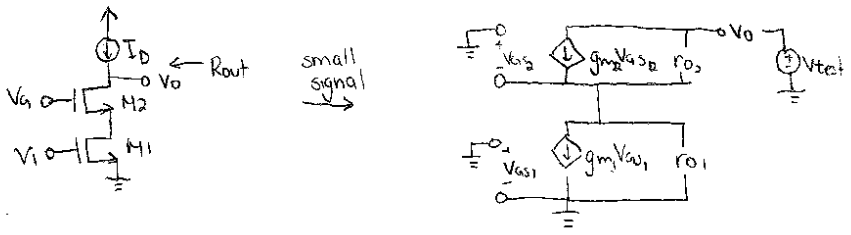
Finally, we can move onto the last step:

$$\begin{aligned} R_{TH} &= \frac{V_o}{I_{test}} \\ &= R_s + g_m R_s r_o + r_o \end{aligned}$$

Which can be approximated to simply $g_m R_s r_o$, given R_s and r_o are large enough values

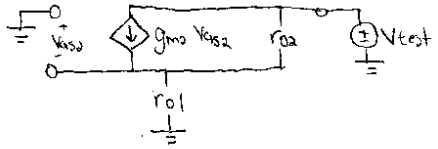
Output Resistance of Cascode Amplifiers

Okay, so now that we've found an approximation for the output resistance of a single MOS, we can take that approximation and use it to calculate the output resistance of multiple.



Again, we've already done the first two steps of solving for R_{TH}. Notice that we've shorted the input signal as well, as it's an independent source

That makes M1's dependent current source zero, and as such, all current provided by M2 must go through r_{o1}, so we could even redraw it as:



Does this look similar? It's because we just solved it - it's the source-degenerated MOSFET circuit, except instead of R_S at the source, it's r_{o1}.

Remember that the Rout came out to:

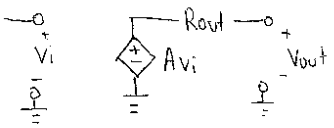
$$R_{out} = R_S + g_m R_S r_o + r_o$$
$$\approx g_m R_S r_o$$

which means the cascode output follows as

$$R_{at} = r_{o1} + g_m r_{o1} r_{o2} + r_{o2}$$
$$\approx g_m r_{o1} r_{o2}$$

Back to the Thevenin / Norton Model

Now, we have all the pieces required to build our equivalent models of cascode amplifiers.



$$A = -g_m r_{o1} [1 + g_{m2} r_{o2}]$$
$$R_{out} = r_{o1} + r_{o2} + g_m r_{o1} r_{o2}$$

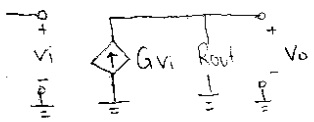
If we want to convert this to the Norton model, all we have to do is calculate G, the transconductance, which is given by A/R_{out}.

$$G = \frac{A}{R_{out}}$$
$$= \frac{-g_m r_{o1} [1 + g_{m2} r_{o2}]}{r_{o1} + r_{o2} + g_m r_{o1} r_{o2}}$$
$$= \frac{-g_m r_{o1} [1 + g_{m2} r_{o2}]}{r_{o1} [1 + g_m r_{o2}] + r_{o2}}$$

If we can neglect r_{o2} in the denominator,

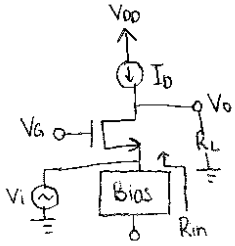
$$\approx -g_{m1}$$

and the resulting Norton equivalent is:



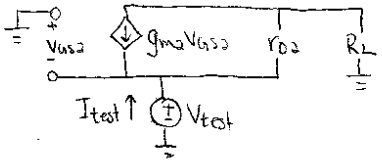
Input Resistance of the Common-Gate Amplifier

We looked at output resistance of the entire cascode amplifier, but what about one piece's input resistance? Let's take a look at the circuit.

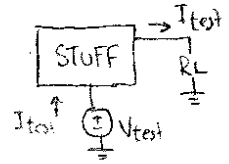


So instead of another MOS in cascode, we have some bias component with the input right above it, and some load resistance R_L on the output

We want to find the input resistance looking up into the source of the MOS. For the purpose of later use, we'll call our MOS M2.



The first thing to note is that if we black box the dependent source and r_{o2}:



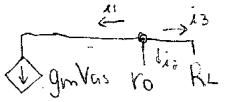
All current must come out of the drain and down into R_L, and as such we can calculate the voltage across it.

$$V_{RL} = I_{test} R_L$$

We also know the gate voltage and the source voltage, and we can find the gate-to-source voltage, and further, the generated dependent current from it.

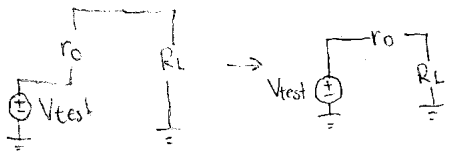
$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 0 - V_{test} \\ \therefore \quad g_m V_{GS} &= -g_m V_{test} \end{aligned}$$

Then, we can use KCL to find the current relationship



$$\begin{aligned} 0 &= i_1 + i_2 + i_3 \\ &= -g_m V_{test} - i_2 + I_{test} \\ i_2 &= -g_m V_{test} + I_{test} \end{aligned}$$

which is the current through r_o. Now, look closely at the configuration of the resistors and the test voltage.



It's clear that V_{test} will be the sum of the resistor voltages

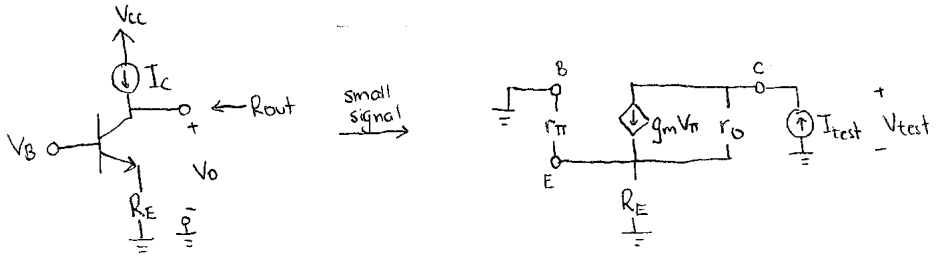
$$\begin{aligned} V_{test} &= V_{ro} + V_{RL} \\ V_{test} &= (-g_m V_{test} + I_{test}) r_o + I_{test} R_L \\ V_{test} &= -g_m V_{test} r_o + I_{test} r_o + I_{test} R_L \\ V_{test}(1 + g_m r_o) &= I_{test}(r_o + R_L) \end{aligned}$$

and as such the input resistance

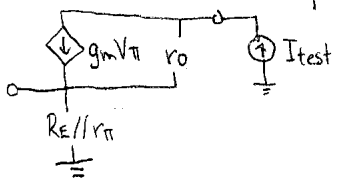
$$R_{in} = \frac{V_{test}}{I_{test}} = \frac{r_o + R_L}{1 + g_m r_o}$$

Output Resistance of Emitter-Degenerated Amplifier

Are you tired of MOSFETs? Well I am too, so we're going to repeat the same exercises with BJTs instead



Notice that r_π and R_E are in parallel. Let's redraw.



Whoa. Deja vu Isn't this just the source-degenerated MOSFET circuit. Recall it had the output resistance

$$R_{out} = r_{o1} + R_S + g_m r_{o1} R_S$$

So now we can simply replace R_S with $(R_E // r_\pi)$:

$$R_{out} = r_{o1} + (R_E // r_\pi) + g_m r_{o1} (R_E // r_\pi)$$

There's a few things that are important here, though, which differs from the MOS side of things First, as we increase R_E, $(R_E // r_\pi)$ approaches r_π.

$$R_{out}|_{max} = r_o + r_\pi + g_m r_\pi r_o$$

The second is $g_m = \frac{I_C}{V_T}$. The third is now r_π is expressed as well: $r_\pi = \frac{V_T}{I_B}$.

And as such: $g_m r_\pi = \frac{I_C}{V_T} \frac{V_T}{I_B}$

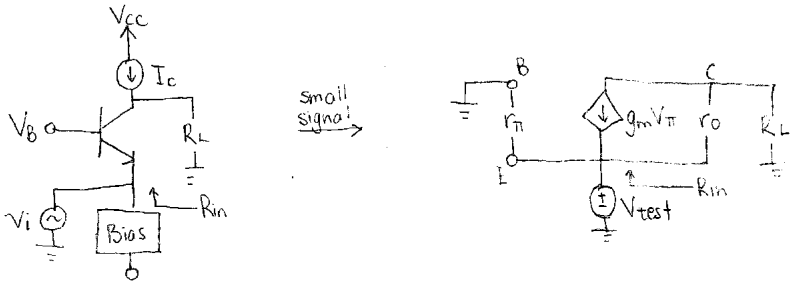
$= \frac{I_C}{I_B}$, which is the definition of β.

$\therefore R_{out} = r_o + r_\pi + \beta r_o$

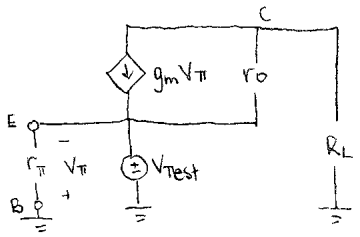
Which means there's a theoretical upper limit to the output resistance, determined by the hardware, when using this configuration.

Input Resistance of Biased Common-Base Amplifier

Following finding the output resistance, we can also find the input resistance looking into the emitter of a BJT. Let's look at the circuit.

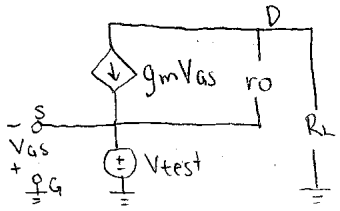


Once again, we cut all of our independent sources and we've pre-emptively attached our test voltage source. Of course, we could've used a current source as well, but it doesn't really matter. Let's redraw the circuit so it's a bit easier to see the relationship between voltages.



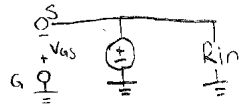
(hybrid-π BJT)

Whoa. Hold up a second. How did our small-signal common-gate MOS in small signal look?

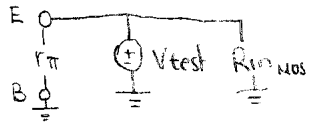


(hybrid-π MOS)

Where the MOS's $R_{in} = \left(\frac{r_o + R_L}{1 + g_m r_o}\right)$. Remember that the ENTIRE circuit represented by R_{in} can be turned into a single resistor with the same terminals. Note V_{test} is connected to the source and ground. As such:



Now, if we simplify the BJT the same way:

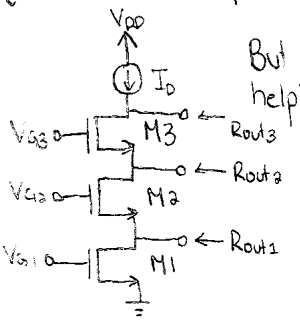


Then isn't our new R_{in} just $r_\pi // R_{in_{MOS}}$?

$$R_{in} = r_\pi // \left(\frac{r_o + R_L}{1 + g_m r_o}\right)$$

The Double Cascode

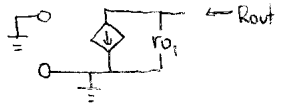
So, what happens if we have a need for an output resistance larger than $R_{out} = r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2}$? Simple → we just stack more transistors on



But exactly how much does this help?

The simplest way to go about figuring this out is to start at the bottom and work our way upwards

R_{out1}:



Small signal diagram as a reminder. $V_{GS} = 0$ ∴ current is 0 and as such R_{out1} is simply r_{o1}.

R_{out2}: We've solved this already to be

$$R_{out2} = R_{out1} + r_{o2} + g_{m2} R_{out1} r_{o2}$$
$$= r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2}$$

R_{out3}: So wouldn't this follow the same pattern?

$$R_{out3} = R_{out2} + r_{o3} + g_{m3} R_{out2} r_{o3}$$
$$= [r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2}] + r_{o3}$$
$$+ g_{m3} r_{o3} [r_{o1} + r_{o2} + g_{m2} r_{o1} r_{o2}]$$
$$= r_{o1} + r_{o2} + r_{o3} + g_{m2} r_{o1} r_{o2} +$$
$$g_{m3} r_{o3} r_{o2} + g_{m2} r_{o3} r_{o1} + g_{m3} g_{m2} r_{o1} r_{o2} r_{o3}$$

In the case where $r_{o1} \approx r_{o2} \approx r_{o3}$
$g_{m1} \approx g_{m2} \approx g_{m3}$

we can generalize this to

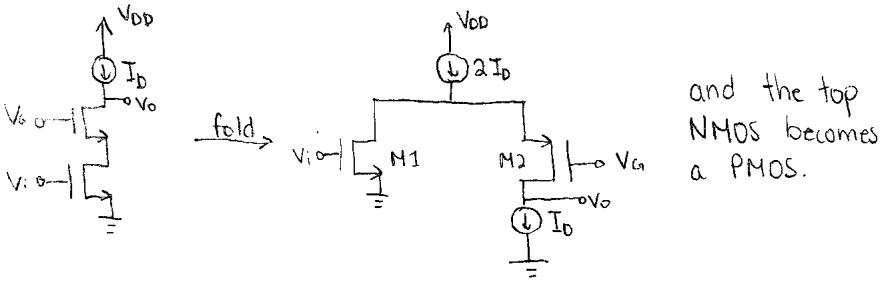
$$R_{out} = 3r_o + 3g_m r_o^2 + g_m^2 r_o^3$$
$$\approx g_m^3 r_o^3$$

if we wanted to be REALLY lazy about it.

However, stacking transistors isn't the end-all be-all of increasing output resistance. Remember that each transistor has a voltage across it required to keep it operating in saturation. As such, the more we have, the higher voltage V_{DD} / V_{SS} we have to supply.

The Folded Cascode Configuration

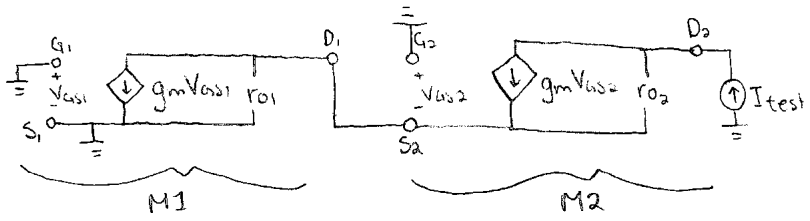
"Folding" a cascode lets us accomplish a few interesting goals. Firstly, note that the "fold" is where the transistors would normally be attached



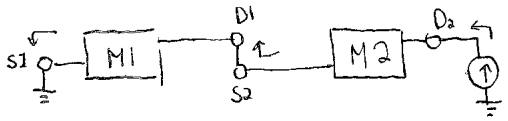
and the top NMOS becomes a PMOS.

This allows us to increase the input and output swing range and means that we can now connect Vo to other inputs to create the feedback loops that we so love. (Remember their prolific use in op-amps)

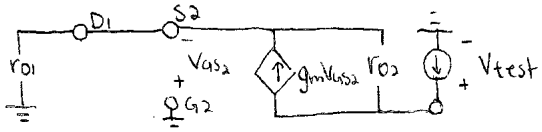
Let's find the output resistance here. Since it's an unfamiliar configuration, we'll draw the entire small-signal model. Of course, as always, we'll turn off independent sources and attach our test source.



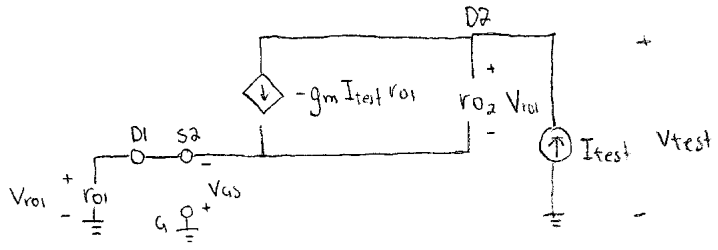
It may be obvious already, but let's make it even more obvious how the test current will flow.



As you can see, we MUST have Itest flowing through S1, D2, and the D1-S2 connection. $g_m V_{gs1}$ is 0, notice, as the V_{gs1} is a ground-to-ground difference. Let's redraw.



Hold up. $-V_{gs2}$ is simply the voltage across r_{o1}. Obviously all of Itest must flow through it, making its voltage $V_{ro1} = (I_{test})r_{o1} = -V_{gs2}$. As follows, the current generated is $g_m(-I_{test})r_{o1}$. But let's redraw again so we can take a look at the voltages in a nicer way.



Now, it's much clearer that $V_{test} = V_{ro1} + V_{ro2}$. We can now do KCL at D2 to determine how much current goes into r_{o2}. Define outwards as positive

$$0 = i_1 + i_2 + i_3$$
$$0 = -g_m I_{test} r_{o1} + i_2 - I_{test}$$
$$i_2 = I_{test}(g_m r_{o1} + 1)$$

And as such its voltage, and the thevenin voltage, is $I_{test}(g_m r_{o1} + 1) r_{o2}$.

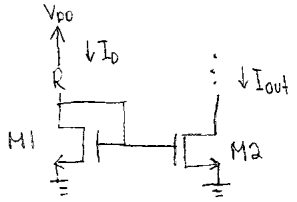
$$\therefore R_{out} = \frac{V_{TH}}{I_{test}} = \frac{I_{test}(g_m r_{o1} + 1) r_{o2}}{I_{test}} = (g_m r_{o1} + 1) r_{o2}$$

Of course, this process can be repeated for any other situations - perhaps the sources are non-ideal and have finite resistances of their own.

The important thing to recognize is that if part of the circuit can be reduced to an already-known resistance, that will make analysis much easier.

The MOS Current Mirror

The name's got it all. We mirror current from one side of this circuit to other. But why do we use them? Current sources aren't very space-efficient, so we can use current mirrors to imitate these sources.



So the first thing to note is that the D1 is connected to G1 which is connected to G2.

Due to this, $V_{GS1} = V_{DS1}$, and as such,

$$V_{DS} \geq V_{GS} - V_t$$
$$V_D \geq V_G - V_t$$
$$0 \geq -V_t,$$

the saturation condition for M1 is always true, therefore our current coming in can be guaranteed

$$I_D = \frac{\mu_n C_{ox} (W/L)}{2} [V_{GS} - V_t]^2$$

Also, since the gates are tied together, and the sources are both grounded, their V_{GS} must be equal.

It's also safe to assume M2 is also in saturation as it doesn't make sense to design configurations like this in triode (god help us if you design with cutoff)

As such, current through both drains and sources can be expressed using the saturation current equation, and their ratios are given as such:

$$\frac{I_{out}}{I_D} = \frac{(1/2)\mu_{n2}C_{ox2}(W/L)_2[V_{GS}-V_{t2}]^2}{(1/2)\mu_{n1}C_{ox1}(W/L)_1[V_{GS}-V_{t1}]^2}$$

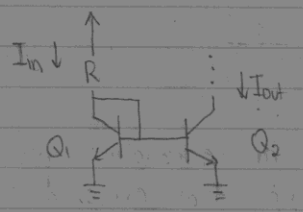
Given the situation where M1 = M2 except for the ratios of widths and lengths, the current gain is

$$\frac{I_{out}}{I_D} = \frac{(W/L)_2}{(W/L)_1}$$

simply the ratio of (the ratio of width and length)s. So given two transistors that are exactly the same, the generated current is exactly that of the input.

The BJT Current Mirror

As always, the law of 242 dictates that anything a MOS can do, a BJT can do, too, so:



Again, the extra wire forces Q_1 to be active, and it is safe to assume Q_2 also operates in that region.

Recall that active collector-emitter current is given by

$$I_c = I_s e^{V_{BE}/V_T}$$

where I_s is the reverse saturation current, a hardware property.

Hilroy

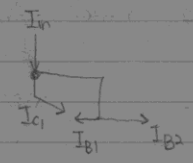
Of course, e and V_T are also parameters we have no control over. We've tied the bases together, so base-emitter voltage is equal. As such:

$$\frac{I_{C1}}{I_{C2}} = \frac{I_{SQ1}}{I_{SQ2}}$$

But remember, this isn't the end of the story. BJTs have a finite amount of base current, and as such,

I_{in} = collector current + base current

Where we have both base currents of each BJT flowing away from Q_1's collector.



$$I_{in} = I_{C1} + I_{B1} + I_{B2}$$
$$= I_{C1} + 2(I_{C1}/\beta)$$

The output current is simply the current in Q_2's collector, which means the gain

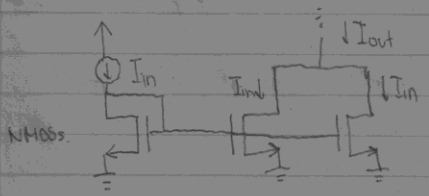
$$\frac{I_{out}}{I_{in}} = \frac{I_{C2}}{I_{C1} + 2\left(\frac{I_{C1}}{\beta}\right)} = \frac{1}{1 + 2/\beta}$$

If we assume the collector currents are essentially equal, where we're left with a small "error" that arises due to the base currents.

Multiple Current Mirrors

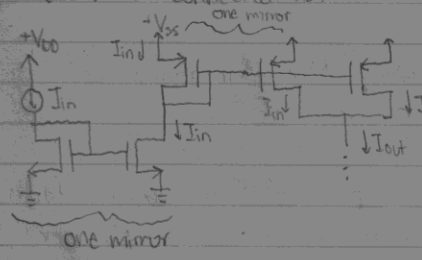
Now, it's fairly clear that current mirrors are highly useful for reflecting current at a 1:1 ratio, but what about if we wanted 1:2 or 1:3, or even 1:n?

Assuming that we only have one transistor with a fixed set of hardware parameters, the simplest thing to do is short the drains/collectors together.



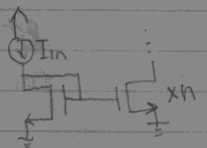
Even without doing an indepth analysis, assuming the transistors are perfectly matched, they will each pull Iin of current down

And as such, by shorting the drains together, it's clear a total of 2Iin must be pulled down from the circuit this short is connected to.



In this larger circuit, the basic NMOS mirror (a sink) is connected to a PMOS mirror (a source), where there are two PMOSs, so they source 2Iin current to the circuit below

Of course, more transistors can be connected to provide more current, and large amounts are generally simplified as



Hilroy

However, like everything, there are limitations to current mirrors

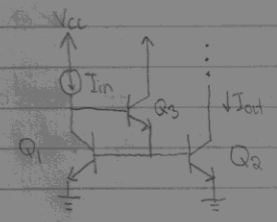
1) Current ratios are dependent on how well individual transistors match
2) There is a limited voltage range the circuit can handle dictated by the regions of operation.
   For example, a MOS must always have: $V_{DS} \geq V_{GS} - V_t$
3) For BJTs, the base currents cause slight imbalance in the mirror. This error becomes larger the higher the # BJTs are involved.
4) These have a finite output resistance. Ideally, this would be infinite.

Improving the BJT Current Mirror

As we mentioned before, the performance of the BJT mirror decreases with the number involved. If we did the analysis (though it makes sense even without it)

$\frac{I_{out}}{I_{in}} = \frac{1}{1 + \frac{N+2}{\beta}}$, where N is the number of additional BJTs

Now, how can we solve this problem? Since our de facto answer is always more transistors, lets shove another BJT in the base - collector wire



There's two important BJT equations to recall here: $I_C = \beta I_B$

$I_E = (\beta + 1) I_B$

so what our new BJT does is amplify the base current.

Let's work backwards from the output. Firstly, $I_{out} = I_{C2}$, which must mean there is a base current in Q2 if its collector current is non-zero, of $I_{B2} = \frac{I_{C2}}{\beta}$.

The same is true of Q1, so it must also have a base current of $\frac{I_{C1}}{\beta}$. By KCL it follows that our new BJT has emitter current $\frac{I_{C1} + I_{C2}}{\beta}$.

Then, we can calculate Q3's base current in the same fashion: $I_{B3} = \frac{1}{\beta+1} \frac{I_{C1} + I_{C2}}{\beta}$.

So, I_{in} must be the sum of Q3's base and Q1's collector.

$$I_{in} = I_{C1} + \frac{I_{C1} + I_{C2}}{\beta(\beta+1)}$$

And from here, we can find our new current gain

$$\frac{I_{out}}{I_{in}} = \frac{I_{C2}}{I_{C1} + \left(\frac{I_{C1} + I_{C2}}{\beta(\beta+1)}\right)} = \frac{1}{1 + 2/\beta^2 + \beta}$$

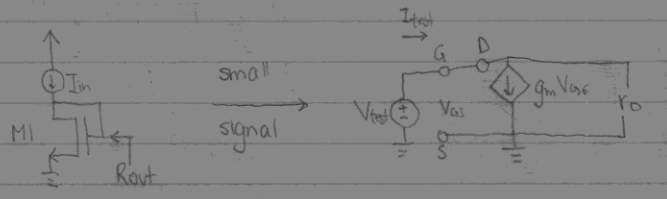
which is a much better match.

Now, to address another problem: possibly low, finite output resistances. Do you remember what we learned at the start?

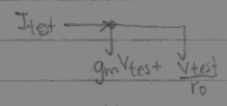
HWray

Small-Signal Diode-Connected Devices

Before we move on, it's important that we actually do a small-signal analysis on diode-connected devices, as it will bring forth a very powerful simplification of the circuit.



We can see V_{test} is in parallel with V_{gs}, so $V_{gs} = V_{test}$, and the source generates $g_m V_{test}$ of current. Of course, this V_{test} is reflected to r_o as well. As such, we now have two components generating current, and both must go towards ground. It is clear that



$$I_{test} = g_m V_{test} + \frac{V_{test}}{r_o}$$

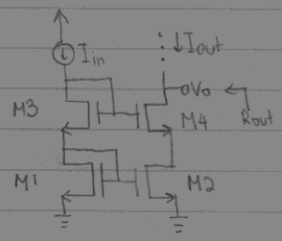
$$= V_{test}\left(g_m + 1/r_o\right)$$

$$\therefore \frac{V_{test}}{I_{test}} = R_{out} = \frac{1}{g_m + 1/r_o} \approx \frac{1}{g_m}$$

So a diode-connected MOS can be expressed simply as a resistor with resistance $\frac{1}{g_m + 1/r_o}$ in small signal.

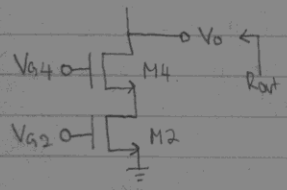
Now, let's move back to the topic at hand.

Cascode Current Mirrors



To solve the problem, we're introducing the cascode current mirror.

The most important thing to note is that looking into the output terminal, there isn't actually a way for current to reach M1 and M3, so we must conclude that those two won't affect the output resistance at all. So let's redraw with the left half removed.



Wait, what's this? It looks just like a regular cascode circuit!

We've already solved this to be:

$$R_{out} = r_{o\,bottom} + r_{o\,top} + g_m r_{o\,bottom} r_{o\,top}$$

$$\therefore \quad R_{out} = r_{o2} + r_{o4} + g_m r_{o2} r_{o4}$$

But again, every circuit is give-and-take. V_{g4} has to be large enough to put both M4 and M2 into saturation, so

$$V_{g4} = 2V_{as}$$
$$= 2V_t + 2V_{ov}$$

Since the output is at the drain, and

$$V_{as} \geq V_{as} - V_t$$

this sets a lower limit for our output voltage.

Hilroy

$$V_{DS} \geq V_{GS} - V_t$$
$$V_D > V_G - V_t$$
$$V_{D\min} = V_{G4} - V_t$$
$$= V_t + 2V_{ov}$$

in order for the MOSs to stay in saturation and keep our high output resistance.

The Differential Signal

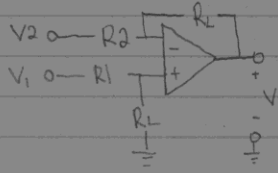
First, we have to learn some terminology.

Single-ended:  Measured between a single node and ground, where ground is a constant potential

Differential signal:  Measured between two non-constant nodes

Common-mode signal: The signal that is applied to both nodes, taken as the average of the two potentials: $V_{cm} = \frac{V_1 + V_2}{2}$

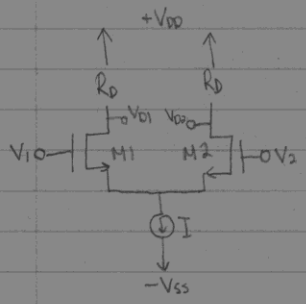
The motivation for the differential pair comes from a component configuration from 240: The differential amplifier.



$$V_o = \frac{R_2}{R_1}(V_1 - V_2)$$

So how do we go about replicating this functionality with transistors?

The MOSFET Differential Pair



For the sake of simplicity, we'll assume that the MOSFETS are matched perfectly, and in saturation

We apply gate voltages V_1 and V_2 to each MOS, and measure the resulting voltage as the difference of the drain voltages.

Can we prove that this circuit acts similarly to the differential amplifier? Let's vary our inputs and see what happens.

1) V_1 and V_2 are both 0V.

The gates and sources are both equal, meaning $V_{GS1} = V_{GS2}$. As such, the generated currents, I_{DS1} and I_{DS2}, must be equal as well (as they are perfectly matched).

Note the current source at the bottom that forces the sum of the currents to be I, and as such, each side must provide ½ I current.

This means the voltage drop across R_D must be $\frac{1}{2} I R_D$, and both $V_{O1} = V_{O2} = V_{DD} - \frac{1}{2} I R_D$.

∴ the difference is 0, so it responds correctly to no inputs.

2) V_1 and V_2 are equal, but non-zero.

Obviously, the gate voltages of both devices are still equal, and in turn, $V_{GS1} = V_{GS2}$, which generate equal currents.

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The total current still needs to be I, so each side provides ½ I.

This means there is a constant voltage drop across each resistor equal to ½ I R_D, which implies the drain voltages don't change. They're still equal.

∴ The circuit responds correctly to a common mode voltage, providing an output of 0 V

3) V_1 and V_2 are not equal (assume $V_1 > V_2$).

Since the gate voltage of M1 is higher, $V_{GS1} > V_{GS2}$, which generates different currents.

HOWEVER, the sum is still forced to be I, so I_{D1} and I_{D2} must equal I. We'll call the difference ΔI.

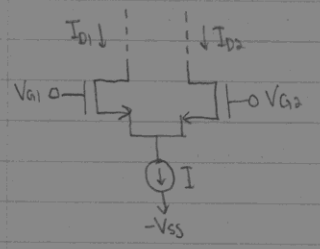
As such, the voltages across the resistors are unequal, now given by $V_{RD} = R_D(\frac{1}{2} I \pm \frac{1}{2}\Delta I)$ where + and − are for M1 and M2 respectively.

This means $V_{D1} = V_{DD} - R_D(\frac{1}{2}I + \frac{1}{2}\Delta I)$

$V_{D2} = V_{DD} - R_D(\frac{1}{2}I - \frac{1}{2}\Delta I)$

and the difference $V_{D1} - V_{D2} = -R_D \Delta I$, which is the proper response to a difference in inputs

Large Signal Behaviour of the MOS Differential Pair



So we want to find how the drain currents change based upon the difference of inputs.

We're going to define $V_{id} = V_{G1} - V_{G2}$.

Thankfully, Nairn/Sedra has done the analysis for us, and we're not expected to be able to reproduce it, so we'll take their word for it.

$$I_{D1} = \frac{I}{2} + \sqrt{kI}\,\frac{V_{id}}{2}\sqrt{1 - \left(\frac{V_{id}}{2\sqrt{I/k}}\right)^2}$$

$$I_{D2} = \frac{I}{2} - \sqrt{kI}\,\frac{V_{id}}{2}\sqrt{1 - \left(\frac{V_{id}}{2\sqrt{I/k}}\right)^2}$$

As we can see, if the differential input voltage $V_{id} = 0$, $I_{D1} = I_{D2} = I/2$.

Note that $I_{D1} = I/2 = \frac{1}{2} k (V_{ov})^2$

$$\rightarrow V_{ov} = \sqrt{\frac{I}{k}}$$ which we can substitute back in to get

$$I_D = \frac{I}{2} \pm \sqrt{kI}\,\frac{V_{id}}{2}\sqrt{1 - \left(\frac{V_{id}}{2V_{ov}}\right)^2}$$

Notice that as V_{id} increases, the amount of current will shift more and more to one side of the circuit. Eventually, $I_{D1} = I$ and $I_{D2} = 0$, when

$$V_{id} = \sqrt{2(I/k)}$$
$$= \sqrt{2}\,V_{ov}$$

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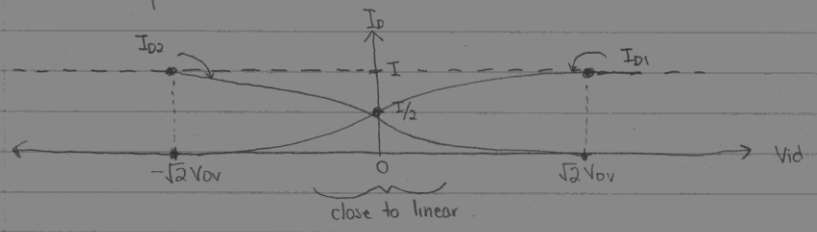
We can plot this characteristic as such:



Now, remember that g_m can be expressed as $2I_D/V_{ov}$, AND that we're currently in saturation.

$$g_m = \frac{2I_D}{V_{ov}}$$

$$= \frac{\mu_n C_{ox}(W/L)[V_{ov}]^2}{V_{ov}}$$

$$\therefore V_{ov} = \frac{g_m}{k}$$

Now, we can plug this back into our saturation current formula:

$$I_D = \tfrac{1}{2} k (g_m/k)^2 \quad \text{(this is just a general drain current)}$$

$$\sqrt{\frac{2I_D}{k}} = \frac{g_m}{k}$$

$$g_m = \sqrt{2kI_D}$$

where $I_D = \frac{1}{2}I \longrightarrow g_m = \sqrt{kI}$ and

$$I_D = \frac{I}{2} + \frac{g_m V_{id}}{2}\sqrt{1 - \left(\frac{V_{id}}{2V_{ov}}\right)^2}$$

DC Bias; Linear-acting gain; Distortion

Distortion is generally quite bad in AC, as if we square a sine wave: $[\cos(\omega t)]^2 = \frac{1}{2}[1+\cos(2\omega t)]$, we get a new wave of a totally different frequency.

Characterizing Distortion

So we know that ideally, distortion should be minimized wherever possible. But how much does it actually hurt us?

Recall we have $i_{D1} = \frac{I}{2} + g_m \frac{V_{id}}{2}\left(1 - \frac{1}{2}\left(\frac{V_{id}}{2V_{ov}}\right)^2\right)$

which can be rewritten as:

$$i_{D1} = \frac{I}{2} + \underbrace{\frac{g_m V_{id}}{2}}_{\text{linear}} - \underbrace{\frac{g_m V_{id}}{2}\left[\frac{1}{2}\left(\frac{V_{id}}{2V_{ov}}\right)^2\right]}_{\text{distorted}}$$

Where we can separate our current into linear and distortion signals, and compare their effects

$$\% \text{ Distortion} = \left(\frac{\text{Distortion}}{\text{Linear}}\right) 100\%$$

$$= \left(\frac{\frac{g_m V_{id}}{2}\left[\frac{1}{2}\left(\frac{V_{id}}{2V_{ov}}\right)^2\right]}{\frac{g_m V_{id}}{2}}\right) 100\%$$

$$= \frac{1}{2}\left(\frac{V_{id}}{2V_{ov}}\right)^2 100\%$$

And now, alternatively, we can solve for the input differential voltage given a percentage of distortion.

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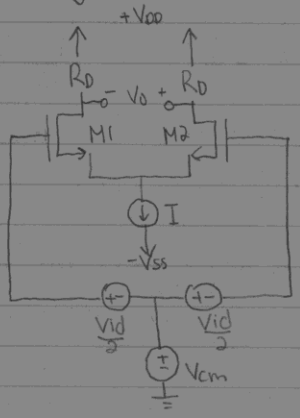
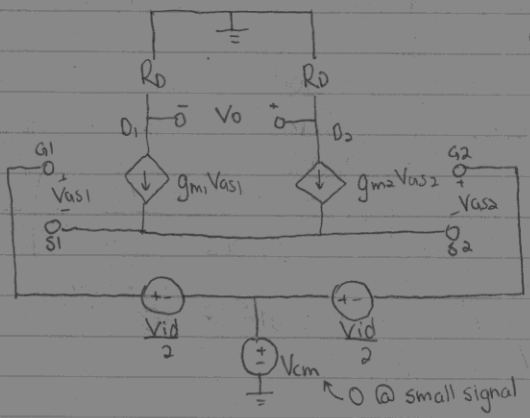
Small Signal Analysis of the MOS Differential Pair

We've done a lot of inspection analysis, so now it's time to crunch down and analyze the differential pair in small signal as an amplifier.



We apply both a differential input and a common mode input to the gates.

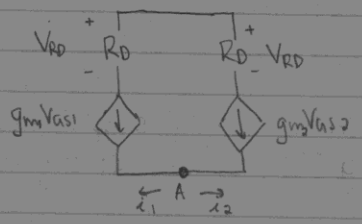


(small signal)

Firstly, the most important thing to remember is that current always does its best to flow in a loop. There's a ground in between the resistors, and though it may be tempting to say current flows into it, that's not actually the case. If it flows into ground, where does it come from? There's nowhere it can start, and as such, the only way

it can flow is the top loop

The second matter is: how much voltage is actually applied to each gate-source junction? The secret actually comes from the previous paragraph



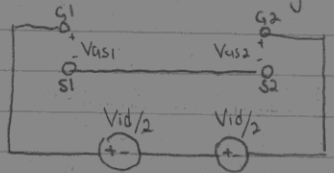
Let's do KCL at A. Define out as positive.

$$i_1 + i_2 = 0$$
$$-g_{m1} V_{GS1} + (-g_{m2} V_{GS2}) = 0$$
$$-g_{m1} V_{GS1} = g_{m2} V_{GS2}$$

As we can assume the transistors are matched,

$$V_{GS1} = -V_{GS2}$$

But, EXACTLY how much voltage is applied to this junction?



+2 for KVL.

$$V_{GS1} - V_{GS2} - Vid/2 - Vid/2 = 0$$
$$V_{GS1} - V_{GS2} = Vid$$
(since $V_{GS1} = -V_{GS2}$)
$$2V_{GS1} = Vid$$
$$V_{GS1} = \frac{Vid}{2} \quad \text{and} \quad V_{GS2} = -\frac{Vid}{2}$$

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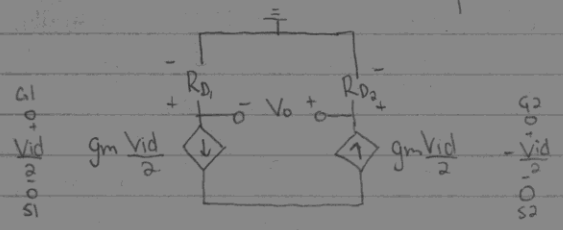
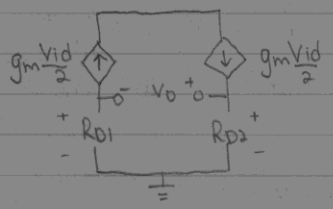
Now that we have V_{GS} for both transistors, we can redraw the circuit's middle portion.



And suddenly, we're left with a really simple circuit that generates a total $\frac{g_m V_{id}}{2}$ current, causing a voltage DROP in R_{D_2} and a voltage RISE in R_{D1}. Let's turn it on its head so the lower potential matches the orientation.



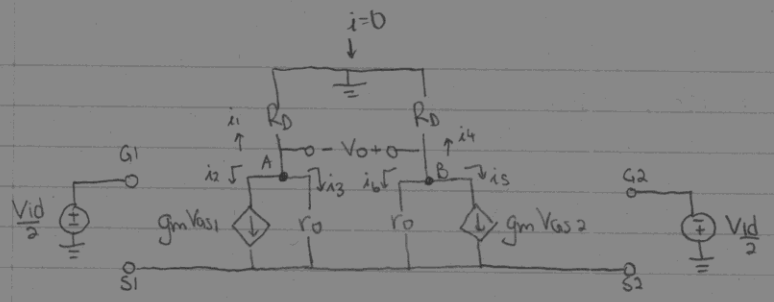
$$V_o^- = -\left(g_m \frac{V_{id}}{2}\right) R_{D1}$$

$$V_o^+ = g_m \frac{V_{id}}{2} R_{D2}$$

Which gives us $V_o = V_o^+ - V_o^-$, and voltage gain $A = g_m R_d$

$= g_m R_d V_{id}$

You may have noticed, though, our small-signal model isn't really complete: "Where is the finite output resistance of each transistor?" Let's do that now.



Alright, let's prove this through KCL. Remember there's still no accessible ground so current into it is still 0. Define outwards as positive.

Remember that R_{DS} can be considered as in series:

V_{D1} o—— R_{D1} ——— R_{D2} ——o V_{D2}

KCL @ A:
$$i_1 + i_2 + i_3 = 0$$
$$\left(\frac{V_{D1}-V_{D2}}{2R_D}\right) + g_m\frac{V_{id}}{2} + \frac{V_{D1}}{r_O} = 0$$

KCL @ B:
$$i_4 + i_5 + i_6 = 0$$
$$\left(\frac{V_{D2}-V_{D1}}{2R_D}\right) + g_m\left(\frac{-V_{id}}{2}\right) + \frac{V_{D2}}{r_O} = 0$$

Since they're both 0, we can equate them:

$$\left(\frac{V_{D1}-V_{D2}}{2R_D}\right) + g_m\frac{V_{id}}{2} + \frac{V_{D1}}{r_O} = \left(\frac{V_{D2}-V_{D1}}{2R_D}\right) - g_m\frac{V_{id}}{2} + \frac{V_{D2}}{r_O}$$

$$g_m\frac{V_{id}}{2} + g_m\frac{V_{id}}{2} = \left(\frac{V_{D2}-V_{D1}}{2R_D}\right) - \left(\frac{V_{D1}-V_{D2}}{2R_D}\right) + \frac{V_{D2}}{r_O} - \frac{V_{D1}}{r_O}$$

$$g_m V_{id} = \frac{V_{D2}-V_{D1}}{R_D} + \frac{V_{D2}-V_{D1}}{r_O}$$

$$= \frac{V_O}{R_D} + \frac{V_O}{r_O}$$

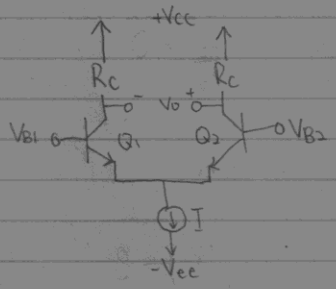
And as such our gain $A = \frac{V_o}{V_{id}}$ has changed to

$$A = \frac{V_o}{V_{id}}$$
$$= g_m \left[\frac{1}{R_D} + \frac{1}{r_o} \right]^{-1}$$
$$= g_m (R_D \,//\, r_o)$$

Which is a diminished gain from when we assumed the output resistance was infinite.

BJT Differential Amplifiers

What is this course if we're not duplicating functionality with BJTs? At this point I kind of wonder why people would use BJTs even with the deficiencies base currents cause, but oh well



Wow, spooky. We can assume the BJTs are in active mode, where $V_{B1} - V_{B2} = V_{id}$.

Recall $i_{C1} = \frac{I_S}{\alpha} e^{(V_{B1} - V_E)/V_T}$

$i_{C2} = \frac{I_S}{\alpha} e^{(V_{B2} - V_E)/V_T}$

We're going to do something a little odd here for the sake of large-signal analysis

$$\frac{i_{E1}}{i_{E2}} = e^{(V_{B1} - V_{B2})/V_T}$$

Which by some freaky magical math yields

$$\frac{i_{E1}}{i_{E1}+i_{E2}} = \frac{1}{1+e^{(V_{B2}-V_{B1})/V_T}}$$

$$\frac{i_{E2}}{i_{E1}+i_{E2}} = \frac{1}{1+e^{(V_{B1}-V_{B2})/V_T}}$$

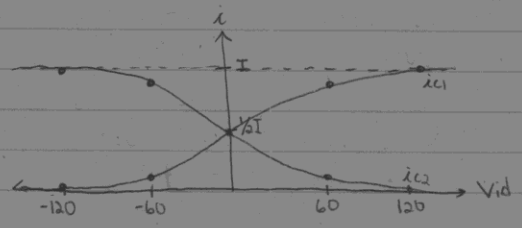
Now, remember total current out of the emitter must equal I due to the current source, and $V_{B1} - V_{B2} = V_{id}$.

$$\therefore\ i_{E2} = \frac{I}{1+e^{V_{id}/V_T}} \quad \text{and} \quad i_{C2} = \frac{\alpha I}{1+e^{V_{id}/V_T}}$$

$$i_{E1} = \frac{I}{1+e^{-V_{id}/V_T}} \qquad i_{C1} = \frac{\alpha I}{1+e^{-V_{id}/V_T}}$$

It's not quite as easy to dissect this function into linear / nonlinear pieces, so let's try plugging in some numbers instead

V_{id}	i_{C1}
0 mV	≈ 50% I
60 mV	≈ 90% I
120 mV	≈ 99% I



Input and Output Signal Swing

One important concept we haven't touched yet is "swing". Essentially, it states the minimum and maximum height a signal can be before it gets clamped by the supply or distorted due to inability to keep a component in its proper region

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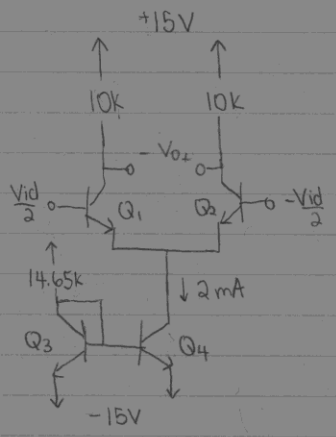

What we want to find here is output and input swing.

Remember that $A_d = \frac{V_o}{V_{id}}$,

so by finding two of these parameters will allow us to find the third.

Don't be intimidated by the bottom part of the circuit It's simply a current mirror. We are given the following

$V_{BE} = 0.7\ V$ for all Q_i $\quad V_A = 40\ V$ $\quad V_{cm} = 0\ V$
$V_{CE} = 0.7\ V$ for all Q_i $\quad \beta = 100$

1) DC Operating Point

The first thing to find is how the circuit reacts to no input.

Q_1's base = Q_2's base = 0V
$\therefore V_{BE_{1,2}} = -0.7\ V$

Because Vid is 0, the current splits equally, pulling 1mA in each branch this causes 10V voltage drops across each 10k resistor.

By the same virtue, Q_3 and Q_4's base must also have a voltage rise of 0.7 V, bringing them up to -14.3 V.

2) Output signal swing

We must make use of our DC operating point: the maximum of $V_o^{\pm}$ occurs when vid is large enough to force all 2 mA of current through a branch, meaning THE OTHER branch with no current has no voltage drops across the resistor.

$$\therefore \quad V_o^+{}_{max} = V_o^-{}_{max} = 15\,V$$

Now, in the opposite branch:

$$V_o^+{}_{min} = V_o^-{}_{min} = -5\,V$$

But wait: The ce voltage is now less than the be voltage, which means we're no longer in the active region: We're stuck at a minimum of 0V.

As such, the largest sine wave we can have at that node is $5V \pm 5V$, without getting out of active. And further, the biggest DIFFERENCE of voltages at the output is 20V.

So what can we do to increase the swing?
The first thing we can do is drop V_{cm} down to $-5V$, which allows us to take advantage of the maximum swing, of two 20Vpp signals, giving a largest difference of 40V.

Another way we can change this is lowering our bias current. For example, if I was lowered to 1.5 mA, the drop across the 10k resistors is 7.5 V when $V_{id} = 0$. This means (assuming $V_{cm} = 0$), so one signal can be 7.5 ± 7.5 V, giving us a maximum difference of 30V.

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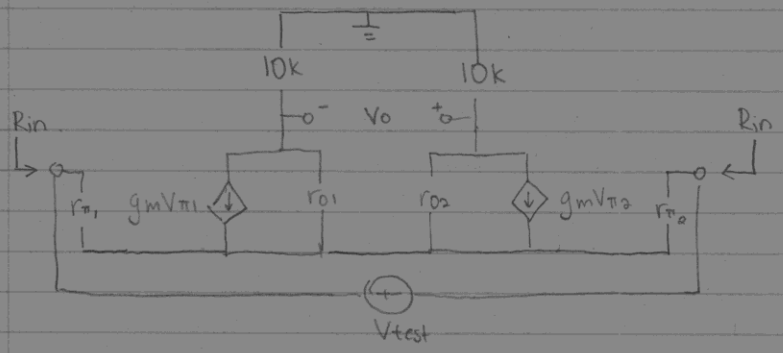
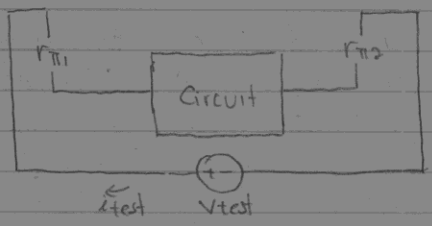
3) Input resistance into the bases

Let's draw the small signal model. Remember that we zero independent sources (Vcm AND the current mirror that acts as a source) and apply our test voltage.



There's a very simple trick to realize here that makes analysis really easy. It goes back to the fact that the ground at the top doesn't have any current going through it, so ALL current MUST go through both $r_{\pi 1}$ and $r_{\pi 2}$.

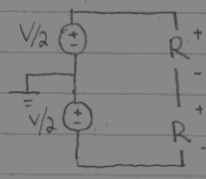


So no matter how many times the current flows through the loop in the middle, it must always exit through and enter into r_π.

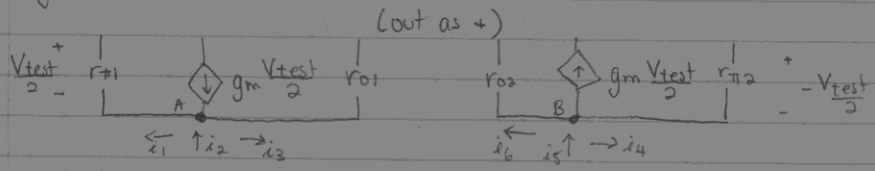
$\therefore R_{in} = 2r_\pi$, if they're equal.

Okay, okay, maybe that isn't enough to convince you, so let's do some KCL. We'll keep in mind an important assumption:

The circuit's input is correctly balanced such that the node between r_{o1} and r_{o2} is a SIGNAL GROUND (a fake one like the one at the top), meaning that that node is a constant 0V. Let's look at a simplified example.



Note that through voltage division, each resistor is given its corresponding voltage, and the voltage between is 0V. Note also that the net current in between is also 0A, as the top R generates V/2R and the bottom generates -V/2R. Let's go back.



KCL @ A: $i_1 + i_2 + i_3 = 0$

$$-\left(\frac{V_{test}}{2r_{\pi 1}}\right) - \left(\frac{g_m V_{test}}{2}\right) + i_3 = 0$$

$$i_3 = \frac{V_{test}}{2}\left(\frac{1}{r_{\pi 1}} + g_m\right)$$

KCL @ B: $i_4 + i_5 + i_6 = 0$

$$\left(\frac{V_{test}}{2r_{\pi 2}}\right) + \left(\frac{g_m V_{test}}{2}\right) + i_6 = 0$$

$$i_6 = -\frac{V_{test}}{2}\left(\frac{1}{r_{\pi 2}} + g_m\right)$$

Hilroy

where i_6 is clearly $-i_3$, so current in, current out; So the world goes.

$$\therefore I_{test} = \frac{V_{test}}{2}\left(\frac{1}{r_\pi} + g_m\right)$$

$$2\left(\frac{1}{g_m} + r_\pi\right) = \frac{V_{test}}{I_{test}}$$

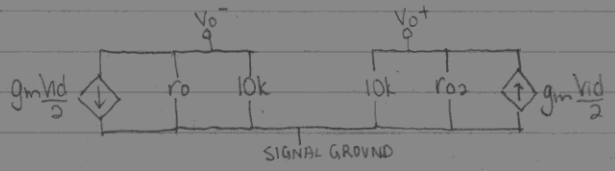
$$R_{TH} = \frac{2}{g_m} + 2r_\pi$$

which is essentially just $2r_\pi$ due to $2/g_m$ being very small.

4) Differential voltage gain

Let's go back to our assumption that we have $g_m(v_{id}/2)$ current flowing down on the left side and $g_m(v_{id}/2)$ flowing up on the other.

Remember that in between each r_o and 10k resistor, there is a signal ground. If we redraw, it could look like this:



It's pretty plain to see that each half contains an r_o and a 10k in parallel, and in conclusion

$$V_o^+ = g_m\, v_{id}/2\, [r_o // 10k]$$
$$V_o^- = -g_m\, v_{id}/2\, [r_o // 10k]$$

and further.

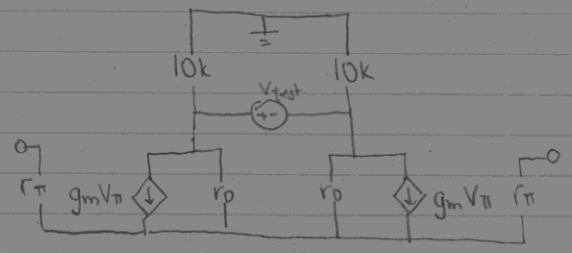
$$V_o = V_o^+ - V_o^-$$
$$= 2g_m \frac{V_{id}}{2} [r_o /\!/ 10k]$$
$$= g_m V_{id} [r_o /\!/ 10k]$$

and from here we can calculate our differential gain

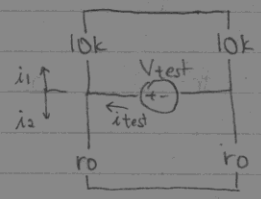
$$\frac{V_o}{V_{id}} = g_m [r_o /\!/ 10k]$$

5) Output resistance

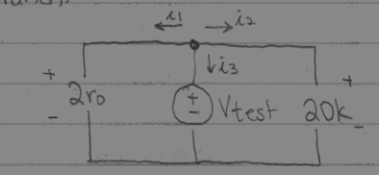
We should be familiar with the methodology by now. Cut independent sources, dump a test source between the output's terminals. Let's do that.



Right off the bat we can ignore r_π because current can't flow into those terminals. Then, we can disregard the dependent sources because there is now no voltage drop across r_π. Let's redraw.



Now, all we're left with is three parallel branches, and i_{test} is simply the current generated across each branch.



$$-i_3 = i_1 + i_2$$

$$= \frac{V_{test}}{2r_o} + \frac{V_{test}}{20k}$$

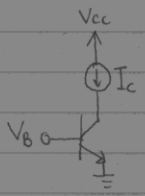
$$i_{test} = -V_{test}\left(\frac{1}{2r_o} + \frac{1}{20k}\right)$$

$$\frac{V_{test}}{i_{test}} = \left[\frac{1}{2r_o} + \frac{1}{20k}\right]^{-1}$$

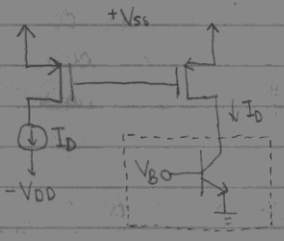
$$R_{TH} = (r_o + r_o) \,//\, (10k + 10k)$$

Active Loads

So what active loads are never really got explained, so here is Wikipedia's take on it. "An active load is a component or a circuit that functions as a current-stable, non-linear resistor".

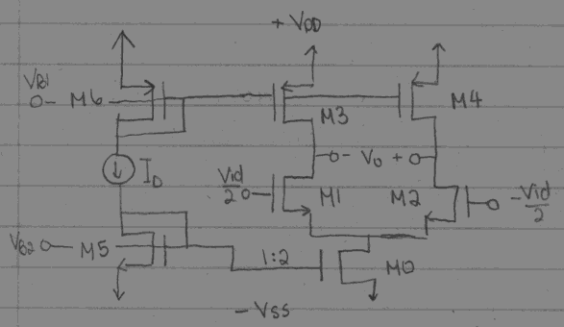


For example, in this basic common-emitter circuit, the current source REPRESENTS an active load. We could expand this.



Here, we've replaced a current source with a MOS current mirror. Due to non-linear properties of transistors, the current mirror is the active load.

Now, what if we're given a more complicated circuit?



For the sake of simplicity, we'll assume that all the transistors are to be biased in saturation.

Like all normal analysis questions, we'll solve for the differential voltage gain A_d, and the output and input resistances looking into their respective terminals.

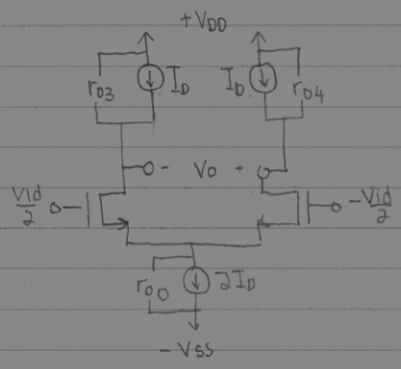
First thing's first (I'll eatcho brains... Sorry, listening to Nicki Minaj) let's see what we can identify from this circuit.

We've got M6 that mirrors I_D current into both M3 and M4. M5 does the same, at a 1:2 ratio, mirroring $2I_D$ into M0. One of the biggest things to remember about this circuit is that no current can enter into the gate of a transistor, so M6 and M5 are essentially an entire separate circuit.

The next thing to take note of is that mirrored MOSs work as non-ideal current sources and sinks, so we could replace M3 and M4 with non-ideal current sources of I_D, and M0 with a non-ideal current sink of $2I_D$.

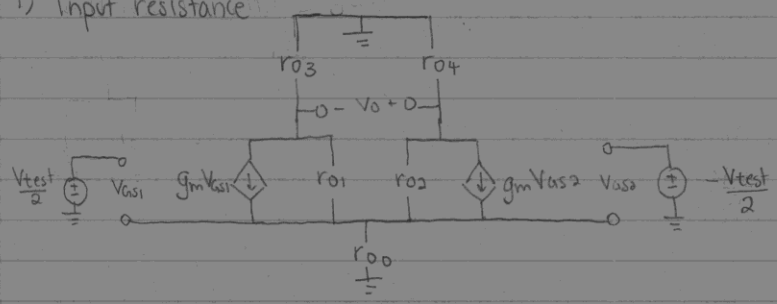
What we're left with is actually a rather tame, uninteresting circuit.

Milroy



which we can redraw in small signal:

1) Input resistance



Remember, due to the balance of the circuit, no current actually flows into/out of r_{oo}, so we could really erase it and nothing would change.

As for the input resistance... Well, no current can go into the gates, so it's ∞.

2) Output Resistance and Differential Voltage Gain

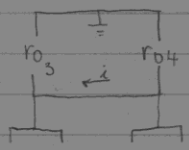
We're going to do things a little differently this time around and make use of this relationship.

$$I_{sc} = \frac{\Delta V_{id}}{R_{out}} = G_v v_{id} \longrightarrow G_1 = \frac{A}{R_{out}}, \text{ and } R_{out} = \frac{V_{oc}}{I_{sc}}$$

Where I_{sc} is the short circuit current and V_{oc} is the open circuit voltage.

The differential output is already open circuit, so $V_o = V_{oc}$.

The short circuit current is fairly simple, too.



Notice how current avoids the two resistors at the top altogether.

The dependent sources each provide $g_m\left(\frac{V_{id}}{2}\right)$ current, and since all the current can do is have itself a nice ring around the rosy through the middle loop, the short circuit current must be just the same.

$$i_{sc} = g_m \, V_{id}/2$$

$$\frac{i_{sc}}{V_{id}} = \frac{g_m}{2}$$

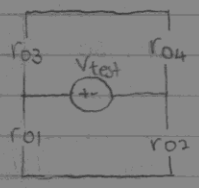
Since $i_{sc} = G V_{id}$, we can conclude

$$G = \frac{g_m}{2}$$

Finally, the last part of the puzzle required is the output resistance, which we can get by cutting sources and replacing our output with a test source.

Remember what happened before? $V_{as} = 0$ meaning the sources don't provide any current, either. So the only current comes from our test source, and only goes through the resistors, avoiding the "grounds" due to the balance of the circuit. Maybe a re-sketch will help.

Hilroy



And you can almost read the resistance right off the page.

$$R_{out} = (r_{O3} + r_{O4}) \,//\, (r_{O1} + r_{O2})$$

If you need a reminder of how this works, go back a couple of pages. We've got all of our pieces, now.

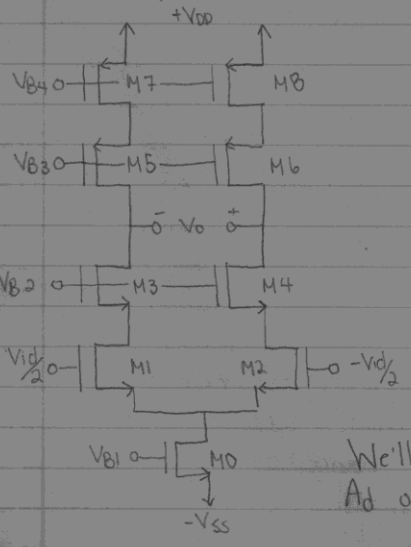
$$G = \frac{A}{R_{out}}$$

$$A = G R_{out}$$

$$= \frac{g_m}{2} \left[(r_{O3} + r_{O4}) \,//\, (r_{O1} + r_{O2}) \right]$$

This analysis can be applied to even more convoluted circuits with active loads.

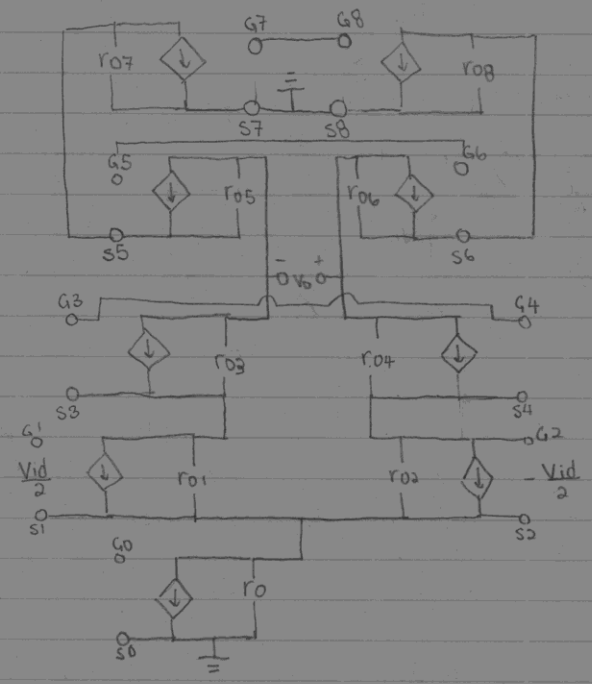
Telescopic Cascode Amplifier



Once again, we can assume the circuit is in saturation for simplicity's sake.

But, since this is something fairly novel and complex, let's small-signal this entire monstrosity and see what happens.

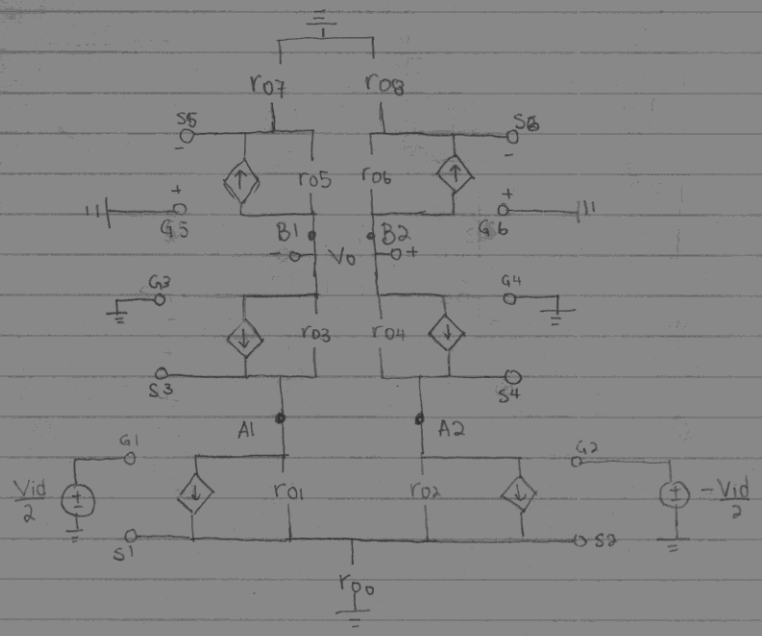
We'll be looking for R_{in}, R_{out}, and A_d once again.



All dependent sources are the standard $g_m V_{GSi}$. All non-small signal gate voltages are set to 0, so anywhere where sources are 0 will guarantee that transistor is reduced to a single resistor due to the sources providing 0 current.

The transistors that fit this description are: M7 and M8 (sources connected to -Vss), and M0 (source connected to -Vss)

Let's redraw and see how this circuit resolves.



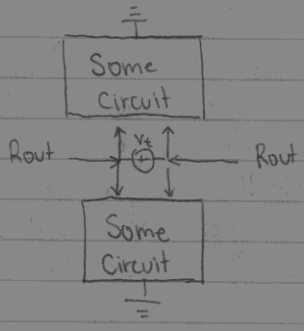
Phew. I flipped some transistors upside-down for better readability. By symmetry and balance, we can once again conclude that no current flows in or out of the signal grounds at the top and bottom.

1) Input Resistance

As with all inputs based at the gates of a MOS, this is ∞.

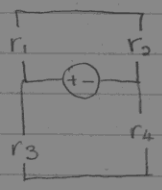
2) Differential Voltage Gain and Output Resistance

Let's find the output resistance first, because it seems like it may be easier. Now, the process of this is a little odd, so bear with me. Remember, we're looking into the V_o^- and V_o^+ terminals.



Look at this somewhat confusing diagram.

The top half is in parallel with the bottom half, and all components within each half are in series.



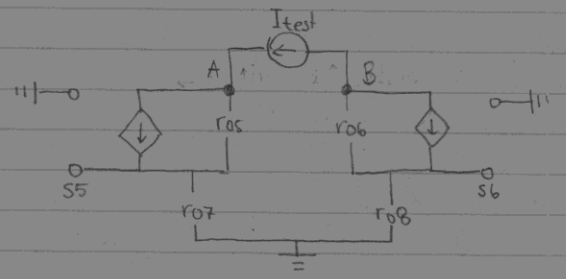
Remember this? Its

$R_{out} = (r_1 + r_2) \,//\, (r_3 + r_4)$

Exact same idea here.

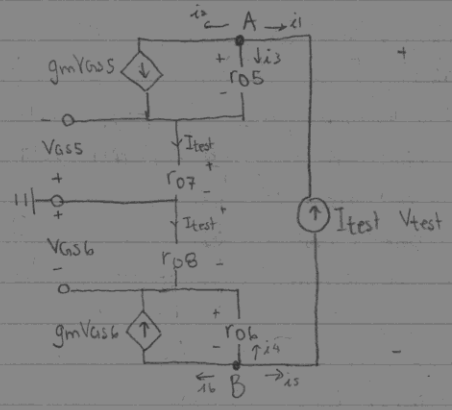
So, in that vein, let's look at the circuit one half at a time.

2a) Top Half Output Resistance



Though this is actually okay, I'm going to redraw this top half of the circuit in another way that I think is more intuitive.

Hilroy



Personally, I find this a lot clearer because position-wise, the circuit is aligned top-to-bottom for higher voltages to lower ones.

Remembering that the ground is simply a signal ground allows us to conclude that there is an $I_{test}(r_{07}, r_{08})$ voltage drop across those resistors.

$$\therefore V_{s5} = I_{test} r_{07} \longrightarrow V_{gs5} = -I_{test} r_{07}$$
$$V_{s6} = -I_{test} r_{08} \qquad V_{gs6} = +I_{test} r_{08}$$

$$\longrightarrow g_m V_{gs5} = -g_m I_{test} r_{07}$$
$$g_m V_{gs6} = g_m I_{test} r_{08}$$

Which of course means the current into r_{05} and r_{06} are a result that can be calculated through KCL.

A: $i_1 + i_2 + i_3 = 0$

$-I_{test} + (-g_m I_{test} r_{07}) + i_3 = 0$

$i_3 = I_{test} + g_m I_{test} r_{07}$

B: $i_4 + i_5 + i_6 = 0$

$i_4 + I_{test} + g_m I_{test} r_{08} = 0$

$i_4 = -I_{test} - g_m I_{test} r_{08}$

So the voltages across those resistors is

$$V_{r05} = I_{test} r_{05}(1 + g_m r_{07})$$
$$V_{r06} = -I_{test} r_{06}(1 + g_m r_{08})$$

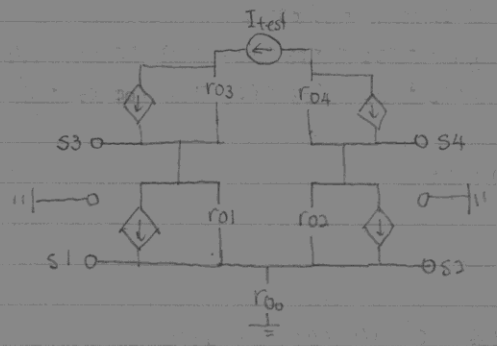
Now, we've got everything we need to calculate Vtest, the voltage difference between A and B.

$$\begin{aligned} V_{test} &= V_A - V_B \\ &= (V_{ro5} + V_{s5}) - (V_{ro6} + V_{s6}) \\ &= (I_{test} r_{o5} + I_{test} r_{o5} r_{o7} g_m + I_{test} r_{o7}) \\ &\quad - (-I_{test} r_{o6} - I_{test} g_m r_{o6} r_{o8} - I_{test} r_{o8}) \\ &= I_{test} (r_{o5} + g_m r_{o5} r_{o7} + r_{o7} + r_{o6} + \\ &\qquad g_m r_{o6} r_{o8} + r_{o8}) \end{aligned}$$

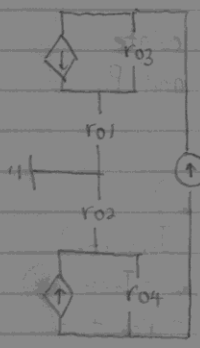
$$\therefore \quad \frac{V_{test}}{I_{test}} = R_{out} = [r_{o5} + r_{o7} + g_m r_{o5} r_{o7}] + [r_{o6} + r_{o8} + g_m r_{o6} r_{o8}]$$

Which makes quite a bit of sense as the circuit is really just cascode circuits in series.

2b) Bottom Half Output Resistance



Remembering that no current goes into r_{o0}, due to the balanced nature of the circuit, we can remove it from the circuit, effectively setting S1/S2 to 0V, thereby turning their dependent sources off and reducing those transistors to finite output resistances. Let's redraw.



WOW, WACKY. It reduces to the exact same thing we had before, two cascode resistances in series.

So without any further calculation, we can simply state that

$$R_{out} = r_{o1} + r_{o3} + g_m r_{o1} r_{o3} + r_{o2} + r_{o4} + g_m r_{o2} r_{o4}$$

2c) Putting it together

$$R_{out} = R_{out\,top} \,//\, R_{out\,bot}$$
$$= [r_{o1} + r_{o2} + r_{o3} + r_{o4} + g_m r_{o1} r_{o3} + g_m r_{o2} r_{o4}] \,//\, [r_{o5} + r_{o6} + r_{o7} + r_{o8} + g_m r_{o5} r_{o7} + g_m r_{o6} r_{o8}]$$

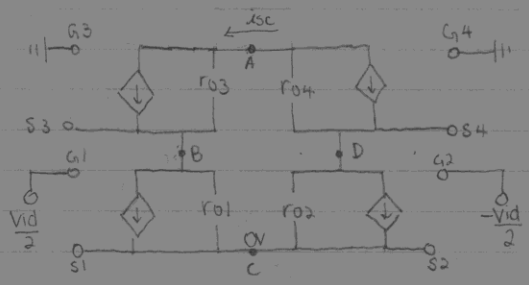
3) Differential Voltage Gain

Again, let's find

$$G = \frac{i_{sc}}{v_{id}} \quad \text{so we can calculate}$$

$$A_d = G R_{out}$$

By replacing Vo's terminals with a short circuit, we can immediately ignore everything above it, as no current will go into there.



Once again, invoke balanced circuit assumption, rendering the sources of S1 and S2 to 0V.

This causes g_m Vid/2 current ↓ in M1
g_m vid/2 current ↑ in M2

Notice that at A, B, C, and D, the current flowing through that area must be the short circuit current as well.