Notes importantes concernant le logiciel Altium

1-) Exportation des schémas et graphiques

Menu → Tools → Copy to clipboard

2-) LF444 et SSM2135

Cette note a pour but de vous indiquer comment instancier dans Altium les amplificateurs opérationnels que l'on retrouve dans l'APP6. Ceci est essentiel étant donné que ces composants se retrouvent dans plusieurs librairies, n'ayant pas tous un modèle associé pour faire des simulations.

1. Suivre les indications à la section 1.3.2 du document S2_H11_Atelier_AltiumDesigner.pdf en vous assurant de choisir l'option *Libraries on Path.* De plus, assurez-vous d'utiliser l'opérateur *contains* et non *equals.* Faire la recherche pour l'amplificateur opérationnel désiré.

Pour le LF444, faire la recherche pour **LF444ACN** (librairie *NSC Amplifier.IntLib*)

Pour le SSM2135, faire la recherche pour **SSM2135S** (librairie *AD Operational Amplifier.IntLib*)

2. Ensuite, avec le menu du bouton droit lorsque le pointeur de la souris est sur le nom de la composante choisir *Install Current Library*.

3-) Note concernant les potentiomètres RvxA de 20kOhms (schémas égaliseur audio)

Dans les paramètres des potentiomètres (composant *Res Tap* de la librairie *Miscellaneous Devices.IntLib,* étiquette *RvxA*), on retrouve le paramètre *Set Position* qui permet d'ajuster la valeur de Ra et Rb, sachant que Ra + Rb = 20 kOhms. Par exemple, avec *Set Position* = 0.5, le potentiomètre est divisé en parts égales par rapport au connecteur du centre, donnant ainsi Ra = 10 kOhms et Rb = 10 kOhms. **Attention : ne pas configurer le paramètre *Set Position* à 0 ou 1. Utilisez plutôt 0.001 et 0.999.**

4-) Circuit ayant 4 composants branchés au même nœud

Regardez les 2 schémas ci-dessous, plus particulièrement le nœud entre C1, C2, C3 et R2. Dans le schéma de droite, nous retrouvons bel et bien la structure de filtre MFB, comme désiré. Il en est tout autrement du schéma de gauche où le nœud n'est pas commun à C1, C2, C3 et R2. D'ailleurs, le schéma de gauche ne converge pas en simulation étant donné qu'il n'y a pas de chemin DC à la masse au nœud entre C1 et C2. Faites attention…
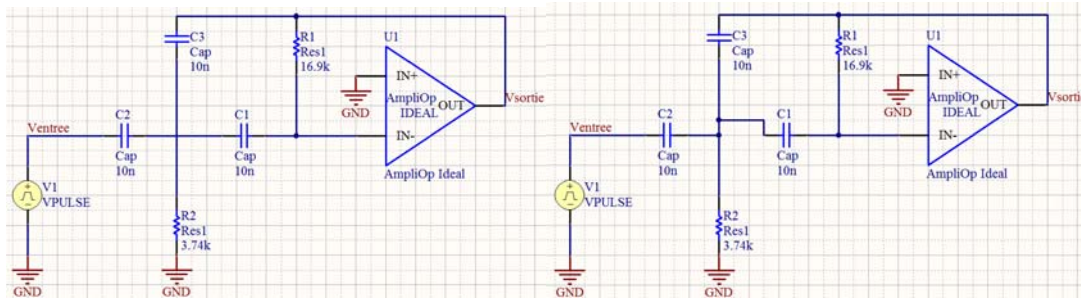
5-) Problèmes de convergence avec Altium

En cas de problème de convergence avec Altium, ce qui se produit fréquemment avec le LF444, expérimentez avec les paramètres de simulation disponibles dans « Advanced Options » de la fenêtre « Analyses Setup », notamment :

- Voir la section 4.2 du tutoriel sur Altium
- Augmentez Gmin par un facteur 10 ou plus (ex. de 10-15 à 10-14 ou plus). Cependant, le fait d'augmenter Gmin pourrait diminuer la précision.
- Augmentez ITL1 (ex. de 100 à 500 ou plus).
- Augmentez ITL2 (ex. de 50 à 200 ou plus).
- Augmentez ITL4 (ex. de 10 à 100 ou plus). Ceci pourrait aider à éliminer les erreurs «timestep too small ».
- Augmentez RELTOL (ex. de 0.001 à 0.005 ou plus). Cette valeur doit cependant demeurer inférieure à 1. Le fait d'augmenter RELTOL pourrait diminuer la précision.
- Changez la méthode d'intégration de « Trapézoïdale » à « Gear2 ».
- Lors de simulation temporelle, essayez sans l'option *Use Initial Conditions.*
- En dernier recours, remplacez les ampli-op par des ampli-op idéaux provenant de la librairie disponible sur la page web de l'APP6.
- Ci-dessous, un extrait du document *Simulation Models and Analyses Reference* provenant du Wiki Altium.

Notes

In general, you should not have to change any of the advanced SPICE parameters in this page of the dialog for accurate simulation. Only change these options if you have a good understanding of SPICE simulation parameters.

When troubleshooting Transient analysis failure, try setting:

- ABSTOL=RELTOL * (lowest current magnitude in the circuit)
- VNTOL= RELTOL * (lowest voltage magnitude in the circuit)

Raising the value of GMIN may help with convergence, but decreases accuracy.

ITL1 may need to be raised as high as 500 for many circuits.

ITL2 may need to be raised as high as 200 for some circuits.

ITL3 is not implemented in SPICE3. It is provided for compatibility in creating SPICE2 netlists.

Raising ITL4 to 100 or more may help to eliminate "timestep too small" errors improving both convergence and speed.

ITL5 is not implemented in SPICE3. It is provided for compatibility in creating SPICE2 netlists.

Enabling the KEEPOPINFO option is useful if the circuit is large and you do not want to run a redundant Operating Point Analysis.

In the numerical pivoting algorithm, the allowed min pivot is determined by:

EPSREL=AMAX1(PIVREL * MAXVAL, PIVTOL)

where MAXVAL is the max element in the column where a pivot is sought (partial pivoting).

With respect to the RELTOL option, larger values mean faster simulation time, but less accuracy.

Simulation Troubleshooting

When a circuit will not simulate you must identify if the problem is in the circuit, or the process of simulation. Follow the information contained in this section of the reference and work through the suggested points, trying one at a time.

Sometimes during a simulation a message will be displayed reporting errors or warnings. These messages are listed in the Messages panel.

Warning Messages

Warning messages are not fatal to the simulation. They generally provide information about changes that SPICE had to make to the circuit in order to complete the simulation. These include invalid or missing parameters, and so on.

Digital SimCode warnings may include information such as timing violations (tsetup, thold, trec, tw, etc.) or significant drops in power supply voltage on digital components.

Valid simulation results are normally generated even if warnings are reported.

Error Messages

Error messages provide information about problems that SPICE could not resolve and were fatal to the simulation. Error messages indicate that simulation results could not be generated, so they must be corrected before you will be able to analyze the circuit.

Troubleshooting netlist generation failure

When you run a simulation, the first thing that happens is the circuit is analyzed and a SPICE netlist is generated. This netlist is then passed to the SPICE engine, which simulates the circuit and generates the results.

Any errors that are detected during netlisting are listed in the Messages panel. Likely causes of netlisting errors include:

- A component in the schematic source document(s) not containing simulation information. To check if a component is suitable for simulation, double-click on the component in the schematic to open its Component Properties dialog and confirm that there is a linked simulation model, in the Models region of the dialog.

- The simulation model file that a component references is not in the location specified iin the Model Location region on the Model Kind tab of the Sim Model dialog. This could happen if the associated integrated library in which the model is stored is not installed, or it has been moved from its original install location.

  All source component libraries are installed to the following location:

  \Library

  This root folder includes various sub-folders containing component integrated libraries from specific manufacturers, as well as two general integrated library files (Miscellaneous Devices.IntLib and Miscellaneous Connectors.IntLib) providing general schematic components (many of which are simulation-ready).

  The \Library\Sim folder contains various .txt and .scb files, for SimCode-based simulation models, such as CMOS and 74XX series digital component models.

  The \Library\Simulation folder contains the following specific simulation-ready component integrated libraries:

  Simulation Math Function.IntLib

  Simulation Sources.IntLib

  Simulation Special Function.IntLib

  Simulation Transmission Line.IntLib

- The path to the Digital SimCode model (uncompiled source file (*.txt) or compiled file (*.scb)), referred to as {MODEL_PATH}, does not match the location of the model. This could happen if the model is moved to a different location on the hard drive. The model path is defined in the Simulation Preferences dialog and is relative to the Library folder of the installation. By default, the path is \Library\Sim\.

Trouble-shooting simulation analysis failures

One of the challenges of all Simulators is convergence. What exactly is meant by the term, "convergence"? Like most Simulators, the Altium Designer-based Simulator's SPICE engine uses an iterative process of repeatedly solving the equations that represent your circuit, to find the quiescent circuit voltages and currents. If it fails to find these voltages and current (fails to converge) then it will not be able to perform an analysis of the circuit.

SPICE uses simultaneous linear equations, expressed in matrix form, to determine the operating point (DC voltages and currents) of a circuit at each step of the simulation. The circuit is reduced to an array of conductances which are placed in the matrix to form the equations (G * V = I). When a circuit includes nonlinear elements, SPICE uses multiple iterations of the linear equations to account for the non-linearities. SPICE makes an initial guess at the node voltages then calculates the branch currents based on the conductances in the circuit. SPICE then uses the branch currents to recalculate the node voltages, and the cycle is repeated. This cycle continues until all of the node voltages and branch currents fall within specified tolerances (converge).

However, if the voltages or currents do not converge within a specified number of iterations, SPICE produces error messages (such as "singular matrix", "Gmin stepping failed", "source stepping failed" or "iteration limit reached") and aborts the simulation. SPICE uses the results of each simulation step as the initial guesses for the next step. If you are performing a Transient analysis (that is, time is being stepped) and SPICE cannot converge on a solution using the specified timestep, the timestep is automatically reduced, and the cycle is repeated. If the timestep is reduced too far, SPICE displays a "Timestep too small" message and aborts the simulation.

General simulation convergence troubleshooting

When a simulation analysis fails, the most common problem is failure of the circuit to converge to a sensible operating point. Use the following techniques to solve convergence problems.

Convergence trouble-shooting steps

- When you have a convergence problem, first turn off all the analyses except the Operating Point analysis.
- Consult the Messages panel for any errors/warnings relating to simulation.
- Make sure the circuit is wired correctly. Dangling nodes and stray parts are not allowed.
- Ensure that the circuit has a ground node, and that every node in the circuit has a DC path to this ground. Components that can isolate a node include transformers and capacitors. Voltage sources are considered a DC short circuit, current sources are considered a DC open circuit.
- Ensure that zeros have not been confused with the letter O when entering simulation parameters.
- Ensure that proper SPICE multipliers have been specified (MEG instead of M for 1E+6) for any component values or simulation parameters. Multipliers are not case sensitive. Also, spaces between values and multipliers are not allowed. For example it should be 1.0uF, not 1.0 uF.
- Make sure all devices and sources are set to their proper values.
- Make sure the gain of any dependent source is correctly set.
- Temporarily eliminate series capacitors or current sources and re-run the simulation.
- Temporarily eliminate parallel inductors or voltage sources and re-run the simulation.
- On the SPICE Options page of the Analyses Setup dialog (from the schematic select Design » Simulate » Mixed Sim, then click the Advanced Options entry in the Analyses/Options list), increase the value of the ITL1 parameter to 300. This will allow the Operating Point analysis to go through more iterations before giving up.
- Add .NS (Nodeset) devices to define the node voltages. If the initial guess of a node voltage is way off, the .NS device can be used to predefine a starting voltage that is used for a preliminary pass of the operating point analysis.
- If the Nodeset device does not assist in convergence, try defining the initial conditions by placing .IC devices. In this case the node voltages are held at the specified values during the Operating Point analysis, then released during the Transient analysis.
- Enable the Use Initial Conditions option on the Transient/Fourier Analysis Setup page of the Analyses Setup dialog (from the schematic, select Design » Simulate » Mixed Sim, then click the Transient/Fourier Analysis entry in the Analyses/Options list). This option works in conjunction with the .IC devices (or the IC parameter of the components). By setting this option, the Operating Point analysis is not performed and the specified voltages are used as the initial conditions for the Transient analysis.
- Specify the series resistance parameters of your models and increase the GMIN option (SPICE Options page of the Analyses Setup dialog) by a factor of 10. Specify the initial condition of semiconductor devices, especially diodes, as OFF.

DC Sweep Analysis troubleshooting

When you have a problem with a DC Sweep analysis, first try the steps listed in the General simulation convergence troubleshooting section.
If you still encounter problems, try the following:

- Change the value of the Primary Step parameter on the DC Sweep Analysis page of the Analyses Setup dialog. If discontinuities exist in a device model (perhaps between the linear and saturation regions of the model), increasing the step size may allow the simulation to step over the discontinuity. Making the steps smaller, on the other hand, will allow the simulation to resolve rapid voltage-transition discontinuities.
- Disable the DC Sweep analysis. Some problems (such as hysteresis) cannot be resolved by DC analysis. In such cases, it is more effective to use the Transient analysis and ramp the values of the appropriate power sources.

Transient Analysis troubleshooting

When you have a problem with a Transient analysis, first try the steps listed in the General simulation convergence troubleshooting section.
If you still encounter problems, try the following.
On the SPICE Options page of the Analyses Setup dialog (from the schematic select **Design » Simulate » Mixed Sim**, then click the Advanced Options entry in the Analyses/Options list):

- Set the RELTOL parameter to 0.01. By increasing the tolerance from its default of 0.001 (0.1% accuracy), fewer iterations will be required to converge on a solution and the simulation will complete much more quickly.
- Increase the value of the ITL4 parameter to 100. This will allow the Transient analysis to go through more iterations for each timestep before giving up. Raising this value may help to eliminate "timestep too small" errors improving both convergence and simulation speed.

- Reduce the accuracy by increasing the values of ABSTOL and VNTOL, if current/voltage levels allow. Your particular circuit may not require resolutions down to 1uV or 1pA. You should, however, allow at least an order of magnitude below the lowest expected voltage or current levels of your circuit.
- change the Integration Method to one of the Gear methods. Gear integration requires a longer simulation time, but is generally more stable than trapezoidal. Gear integration may be particularly useful with circuits that oscillate or have feedback paths.

Additional things to try:

- Realistically model your circuit. Add realistic parasitics, especially stray/junction capacitance. Use RC snubbers around diodes. Replace device models with subcircuits, especially for RF and power devices.
- Increase the rise/fall times of any Periodic Pulse sources in your circuit. Even the best pulse generators cannot switch instantaneously.