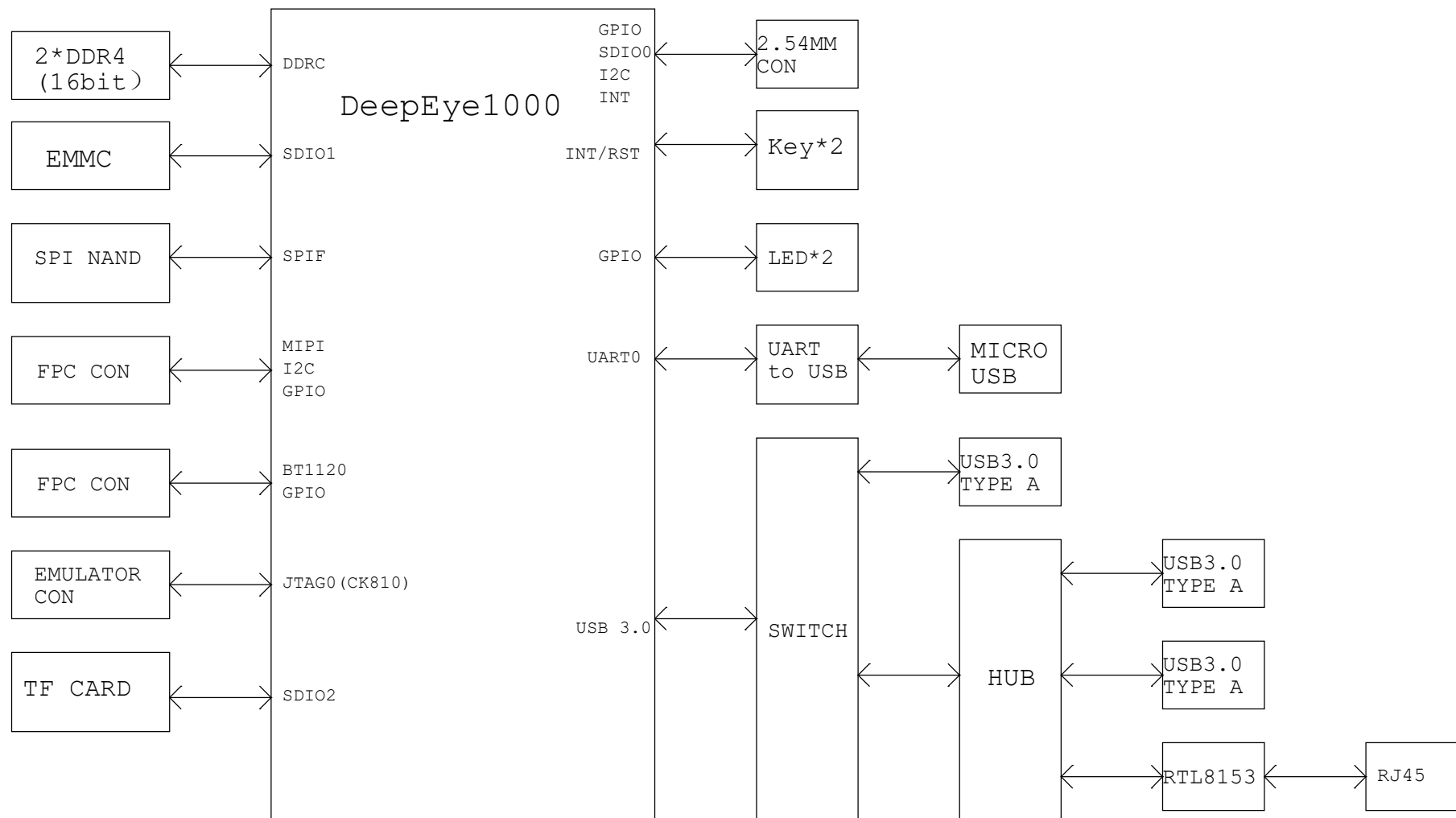


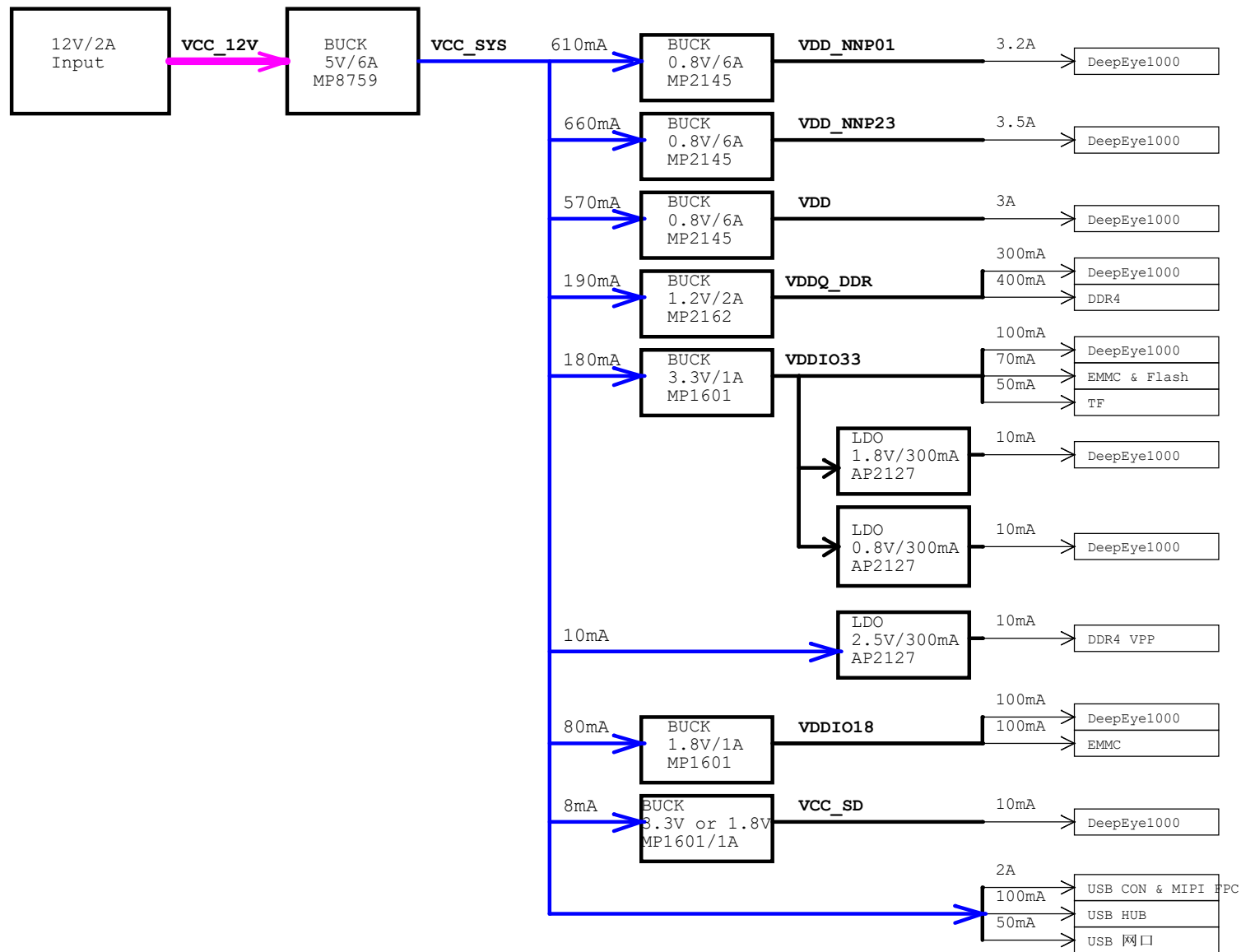
5	4	3	2	1
D				D
C				C
B				B
A				A
5	4	3	2	1

Page	Description
1	Cover Page
2	Block Diagram
3	Power Tree
4	Power1
5	Power2
6	Power of DeepEye1000
7	GND of DeepEye1000
8	DDR4
9	EMMC
10	OSC & RST & CONF
11	TF & Flash
12	Uart &GPIO
13	BT1120 & SDIO0
14	MIPI
15	Uart to USB
16	USB Switch
17	USB HUB
18	USB Port
19	USB to ETH

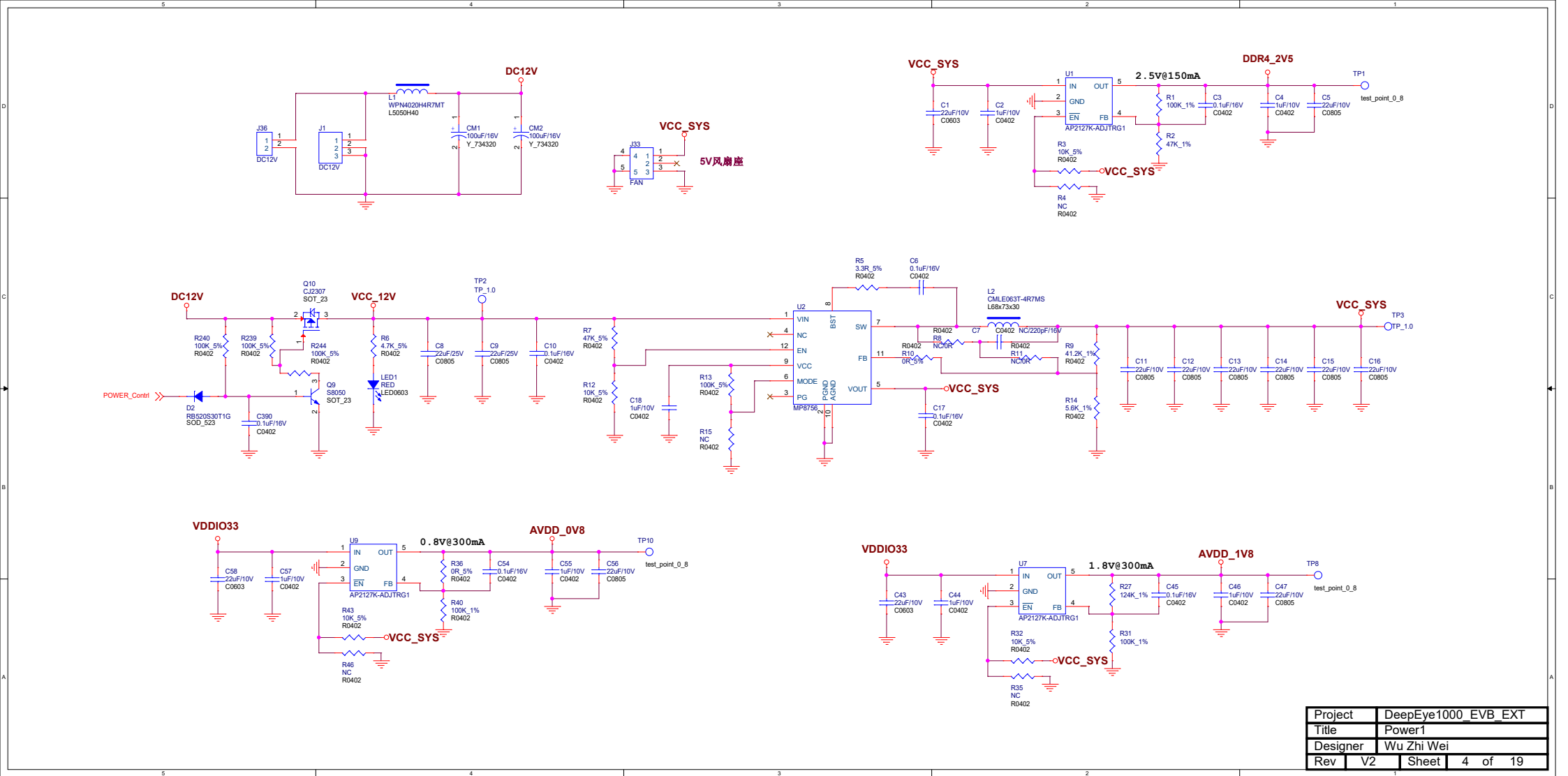
Project		DeepEye1000_EVB_EXT	
Title		Cover Page	
Designer		Wu Zhi Wei	
Rev	V2	Sheet	1 of 19

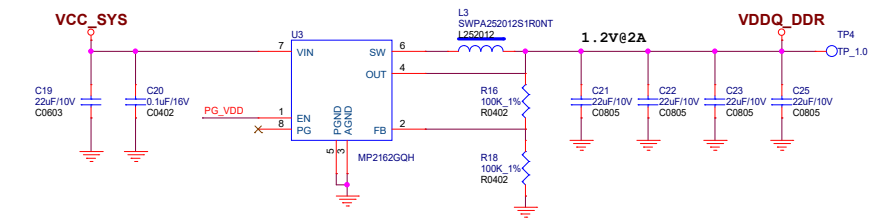
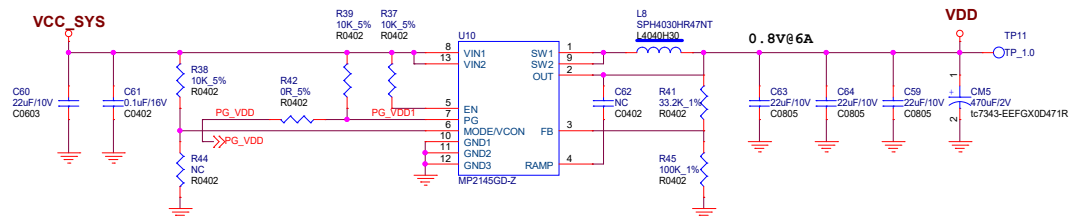
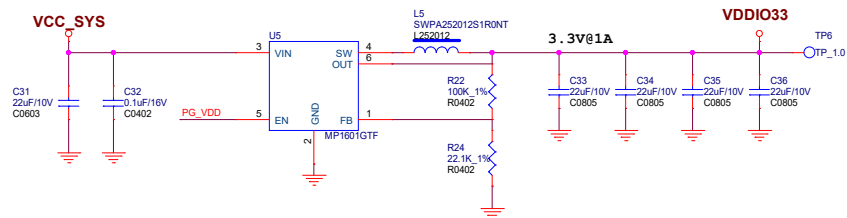
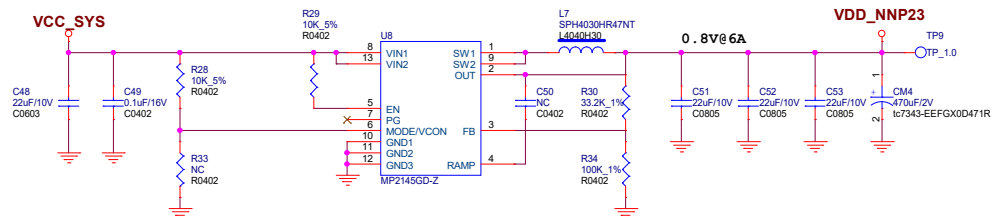
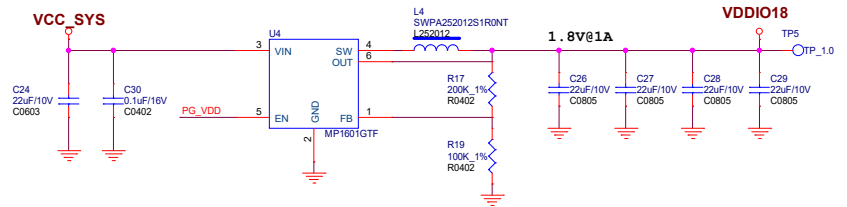
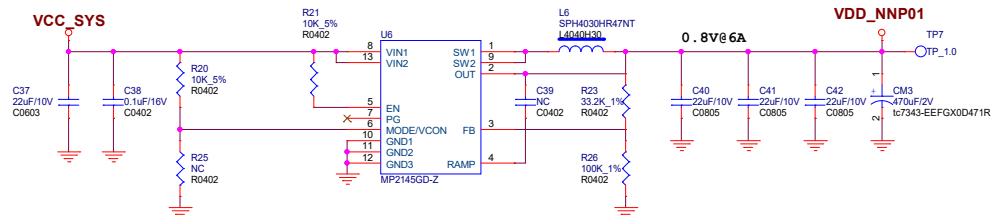


Project	DeepEye1000_EVB_EXT		
Title	Block Diagram		
Designer	Wu Zhi Wei		
Rev	V2	Sheet	2 of 19



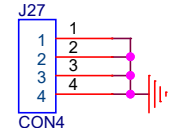
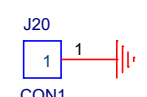
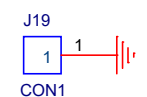
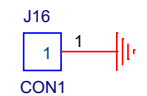
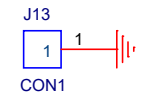
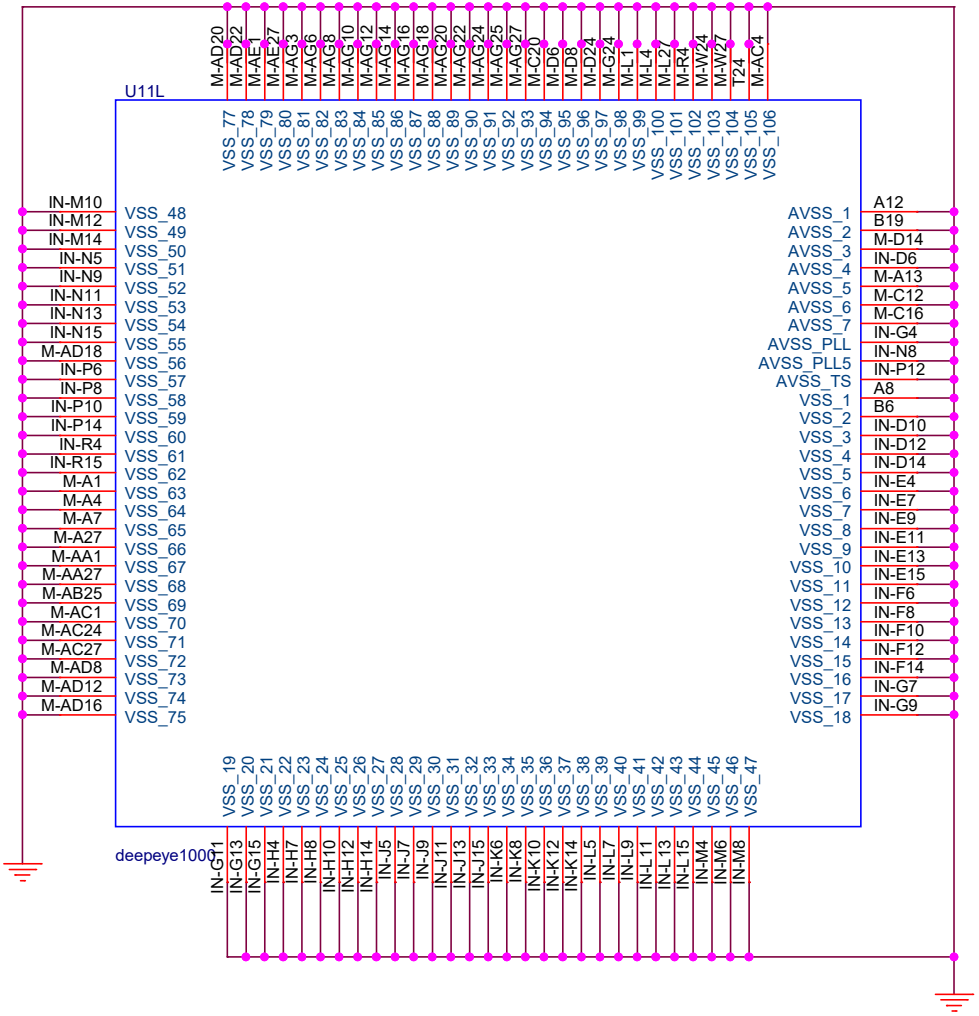
Project	DeepEye1000_EVB_EXT		
Title	Power Tree		
Designer	Wu Zhi Wei		
Rev	V2	Sheet	3 of 19



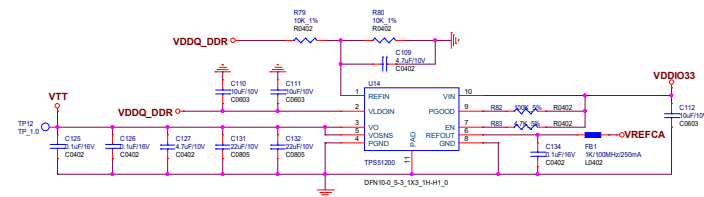
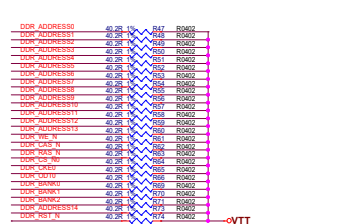


Project	DeepEye1000_EVB_EXT
Title	Power2
Designer	Wu Zhi Wei
Rev	V2
Sheet	5 of 19

Project		DeepEye1000_EVB_EXT	
Title		DP1000_POWER	
Designer		Wu Zhi Wei	
Rev	V2	Sheet	6 of 19



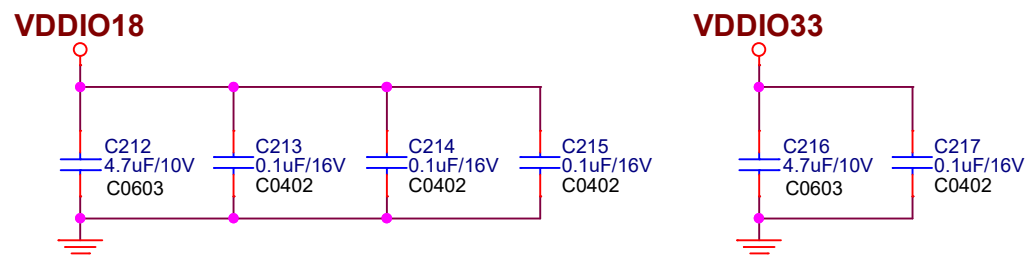
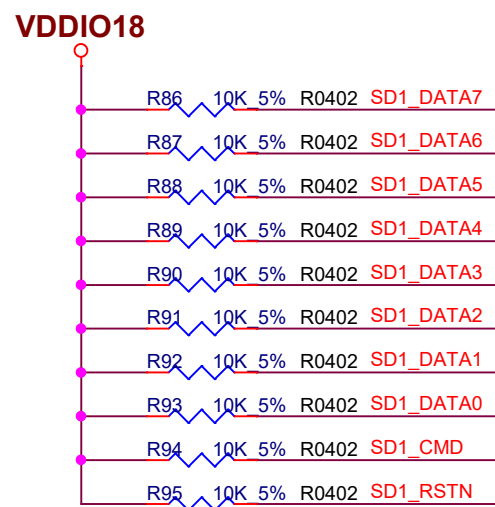
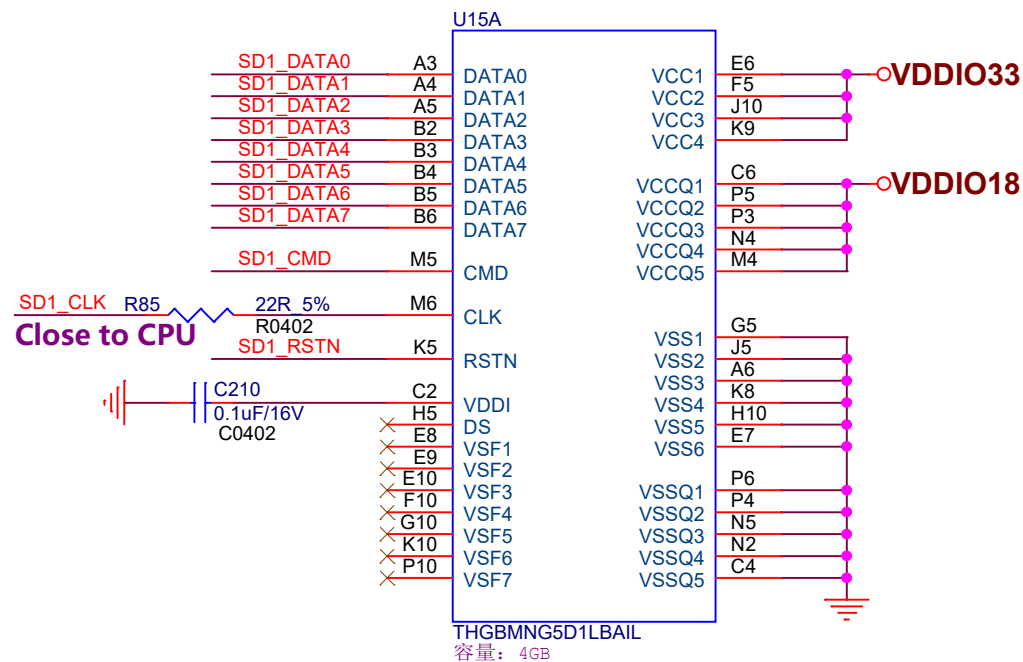
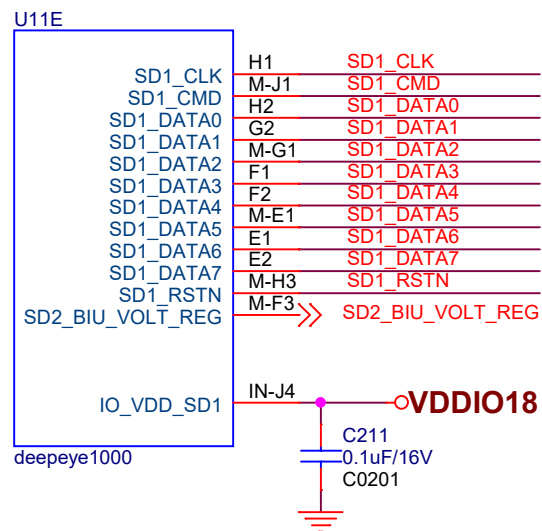
Project	DeepEye1000_EVB_EXT		
Title	DP1000_GND		
Designer	Wu Zhi Wei		
Rev	V2	Sheet	7 of 19



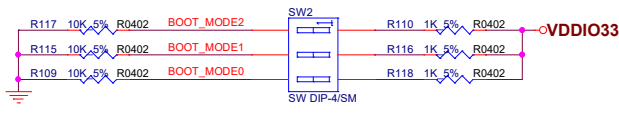
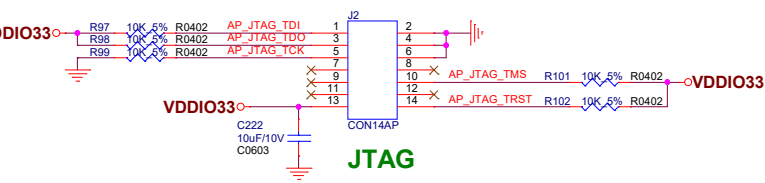
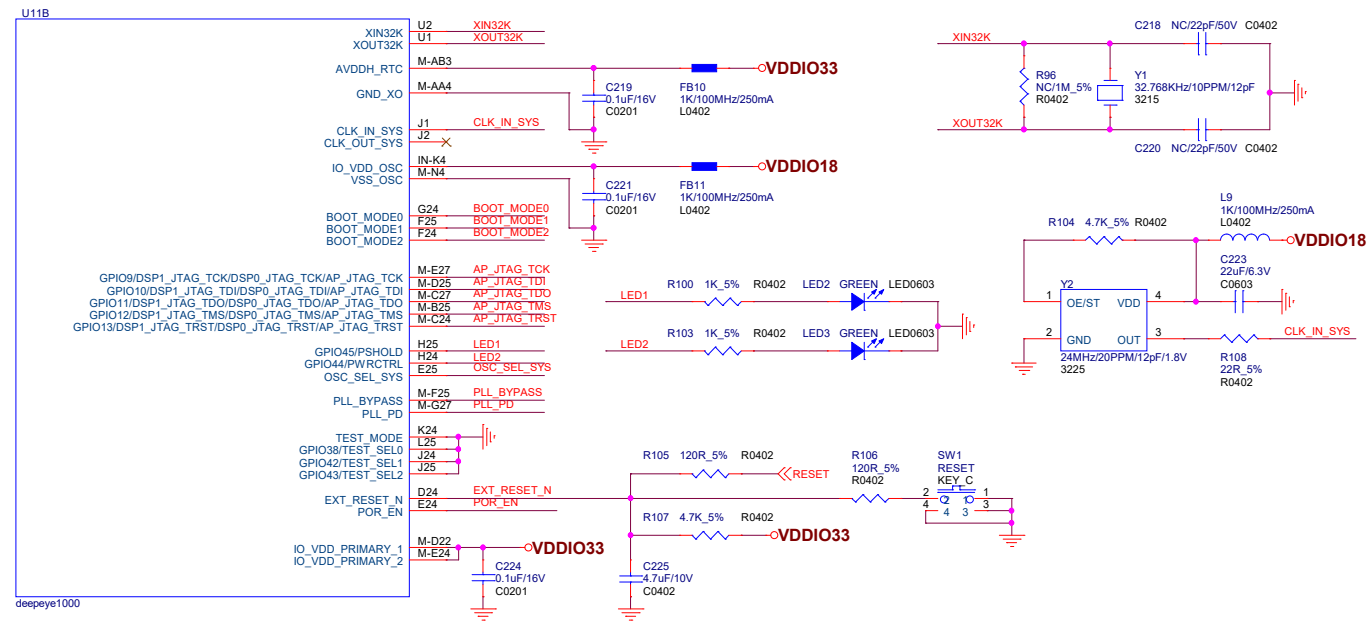
颗粒端放置，靠近焊盘和过孔

Project	DeepEye1000_EVB_EXT		
Title	DDR4		
Designer	Wu Zhi Wei		
Rev	V2	Sheet	8 of 19



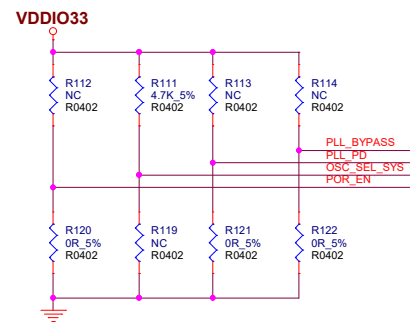


Project	DeepEye1000_EVB_EXT		
Title	EMMC		
Designer	Wu Zhi Wei		
Rev	V2	Sheet	9 of 19



boot mode	boot mode2	boot mode1	boot mode0
uart	0	0	0
usb	0	0	1
spi slave	0	1	0
sd card	0	1	1
emmc	1	0	0
spi nor	1	0	1
spi nand	1	1	0
default	1	1	1

拨码开发 (boot方式选择)



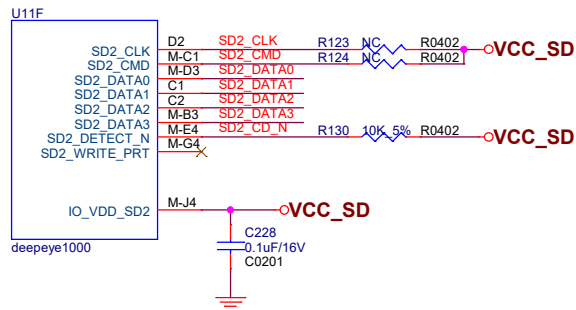
mode	POR_EN
POR ENABLE	1
POR DISABLE	0

	OSC_SEL_SYS
OSC BYPASS,CLK FROM OUTSIDE	1
OSCILLATEOR ENABLE	0

mode	PLL_PD	PLL_BYPASS
PLL ACTIVE	0	0
PLL BYPASS	0	1
PLL POWER DOWN	1	0
PLL POWER DOWN	1	1

CONFIG

Project		DeepEye1000_EVB_EXT		
Title		OSC & RST & CONF		
Designer		Wu Zhi Wei		
Rev	V2	Sheet	10	of 19

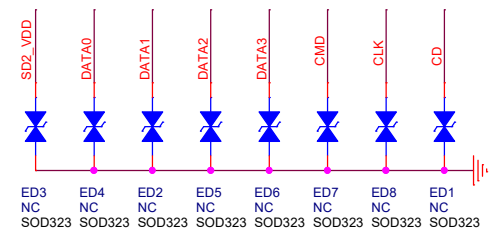
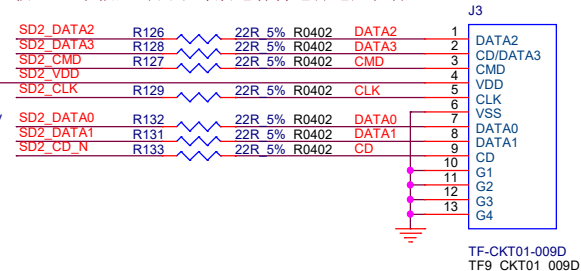


VDDIO33

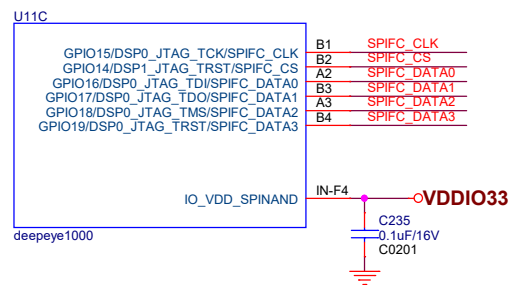
2.7R电阻作用:

防止TF卡插入时由于等效电容将电源电压拉低

Close to TF

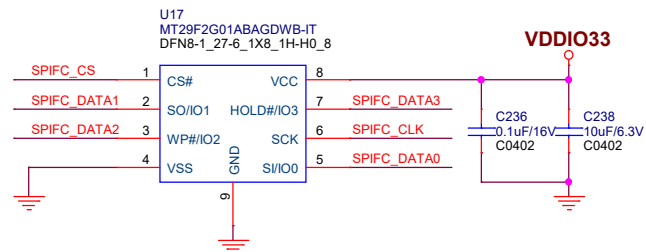


## TF Card

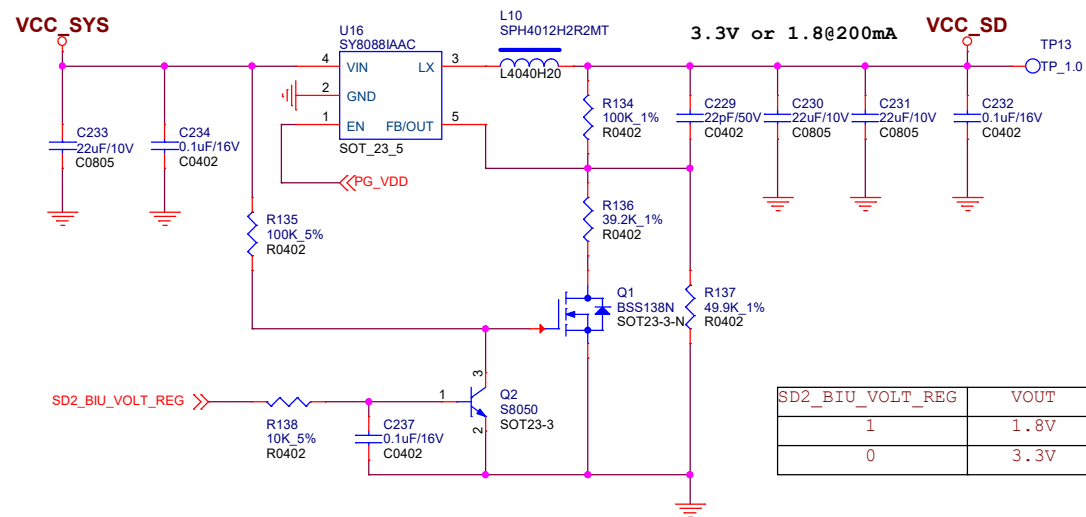


VDDIO33

## SPI FLASH



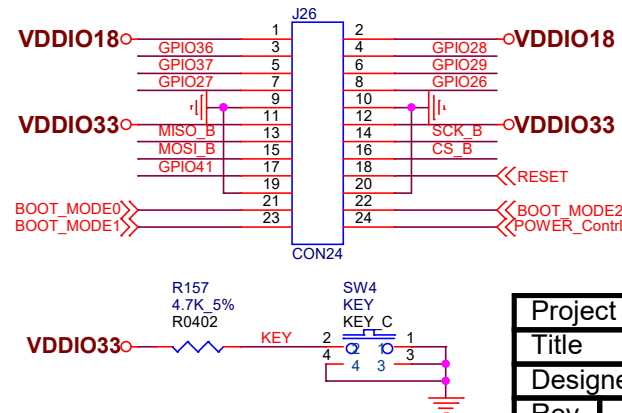
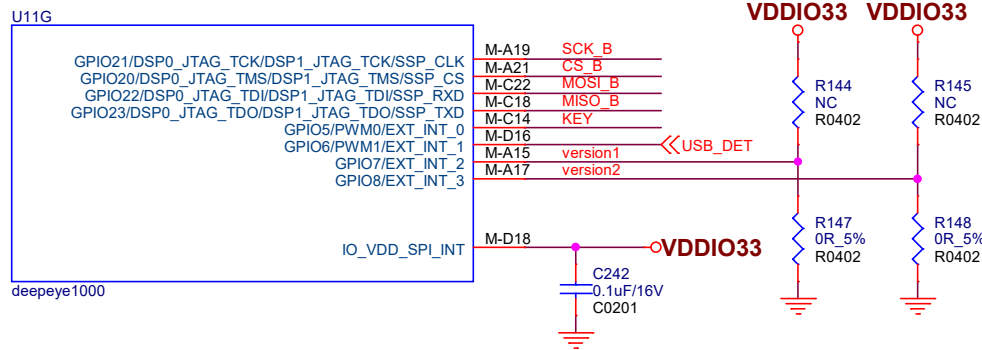
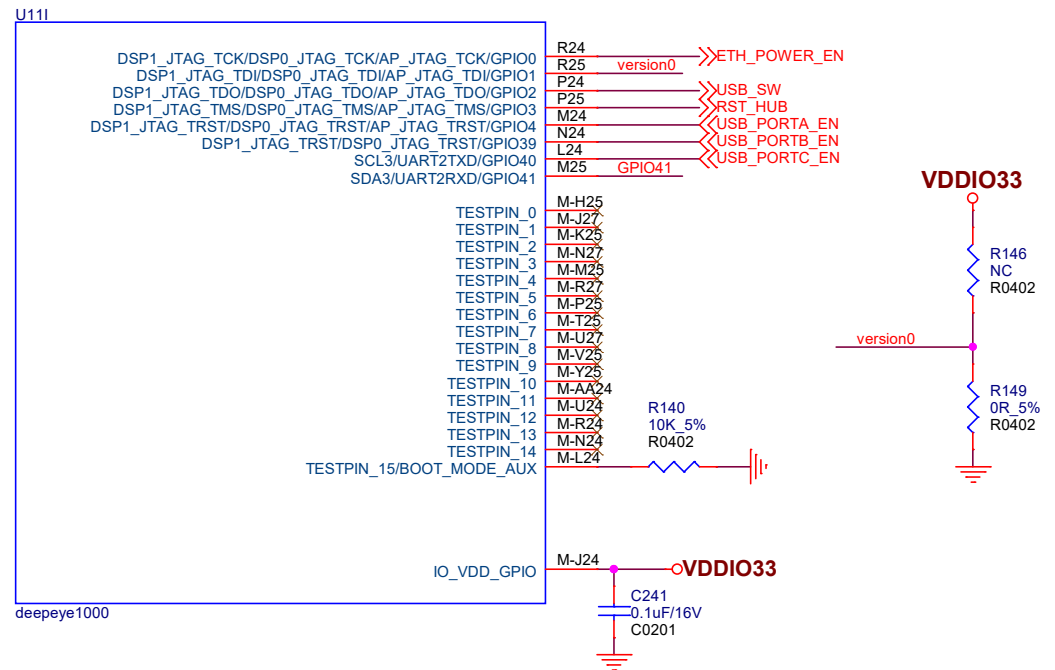
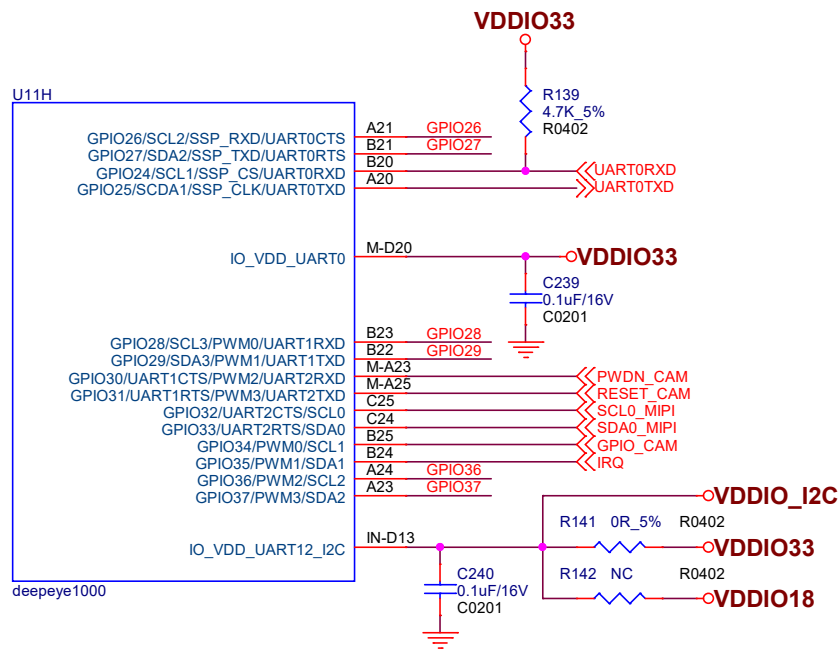
VCC\_SYS



SD2_BIU_VOLT_REG	VOUT
1	1.8V
0	3.3V

## SD2 POWER

Project	DeepEye1000_EVB_EXT
Title	TF & FLASH
Designer	Wu Zhi Wei
Rev	V2
Sheet	11 of 19



Project	DeepEye1000_EVB_EXT		
Title	UART & GPIO		
Designer	Wu Zhi Wei		
Rev	V2	Sheet	12 of 19

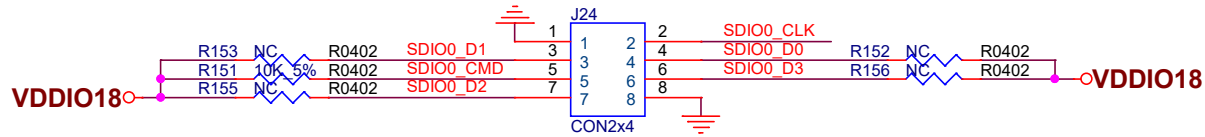
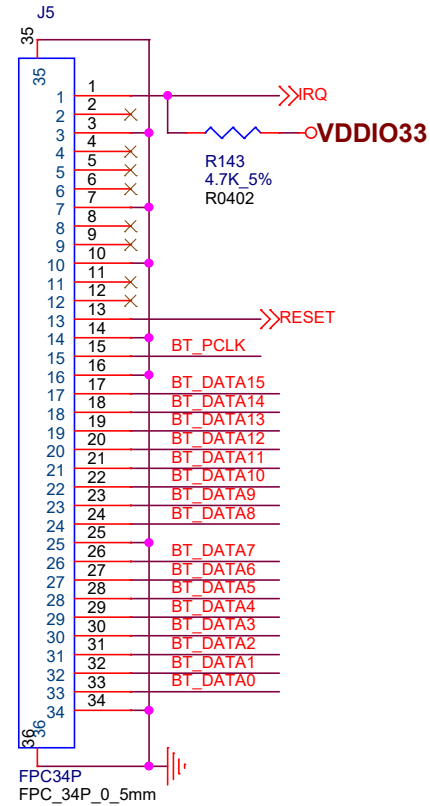
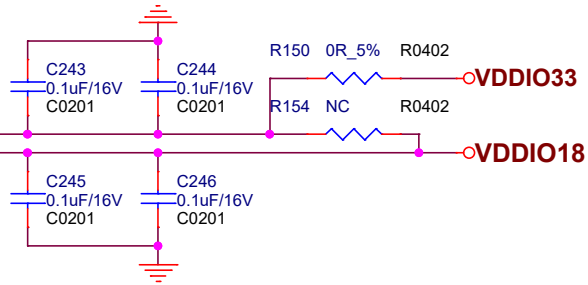
U11D

VCLK  
VDATA0  
VDATA1  
VDATA2  
VDATA3  
VDATA4  
VDATA5  
VDATA6  
VDATA7  
VDATA8  
VDATA9  
VDATA10  
VDATA11  
VDATA12  
VDATA13  
VDATA14  
VDATA15  
SD0\_CLK  
SD0\_CMD  
SD0\_DATA0  
SD0\_DATA1  
SD0\_DATA2  
SD0\_DATA3

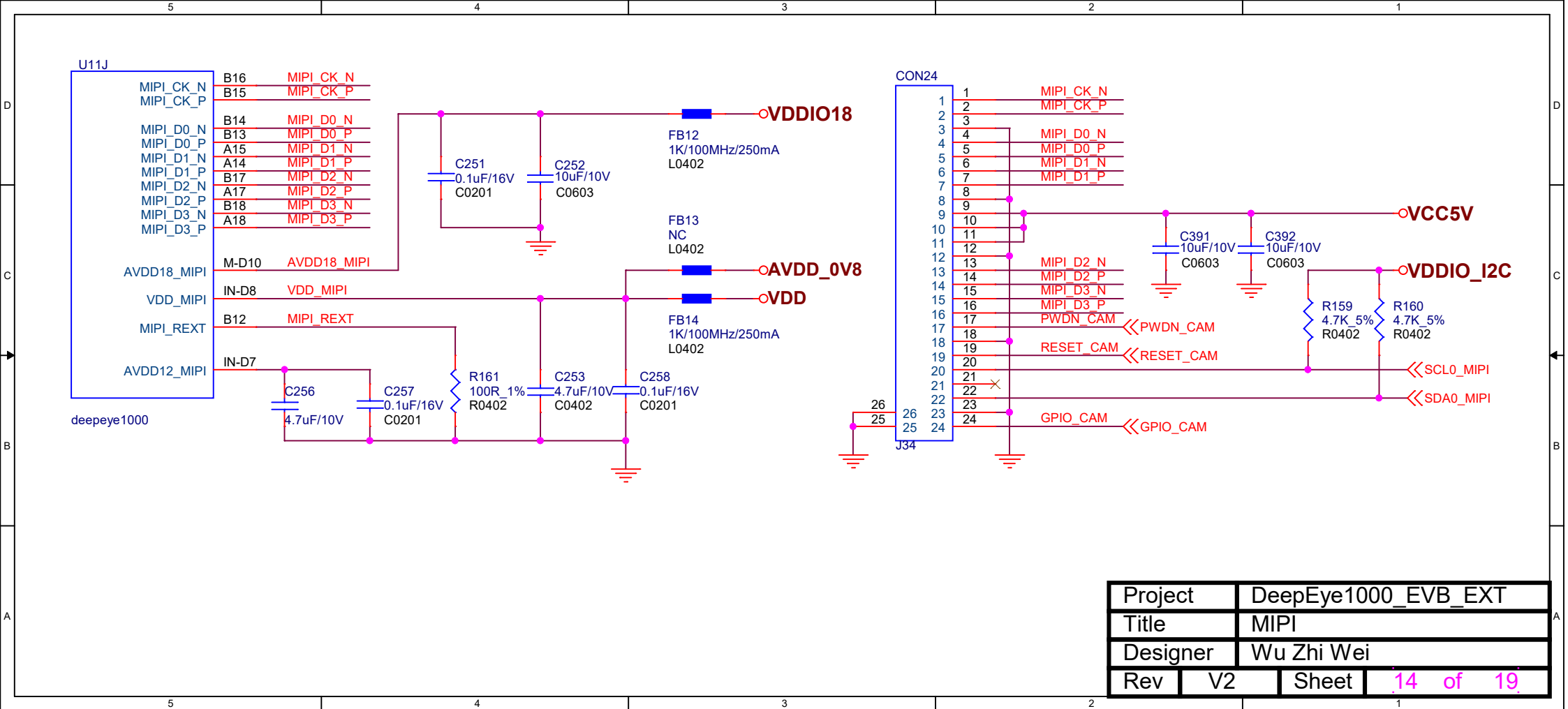
R1 BT\_PCLK  
R2 BT\_DATA0  
P1 BT\_DATA1  
P2 BT\_DATA2  
M-T3 BT\_DATA3  
M-U4 BT\_DATA4  
M-R1 BT\_DATA5  
N2 BT\_DATA6  
M-N1 BT\_DATA7  
M-P3 BT\_DATA8  
M1 BT\_DATA9  
M2 BT\_DATA10  
L1 BT\_DATA11  
L2 BT\_DATA12  
K2 BT\_DATA13  
M-M3 BT\_DATA14  
M-K3 BT\_DATA15  
M-Y3 SDIO0\_CLK  
M-W1 SDIO0\_CMD  
M-W4 SDIO0\_D0  
T2 SDIO0\_D1  
M-U1 SDIO0\_D2  
M-V3 SDIO0\_D3

IO\_VDD\_BT1120  
IO\_VDD\_SD0\_18

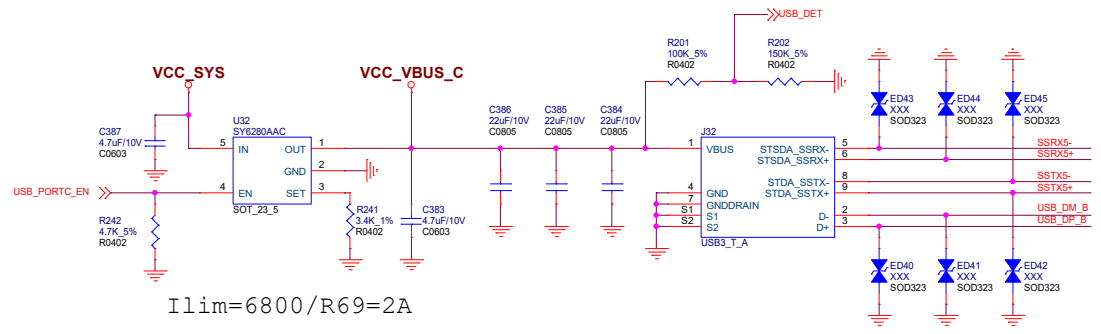
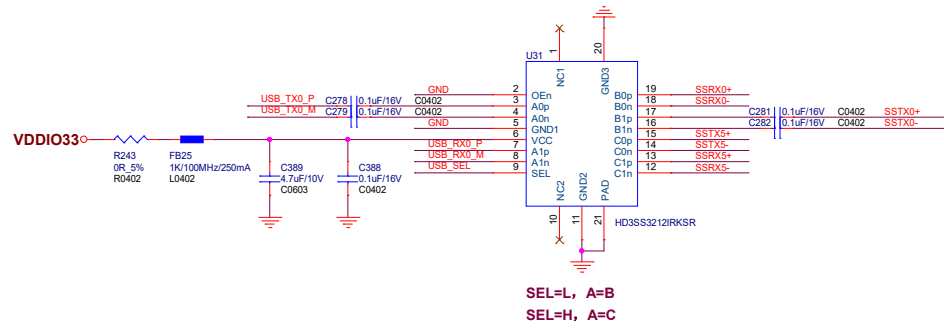
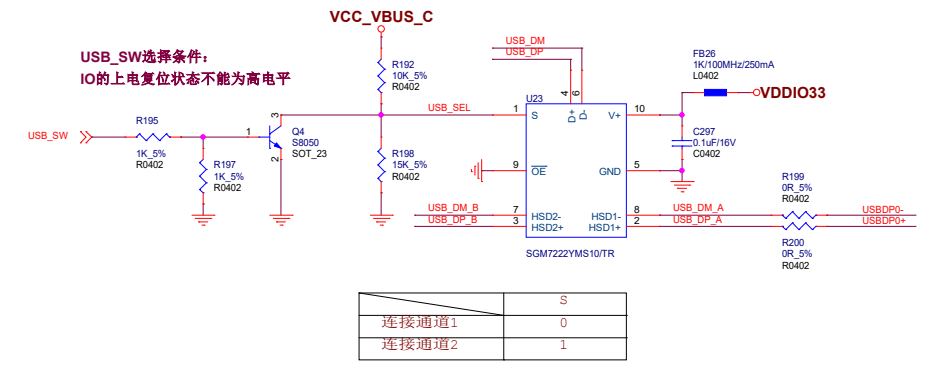
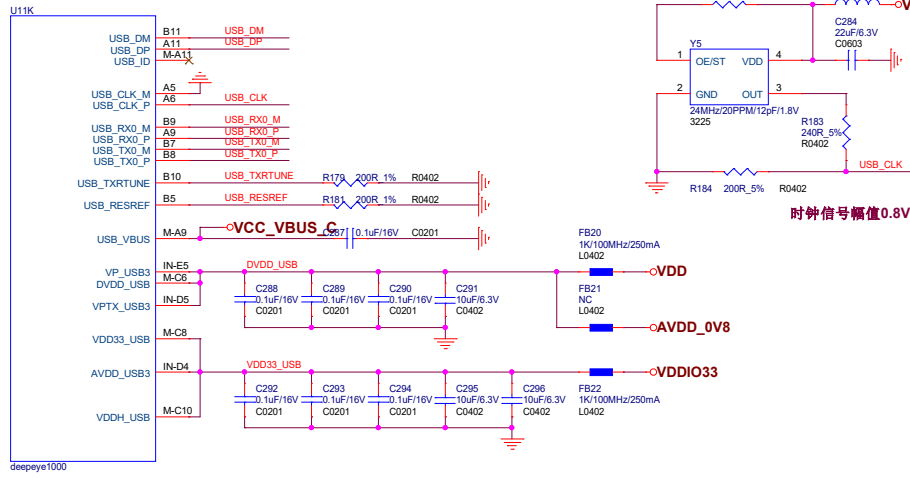
deepeye1000



Project	DeepEye1000_EVB_EXT
Title	BT1120 & SDIO0
Designer	Wu Zhi Wei
Rev	V2
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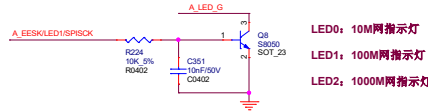


Project	DeepEye1000_EVB_EXT
Title	USB Switch
Designer	Wu Zhi Wei
Rev	V2
Sheet	16 of 19









**Bob Smith**

