NFC sensor tag development using industrial flexible integrated circuit process

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***Abstract*—The electronics industry has changed significantly in the past few years, and the growth of wearable electronic devices and sensors, in addition to the Internet of Things upward trend. Flexible electronic circuits are very suitable for making wearable devices with sensors for measurement as needed. According to its flexibility, lightweight, low cost to manufacture and produce quickly, are the characteristics of amorphous indium gallium zinc oxide (a-IGZO). In this project, we study and design an NFC sensor tag using industrial flexible integrated circuit process. Begin with design, analysis and layout using Candence Virtuoso program, which will be used as an example for making other devices with this technology.**

Keywords— Internet of Things, NFC sensor tag, flexible integrated circuit, amorphous Indium Gallium Zinc Oxide (a-IGZO)

I. Introduction

The field of electronics has witnessed a transformation phase in recent years, due to the rapid growth of wearables and widespread sensors, and the advent of the Internet of Things (IoT), flexible electronics have become increasingly accepted. It can also be applied to sensors due to its low cost and light weight. Ultra-thin shapes and large spaces, consistency, and mechanical flexibility, which are the inherent elastic characteristics of substrates in these technologies can be used for applications that require bending ability and flexibility an example of a common application that can benefit greatly from flexible electronics is the domain of flexible and adaptive wearables, e.g., for health and healthcare monitoring.

Amorphous Indium Gallium Zinc Oxide (a-IGZO) is considered one of the best choices for flexible electronics due to its high mobility, large area uniformity, compatibility with low-temperature processing, and good stability provided. The formatter will need to create these components, incorporating the applicable criteria that follow.

II. Implementation of A-IGZO TFT

A. A-IGZO TFT vs Tranditional CMOS Transistor

In the flexible integrated circuit manufacturing process, the heat is used at 150-350 °C, whereas in the silicon process, heat is used around 850-1100 °C. Transistors manufactured at room temperature have a relatively high threshold voltage, and their charge carrier mobility (μ) is about 15-20 cm^2/V.s, which is much lower than that of silicon. This affects the design, including the threshold voltage in the range of 0-2 V, causing the system to require a high voltage of 5-30 V [1].

B. Design Technique of Unipolar Device

Designing an a-IGZO TFT is extremely difficult because it can currently only be made as n-type. As a result, different loads must be used in design approaches and strategies in place of the p-type. Figure 1 is an example of an inverter [2]. When using different loads in place of p-type transistors, it suffers from the static power created by diode coupled transistor biasing, leading to low power efficiency. This is due to the circuit's high power consumption; hence, in order to optimize the system, the designer also had to consider power dissipation.

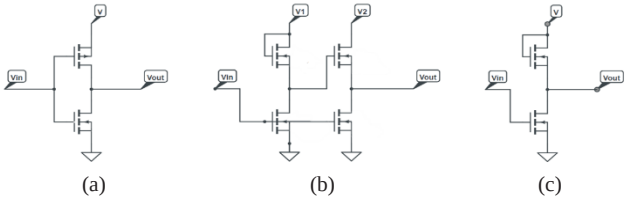


FIGURE 1. The active load place of p-type transistors (a) traditional CMOS inverter (b) pseudo-CMOS diode-connected inverter (c) diode-connected inverter.

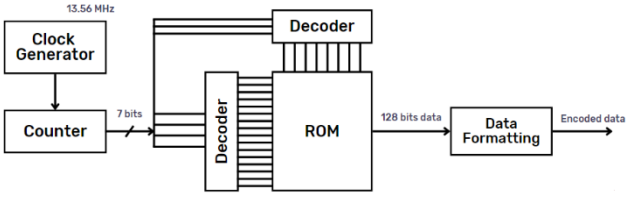


FIGURE 2. A block diagram of digital core generator

C. NFC Tag components

- Digital Core Generator

  A digital integrated circuit consists of parts [3], as shown in Figure 2, to generate signals and send them out according to ISO 14443 standards. The Clock Generator receives frequency from the NFC reader and transmits clocks for other sectors. The 7-bit counter then uses the resulting frequency to count and send a 7-bit count to each decoder, and sends the code to read-only memory (ROM), where the memory transfers the data bit by bit as batch code using a decoder that addresses each bit in ROM, after which the data is output from the ROM. It is formatted by data formatting blocks using Manchester coding principles. This is due to benefits such as clock self-tuning, DC balancing, and improved error detection.

- Temperature Sensor

  The temperature sensor circuit uses a semiconductor made up of transistors, capacitors and resistors. Due to temperature sensor using threshold voltage dependence of transistor which rely on material instead of circuit design [4]. Therefore, we create a proposed circuit that works in the form of PTAT [5]

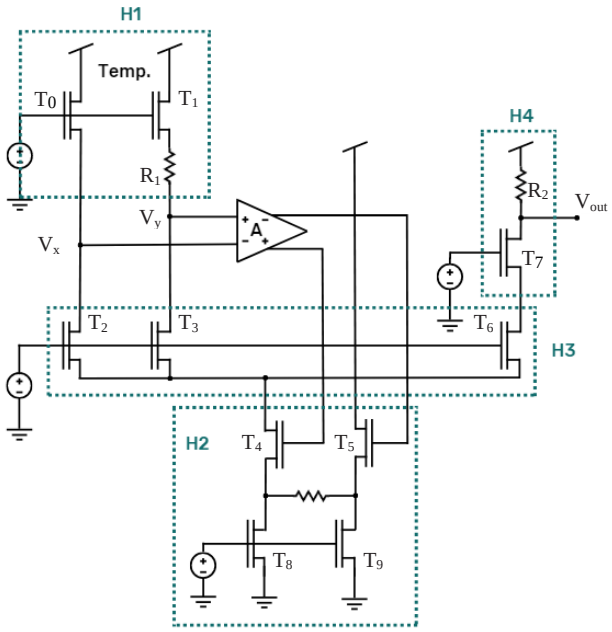


FIGURE 3. The proposed temperature sensor circuit using only n-type thin film transistors.

(Proportional to Absolute Temperature). The working principle of the system is shown in Figure 3.

Firstly, the subthreshold operational region is employed to bring sensitivity out of H_1, using current of proportional to absolute temperature (PTAT) in order to force voltage node of x and y to be equal by using negative feedback. The differential voltage between those two nodes is then transmitted to a differential output op-amp (operational amplifier). the op-amp are then biased to H_2, where the differential voltage is converted into a single-ended current. Using The feedback current splitting of H_3 is utilized to maintain system stability in the face of temperature variations, with the current from H_2 controlling this feedback loop. Finally, H_4 uses one branch of this current to generate an output voltage that is proportional to absolute temperature. The temperature-dependent voltage equation can be written as:

$$\Delta V_{out} = \frac{k}{q}\frac{R_2}{R_1}\ln(n)\cdot\Delta T \tag{1}$$

where, k is Boltzmann's constant (1.380×10^{-23} J/K), q is electronic charge (1.602×10^{-19} coulomb), and n is width ratio between T_0 and T_1.

- Operational Amplifier (Op-Amp)

Due to the unipolarity problem of a-IGZO [2], the design has to consider the critical part required by the temperature sensor circuit including a high gain. Therefore, the principle of positive feedback [6] is proposed to increase the gain of the op-amp and this op-amp has the equation of gain as follows.

$$\frac{V_{out+}}{V_{in+}-V_{in-}} = \frac{g_{m6}}{g_{s5}+g_{m7}A} = \frac{g_{m6}}{g_{s5}-g_{m7}\frac{g_{m0}}{g_{s1}}} \tag{2}$$

It can be divided into two parts: the first part, in Fig. 4(a), has a low gain close to 1 V/V, and the second part, in Fig. 4(b), is based on the principle of shunt

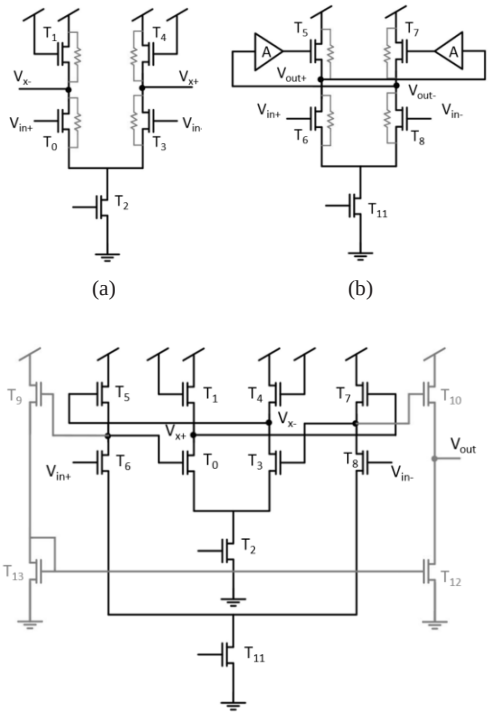


FIGURE 4. Components of positive feedback Op-amp (a) First stage gain (b) Second stage using the first stage as positive feedback (c) Add the third stage, which is the buffer stage.

feedback. plus Therefore, when the gain of the first part is very close to 1 V/V, it will result in a very high total gain as in Equation 2, but the circuit still has a problem of low output oscillation. As a result, the op amp is easily saturated. Therefore, it is necessary to add another part that is a voltage driver circuit (Buffer) as shown in Figure 4(c).

III. BLOCK DIAGRAM

By calculating the transfer function of the sections within the temperature sensor circuit in Section II part C, the parameters can be designed by looking at the diagram of the system. The designed system has an open loop gain in the negative feedback loop that helps itself in terms of system stability and linearity, which is represented by L(s) and has Pole and Zero as follows:

$$L(s) = L_{s=0}\cdot\frac{(1-\frac{s}{z_0})}{(1+\frac{s}{p_0})\cdot(1+\frac{s}{p_1})} \tag{3}$$

Where $L_{s=0}$, z_0, p_0, and p_1 can be written as:

$$L_{s=0} = \frac{A}{3}\cdot\left(\frac{g_{m4}/2}{1+g_{s4}R_3}\right)\cdot\left(\frac{1}{g_{s0}}-\left(R_1+\frac{1}{g_{s1}}\right)\right) \tag{4}$$

$$z_0 = \frac{2}{C_{gs4}R_3\left(\frac{g_{s4}}{g_{m4}}-1\right)} \tag{5}$$

$$p_0 = \frac{2}{C_{gs4}R_3} \tag{6}$$

$$p_1 = \frac{g_{s0}+g_{s2}}{C_{gs2}} \tag{7}$$

Where g_m and g_s are transconductance of each transistor, C_{gs} is parasitic capacitance between gate and source pin of each.

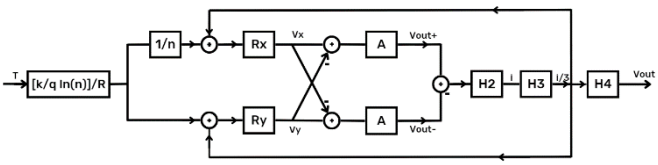
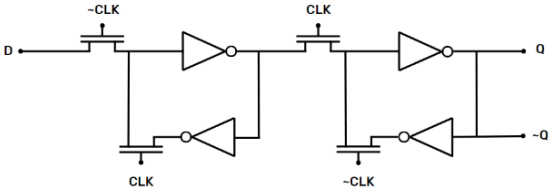


FIGURE 5. The block diagram of temperature sensor system



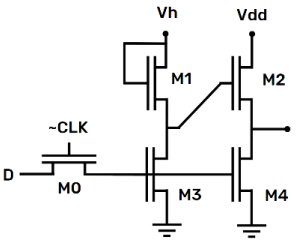


FIGURE 6. Schematic of D flip-flop and circuit inside every inverter.

From equation 3, it can be seen that when considering the frequency response, the open loop gain is affected by Zero RHP (Right half plane), which keeps the phase margin low resulting in the stability of the system is worse. As for Figure 5, the diagram of the system shows the open loop gain that has been calculated as an equation. To force the voltages at the nodes V_x and V_y to be equal according to the system conditions while a transistor operating in the subthreshold region, it also generates temperature-dependent current entering the system in order to amplify signal to the voltage at V_{out}.

IV. DESIGN RESULT

A. *Digital Core Generator*

From the analysis of the power consumption of each part of the digital circuit in Figure 7, it can be observed that most of the power is lost to the 7-bit counter, which consists of the clock generator. It consists of 7 D-flip flops connected together, designed to generate the lowest power consumption clock circuit. This can be done by adjusting the channel amplitude of each transistor inside the D-flip-flop as shown in Figure 6 and obtaining the Table 1 (length = 0.8 um).

TABLE 1. WIDTH DESIGN IN INVERTER FOLLOWING SPEED USED

	W_{m1} (um)	W_{m3} (um)	$W_{m2,m4}$ (um)	W_{m0} (um)	Power (mW)	Speed
D1	4.8	8.8	40.8	40.8	1.50	13.56 MHz
D2	0.8	4.8	40.8	40.8	0.645	6.780 MHz
D3	0.8	4.8	10.8	40.8	0.398	1.690 MHz
D4	0.8	1.8	10.8	100.8	0.302	423.7 kHz
D5	0.8	1.8	3.80	100.8	0.224	212.8 kHz

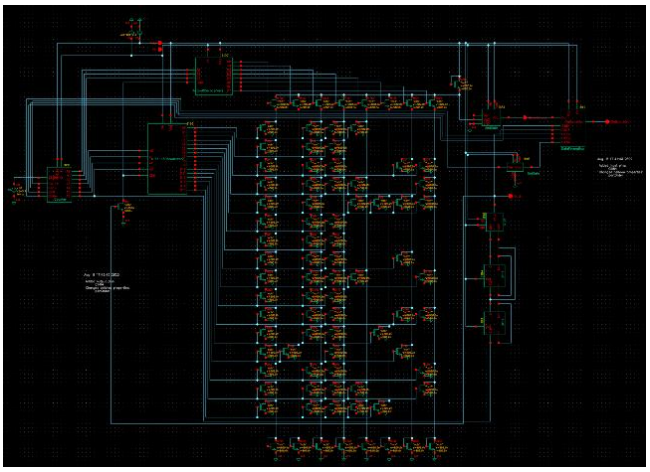


FIGURE 7. Overall Schematic of Digital Core Generator

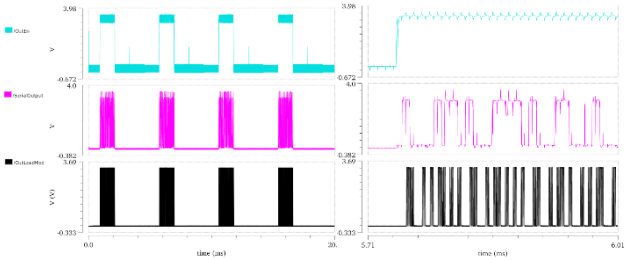


FIGURE 8. 128-bit code generated from Digital Core Generator following ISO 14443 standard

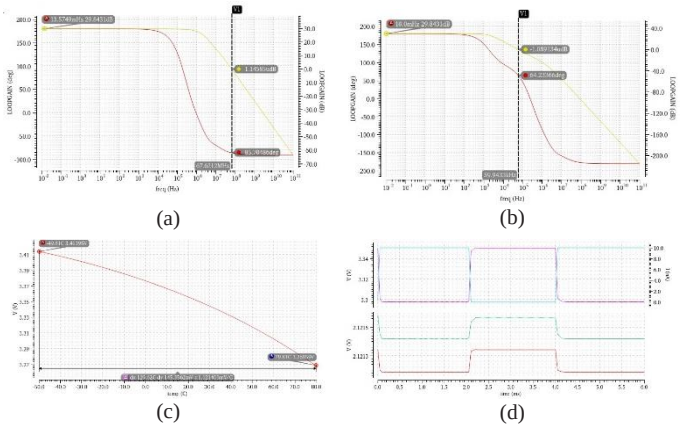


FIGURE 9. (a) frequency response of a temperature sensor using ideal op-amp (b) frequency response of a temperature sensor using op-amp (c) temperature versus voltage represented sensitivity (d) transient response of system after injecting current

Then, the decoder circuit has been tweaked to reduce complexity in order to reduce wasteful logic circuits, while counters require clock speeds to drive D-flip-flop signals, which makes it difficult to reduce energy consumption. Therefore, the POWER GATING technique has been used to reduce unnecessary energy consumption. As a result, the power can be reduced to 5.82 mW, which is less than the reference paper that consumes about 7-8 mW. The 128-bit code, as in Figure 8, can be generated clearly and without error.

B. *Temperature Sensor Circuit*

In the design above, since the experiment was done using an ideal op amp, thus, phase margin at the loop gain is very low as in Figure 9(a), with DC gain of 29.8 dB, phase margin at -85 deg, with a unity gain frequency of 67 MHz

The gain of the loop after inserting the actual op-amp has been designed, calculated and the experimental results are as follows from Fig. 9(b), with DC Gain of 29.8 dB, phase margin at 64 degrees, with a unity gain frequency of 60 kHz.

The output voltage proportional to temperature in degrees Celsius, from -50 to 80 degrees Celsius, in the DC mode, results in a rate of change of 1.12 mV/C, Fig. 9(c).

Simulate the temperature change by adding more current to the circuit and taking measurements in transient mode to determine the stability of the circuit and the ability to converge to constants value and convergence time, as shown in Fig. 9(d).

C. *Layout Design*

In this process, we follow DRC rule check (design rule constraints) which determine the dimensions of a minimum-size transistor and LVS (layout vs schematic) which compares the extracted netlist from the layout to the original schematic netlist to determine if they match. Figure 10 shows example of layout design of D flip-flop.

TABLE 2. COMPARASION BETWEEN THIS WORK AND REFERENCES

		This work	Jeong, H. IEEE '13[4]	K. Myny ISSCC '17[7]
NFC tag	frequency	13.56 MHz	-	13.56 MHz
	power	5.82 mW	-	7.5 mW
Temp. sensor	sensitivity	1.12 mV/C°	9 mV/C°	-
	open loop gain	29.8 dB	-	-
	op-amp gain	44.6 dB	-	-

V. CONCLUSION

In a study on the development of NFC tag sensors with flexible integrated circuit design technology, the transistors are quite different from silicon transistors because they are larger, work in the lower frequency band, and take up more space. There is also a lot of leakage current in the circuit, which increases the power consumption of circuits designed with this process. In addition, the transistors are only n-type; thus, they cannot provide a voltage reference to the circuit, so future additions to the p-type will make this type of transistor more efficient. can be used more concretely.

In the digital or NFC tag part, the design uses different loads instead of the p-type loads as shown in Figure 1 to form the logic gates, and different transistor sizes are required for each part of the circuit to work in the desired frequency band, including reducing power as much as possible. The circuit in the part that consumes the most energy is the 7-bit counting circuit because it must receive the 13.56 MHz signal directly from the receiver before converting to a lower frequency with a clock divider circuit. The power consumption is still very far apart (mW for this type of transistor and µW for silicon).

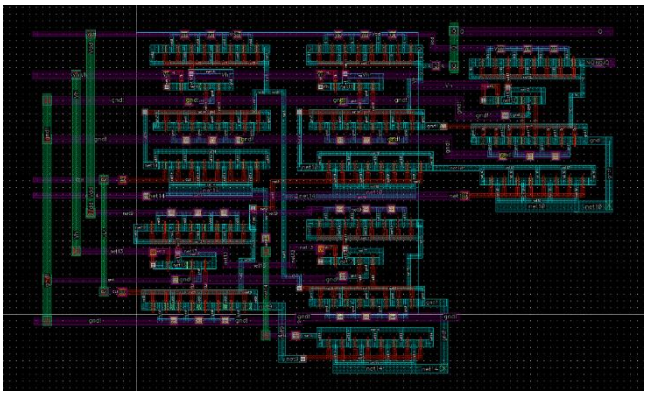


FIGURE 9. An example of D flip-flop layout design

As for the analog or temperature sensor, the subthreshold current of the transistor is subtracted and feedback is given to both so that both input pins of the op-amp are equal to get the current that changes depending on the temperature and bring the current to change to a voltage that depends on the temperature, but because the voltage reference cannot be established for the circuit Now, multiple bias voltages are required in the circuit. Moreover, there is also a problem with channel length modulation, which makes the current copy in the circuit unstable. There is also a parasitic capacitor due to the large size of the transistor, which affects the simulation.

Circuit design with flexible integrated circuit design technology still has a lot of instability and drawbacks. Development to add p-type transistors, including ways to reduce the size and leakage current, will result in a reduction in power consumption, increased stability, and better overall efficiency of the circuit. Implementation with various circuits will have a higher possibility in the future.

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