

说明：

一．从下面的 7 个设计题目中选 3 完成提交，选择规则如下：

1．Design Challenge 1 和 Design Challenge 2 任选 1

2．Design Challenge 3, Design Challenge 4, Design Challenge 5 从中选 2, 或者从中选 1, 再从 Design Challenge 6, Design Challenge 7 中选 1。

二．截止提交时间：2022.6.5-24:00

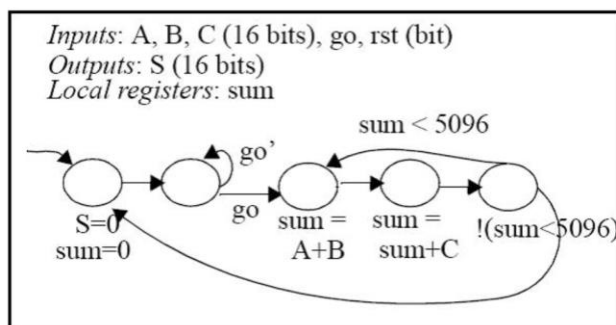
三．中英文作答均可，请写明选择的题目序号

Design Challenge 1

Create a high-level state machine that describes the following system behavior. The system has an 10-bit input A, a single-bit input C, and a 32-bit output S. On every clock cycle, if C=1, the system should add A to a running sum and output that sum on S. On every clock cycle, if C=0, the system should add 2*A to a running sum and output that sum on S. *Hint: declare and use an internal register to keep the sum.* Add a 1-bit input Clr to the system. When Clr=1, the system should clear the sum, S, to 0. Using the RTL design method, convert the high-level state machine to a datapath and controller.

Design Challenge 2

Using the RTL design method, convert the following high-level state machine to datapath and controller. Design the datapath to structure, but design the controller to the point of an FSM only.



Design Challenge 3

Design a high-level state machine for a digital thermostat for an air conditioner. The digital thermostat has a single-bit input on, and 8-bit input dtemp indicating the user's desired temperature, an 8-bit input ctemp providing the current temperature, and a single-bit output ac_on controlling the air conditioner. When on = 1, if the current temperature, ctemp, has been greater than the desired temperature, dtemp, for more than 5 minutes the thermostat will turn on the air conditioner by setting ac_on to 1. The air conditioner should remain on until the current temperature is less than or equal to the desired temperature.

Design Challenge 4

Assuming a 1 Hz clock input, design a high-level state machine for a programmable flashing LED display. The flashing light display has an 8-bit input ontime indicating the number of seconds the LED should be illuminated, an 8-bit input offtime indicating the number of seconds the LED should not be illuminated, a single-bit input enable, and a single output led to control the LED. If the enable input is 0, the LED will remain off (led = 0). Otherwise, the flashing LED display will alternate between illuminating the LED (led = 1) and not illuminating the LED (led = 0) according to the number of seconds provided by the ontime and offtime inputs.

Design Challenge 5

Design a high-level state machine for an event timer. The event timer has a 1-bit input e that will be 1 for one clock cycle indicating when each distinct event occurs. The event timer has two 8-bit outputs, et and ot . The et output will output the elapsed time in clock cycles between the last two events. The ot output will output the number of times the measured elapsed time between the last two events exceeded a user-defined threshold specified by an 8-bit input th . Ensure that your event timer design works correctly regardless of how fast events occur. Note: You do not need to convert the state diagram to a datapath and controller.

Design Challenge 6

Using the RTL design method, create an RTL design that counts the number of entries within a 128x32 register file A that are both greater than a 32-bit input Low and less than a 32-bit input $High$, i.e. $Low < A[i] < High$, outputting the count on an 8-bit output $InRange$. Create a datapath for your design, clearly labeling all data inputs/outputs, control inputs/outputs, and bit widths. Note: You do not need to convert your high-level state machine to an FSM.

Design Challenge 7

Create a high-level state machine that adds each register of one 128x8 register file to the corresponding registers of another 128x8 register file, storing the results in a third 128x8 register file. The system should only begin the addition when a bit input add is 1, and should not perform the addition again until it has finished adding (only adding again if add is 1).