Literature Review

Cheng Liu

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1 Accelerator Design for Graph Analytics

This paper [3] is essentially a graph accelerator implementation framework of Gather-Apply-Scatter model as in GraphLab [2]. It particularly focuses on iterative graph-parallel applications with asynchronous execution and asymmetric convergence. In order to support domain of graph processing, it has a template of hardware for common operations including memory access, synchronization and communication. In order to provide application specific optimization, a design space exploration is also supported like typical domain specific accelerators.

1.1 Highlights

Here are the list of highlights of this work.

- It targets graph applications with asynchronous execution and asymmetric convergence which doesn't work well on GPUs. This is also one of the major reasons that contributes to the the high power efficiency.
- It provides a hardware version of GraphLab [2] and maintains sequential consistency model with a synchronous unit (SYU) which essentially follows the edge consistency.
- memory access optimization: It has special cache, load, store units for each data type such as vertex information (VI) and edge information (EI). The cache structure is also configurable to meet the requirements of as VI and EI which have different locality characteristic.
- Graph partition: The framework has each accelerator optimized for fine grained operation level parallelism. And it also replicates the accelerator unit to explore high-level parallelism based on a static graph partition.

1.2 Questions

Is it necessary to maintain sequential consistency, will it be possible to loose the consistency model for more parallelism and higher performance?

According to the Graphicionado [1], cache may not be a good memory hierarchy for graph processing as the graph problems typically has poor locality. Will a

scratch pad memory work better for this design? This work utilize vertex and edge as the basic cache granularity instead of general data type may probably alleviate the problem.

The graph partition is not detailed, how does the partition affect the overall system performance?

2 Graphicioando

This paper utilize GraphMat [4] as the graph processing framework. With the observation that graph processing has ineffective usage of both on-chip memory and bandwidth, this work particularly optimizes the on chip memory usage over the baseline hardware accelerator obtained from GraphMat.

According to the pipeline of the baseline accelerator, the on chip memory access characteristics of the different pipeline stages are analyzed and a few optimizations are applied to remove the bottleneck of the accelerator pipeline. Here are the list of the major optimizations.

- It uses on-chip eDRAM as scratchpad memory to alleviate the random destination vertex and edge ID access. For the rest of the sequential memory access, a prefetch scheme is used to hide the memory access latency,
- Instead of replicating the accelerator directly, the authors divide the processing phase into source oriented portion and destination oriented portion. With this strategy, the hardware can be easily partitioned into parts without overlaps. Basically, the scratchpad memory is shared among the vertex processing streams.
- The number of edges are typically much larger than that of the vertex, so the edge access is usually a bottleneck of the accelerator design. This work uses an array of input queues and output queues connected with a crossbar to access memory and feed data to the downstream processing.
- In order to cope with graphs with larger scratchpad memory requirements, the graph is sliced, though the slicing is a simple one.

3 Database query with hardware/software co-design

This work is supposed to handle OLTP, but it doesn't show any special design for OLTP system.

References

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[3] Muhammet Mustafa Ozdal, Serif Yesil, Taemin Kim, Andrey Ayupov, John Greth, Steven Burns, and Ozcan Ozturk. Energy efficient architecture for graph analytics accelerators. In *Computer Architecture (ISCA), 2016 ACM/IEEE 43rd Annual International Symposium on*, pages 166–177. IEEE, 2016.

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