

Multi-Query Stream Processing on FPGAs

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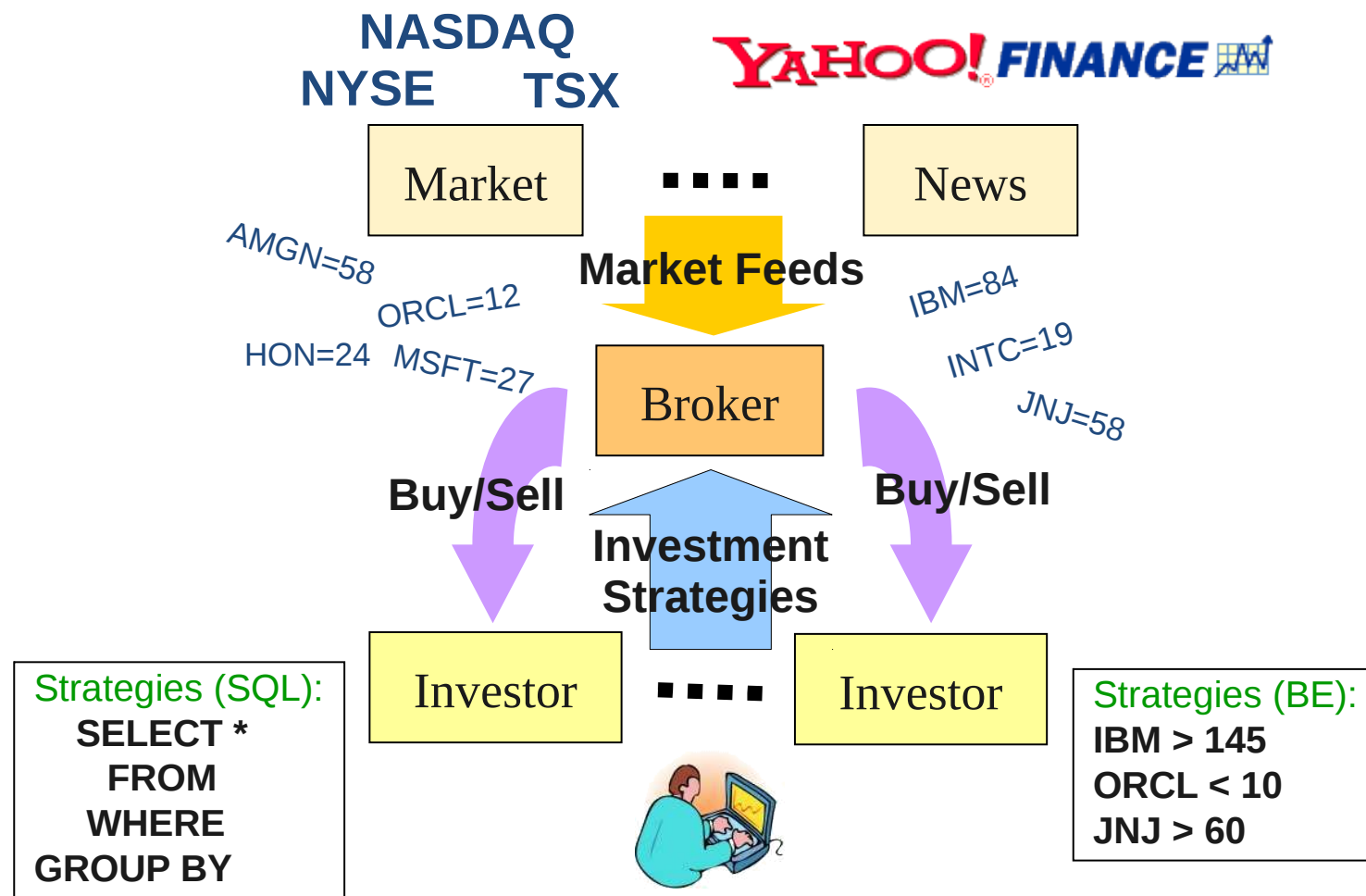
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Algorithmic Trading



(Complex) Event Processing

Data Streams



Patterns
(SQL Continuous Queries)

Real-time Data
Analysis



Matched Patterns

Event/Publication



Subscriptions
(Boolean Expressions &
XPath Expressions)

Content-based
Publish/Subscribe



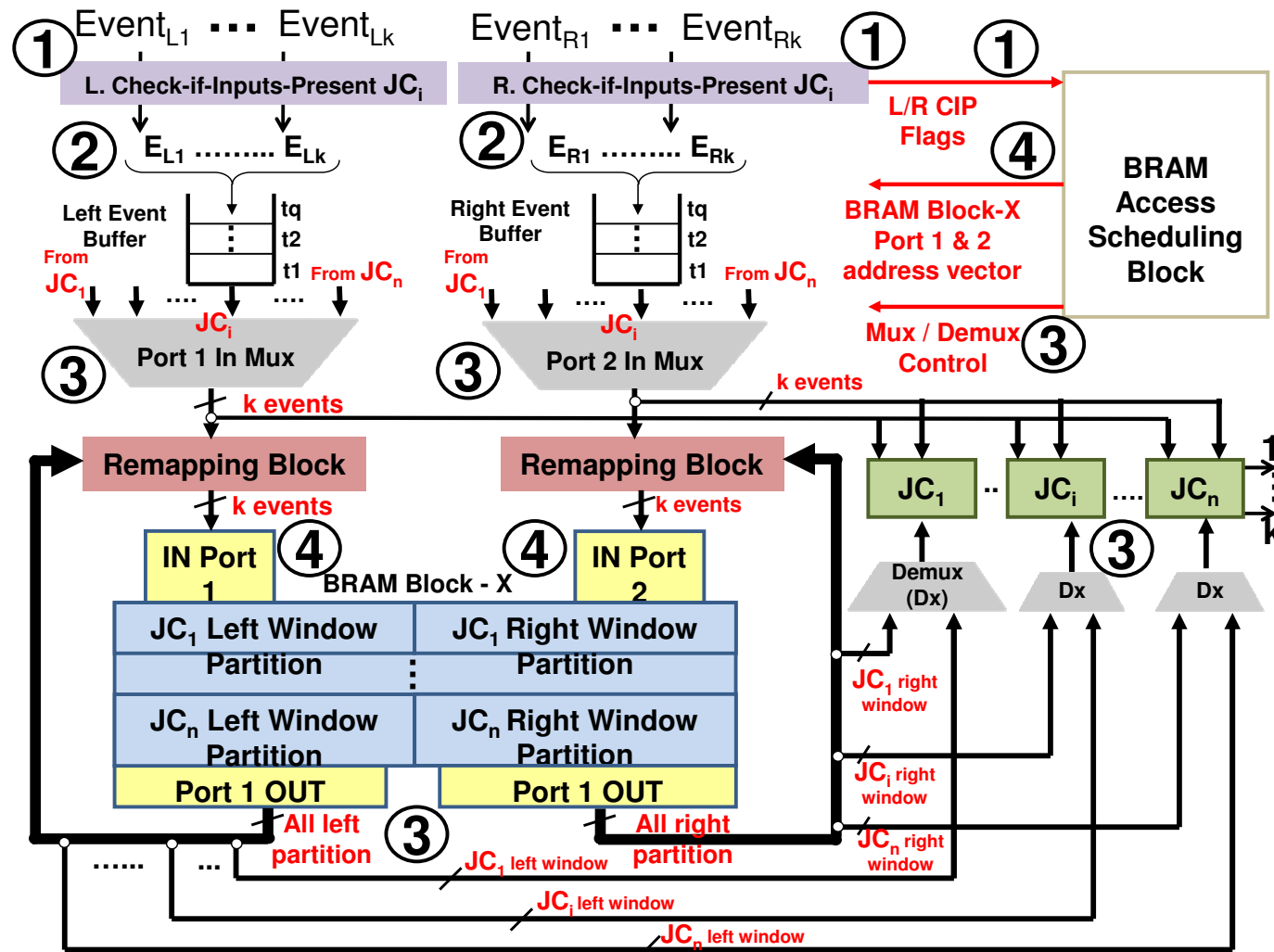
Matched Subscriptions

Why FPGAs

FPGA distinctive features

- 1 *Hardware reconfigurability*: re-configuring the application on-demand into a highly parallel custom processors
- 2 *Hardware parallelism*: eliminating inter-processor signalling and message passing overhead associated with the concurrency management at the program and the OS level
- 3 *Onboard packet processing*: using multiple high bandwidth (giga-bit) I/O pins to eliminate the OS layer latency overhead in moving data between input and output ports
- 4 *Cost-effective and Energy-efficient*

Overview of parallel join processing - Inter-parallelism

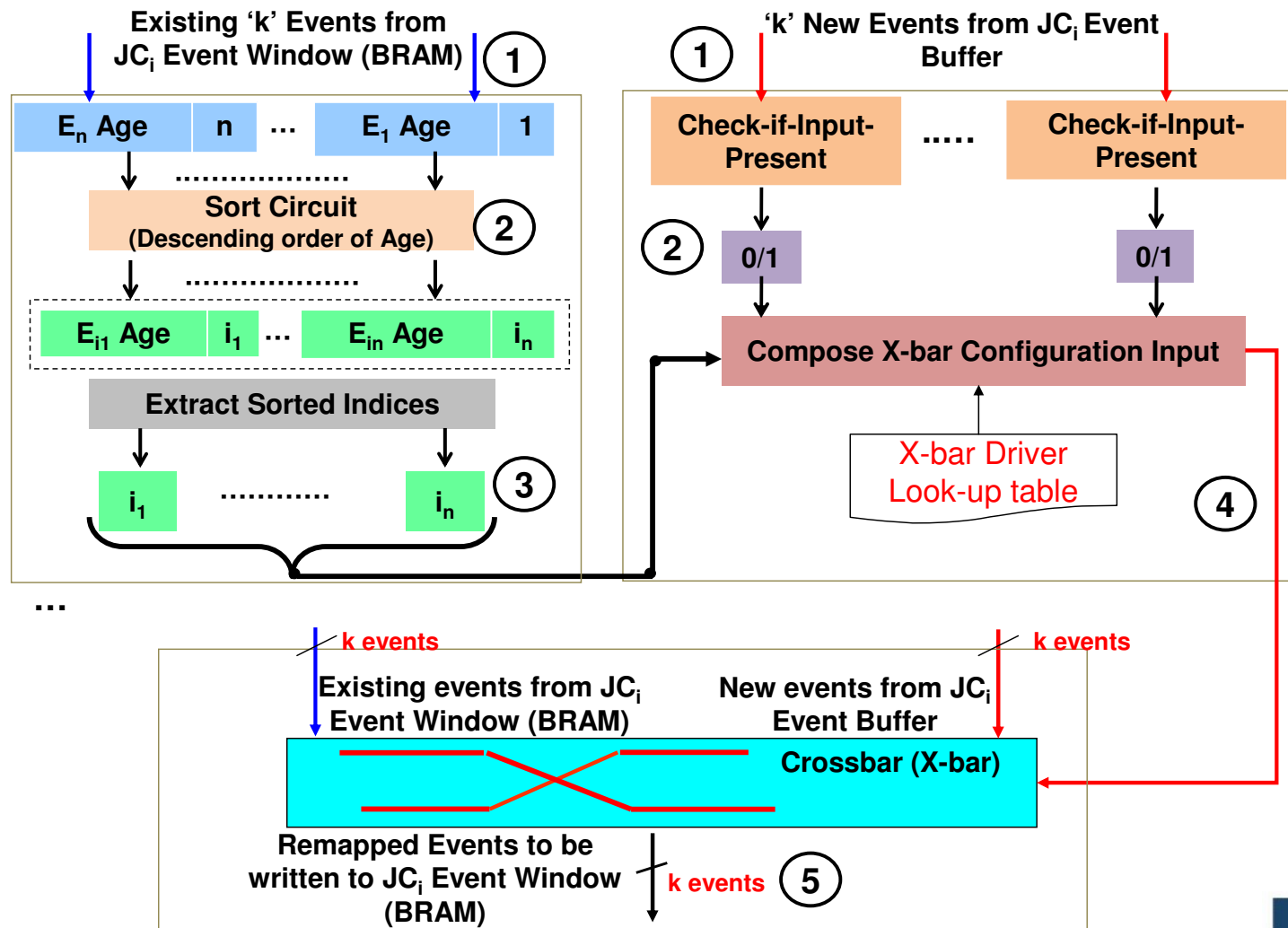


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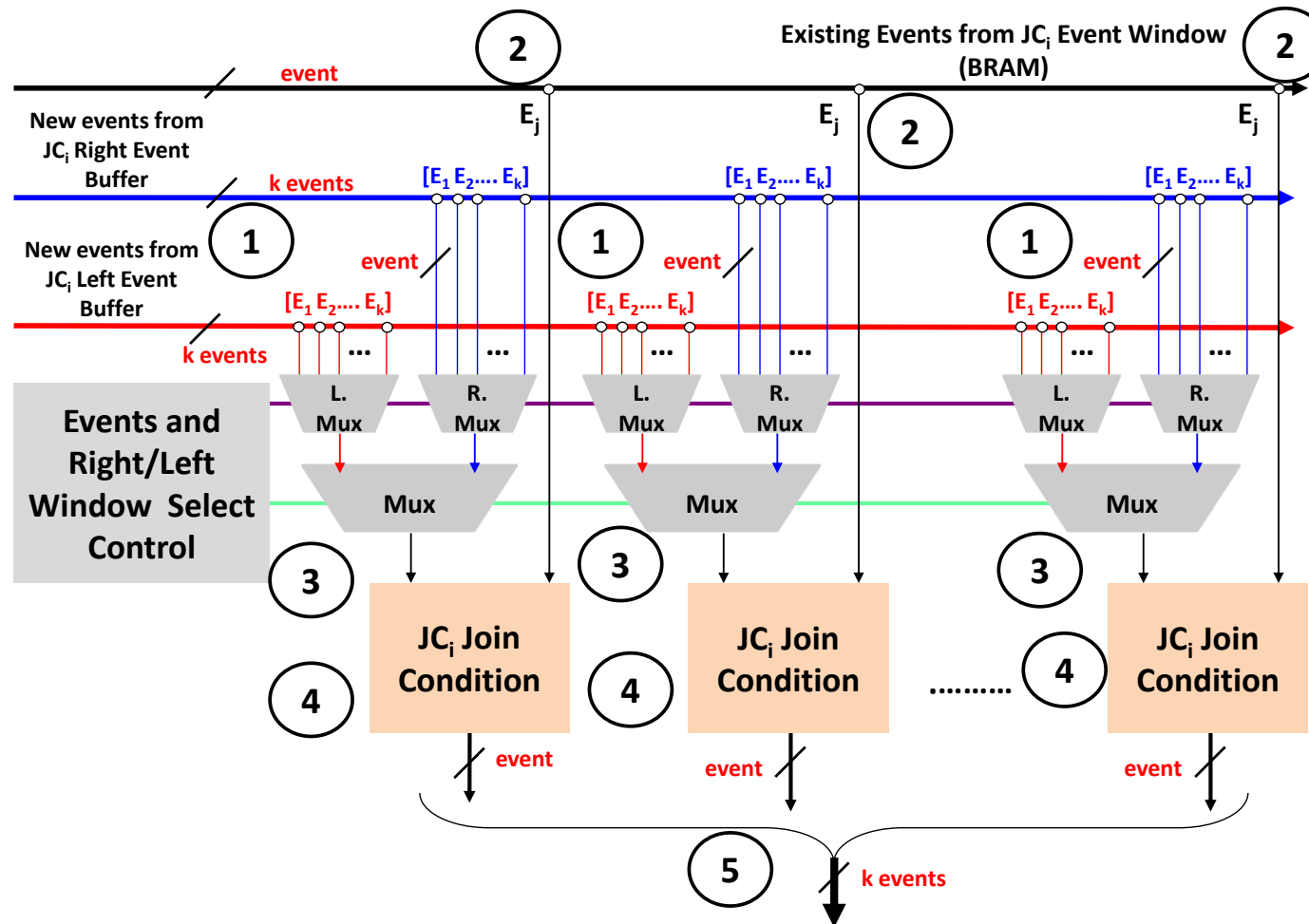


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Overview of parallel join processing - Coordination

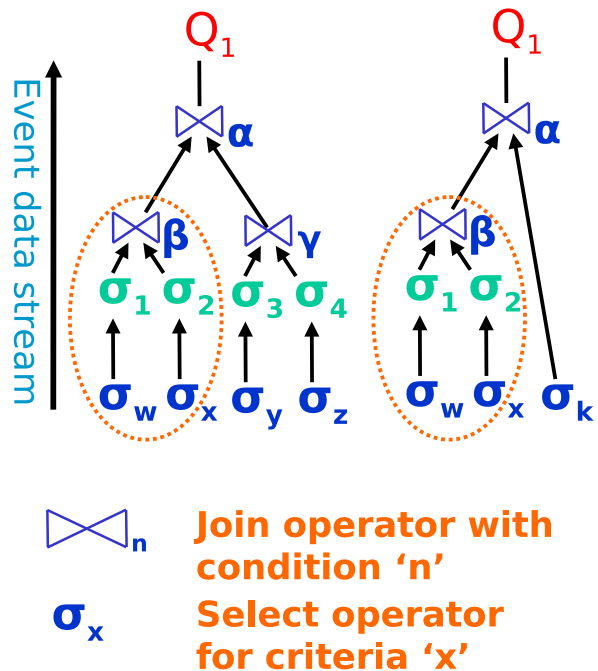


Overview of parallel join processing - Intra-parallelism

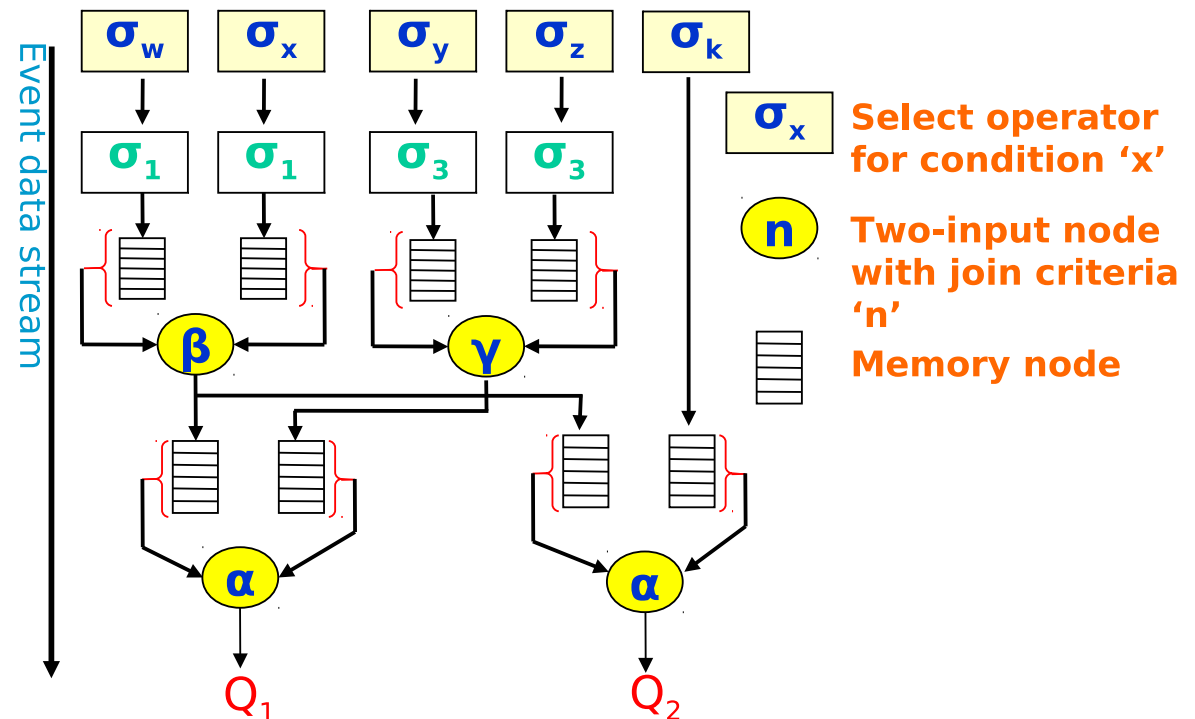


Complex Event Processing - Multi-query Processing (MQ)

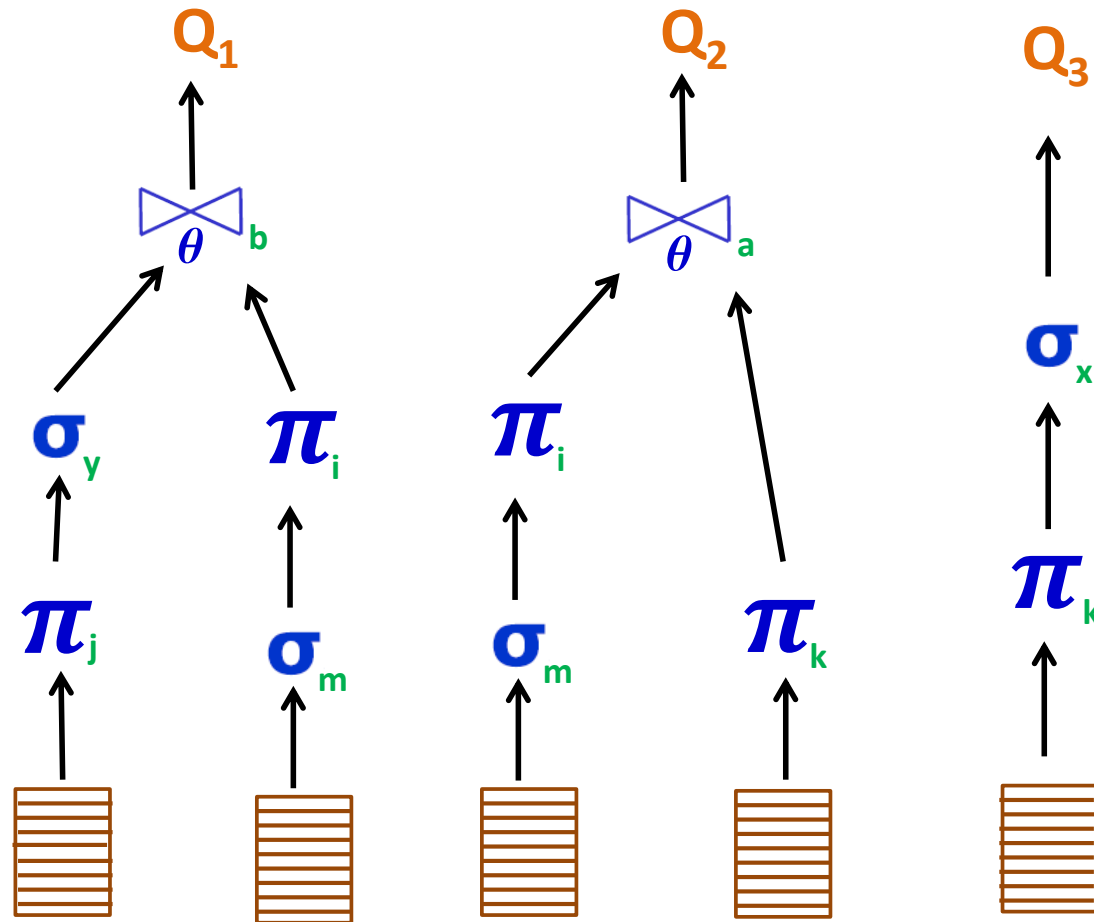
Standard SPJ query plan



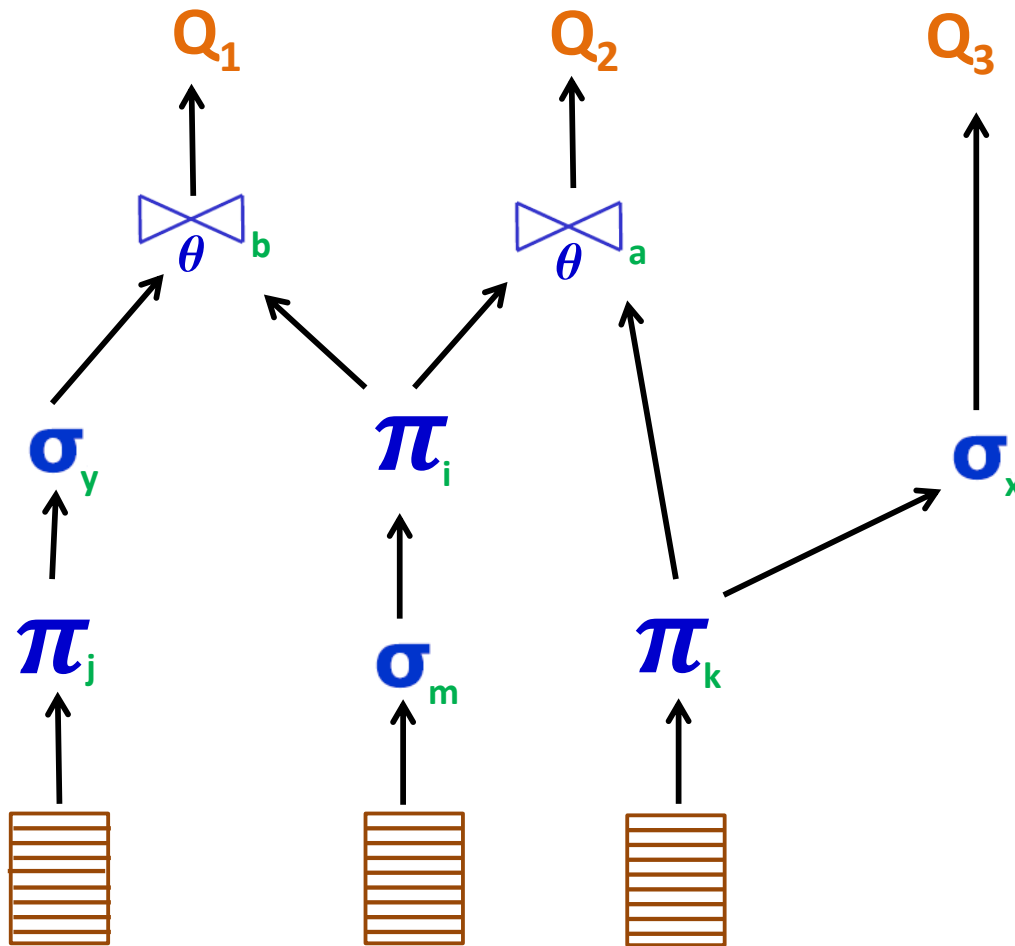
Global query plan for Q1 & Q2 via Rete network



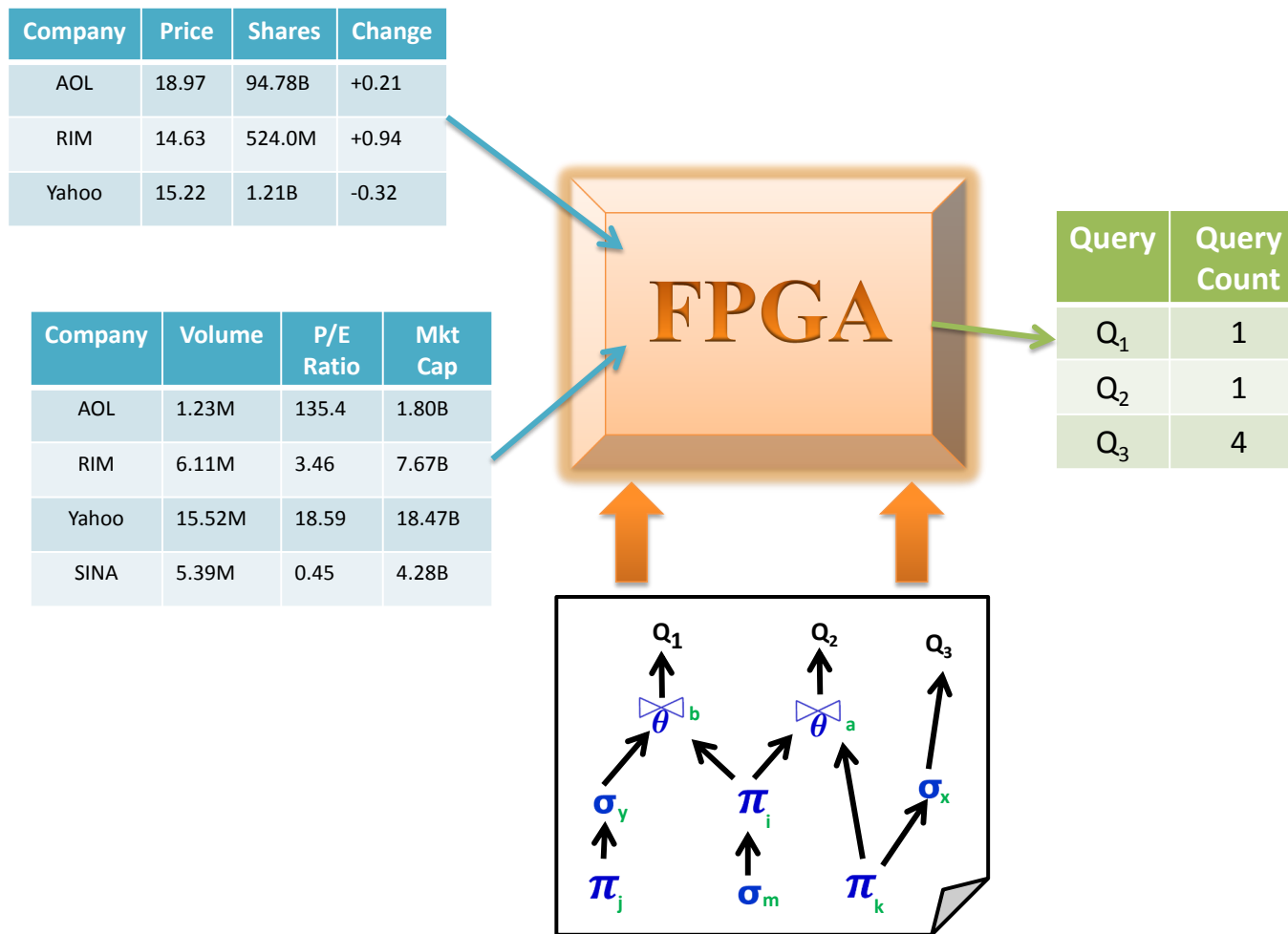
Multi-query Processing Example - Individual Query Plans



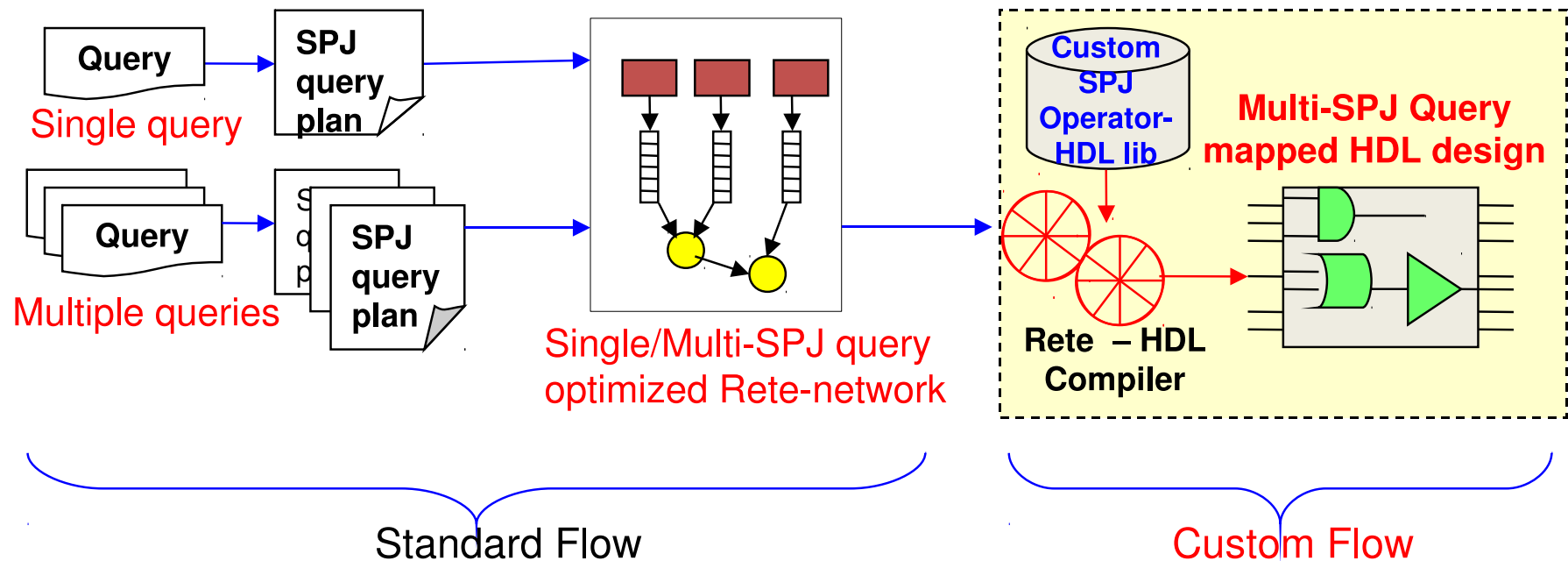
Multi-query Processing Example - Global Query Plan



Multi-query Processing Example Running on FPGA



Complex Event Processing - MQ Compiler



Thank You

Further Information:

- M. Sadoghi, H. Singh, and H.-A. Jacobsen. *fpga-ToPSS: Line-speed Event Processing on FPGAs*. **ACM DEBS'11**. Demonstration
- M. Sadoghi, H. Singh, and H.-A. Jacobsen. *Towards Highly Parallel Event Processing through Reconfigurable Hardware*. **(DaMoN'11, Collocated with ACM SIGMOD)**
- M. Sadoghi, M. Labrecque, H. Singh, W. Shum, and H.-A. Jacobsen. *Efficient Event Processing through Reconfigurable Hardware for Algorithmic Trading*. **VLDB 2010**

Synthetic/Real Workload Generator (BEGen):

- <http://msrg.org/datasets/BEGen>

FPGA Project Web Site

- <http://www.msrg.org/project/fpga-ToPSS>

