

*Ali*

ALDEN LUTHP

2 2 0 6 0 2 8 9 3 2

$$\begin{aligned} \textcircled{1} \text{ a. } 379_{10} &= 000101111011 \\ -379_{10} &= 100000010111011_{SM} \\ &= 11111101000010015 \\ &= 11111101000010125 \end{aligned}$$


$$\begin{aligned} \textcircled{b} 643_8 &= 0110100011 \\ -643_8 &= 1000000110100011_{SM} \\ &= 11111100101110015 \\ &= 11111100101110125 \end{aligned}$$

$$\begin{aligned} \textcircled{c} 67C_{16} &= 011001111100 \\ -67C_{16} &= 1000011001111100_{SM} \\ &= 111110011000001115 \\ &= 111110011000010025 \end{aligned}$$

$$\begin{aligned} \textcircled{d} 1112_8 &= 001001001010 \\ -1112_8 &= 1000001001001010_{SM} \\ &= 111111011011010115 \\ &= 111111011011011025 \end{aligned}$$

$$\begin{aligned} \textcircled{e} 521_7 &= 0100000100 \\ -521_7 &= 1000000100000100_{SM} \\ &= 111111101111101115 \\ &= 11111110111110025 \end{aligned}$$

$$\begin{aligned} \textcircled{2} \text{ a. } 10001_{25} + 1001_{15} \\ &= -15_{10} + (-6_{10}) \\ &= -21_{10} \\ &= 10010101_{SM} \end{aligned}$$

  
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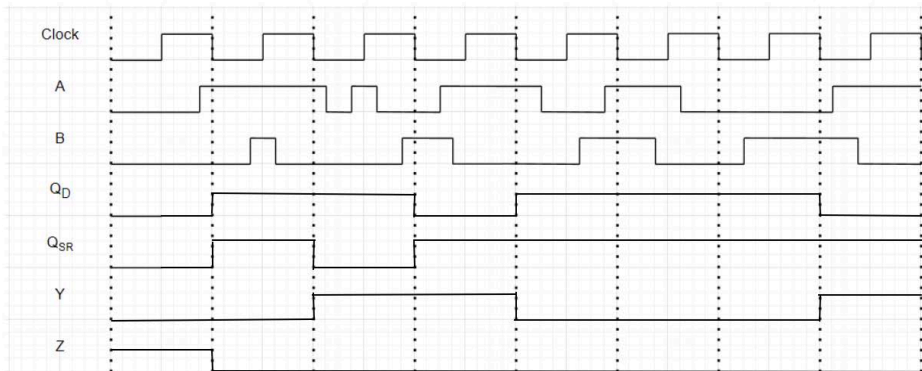
b)  $11001101_{25} - 37_8$   
 $= -51_{10} - 31_{10} = -82_{10}$   
 $= 10101101_{15}$

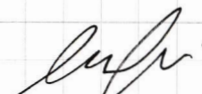
c)  $10101_{5M} - 1C_{16}$   
 $= -5_{10} - 28_{10} = -33_{10}$   
 $= 11011110_{15}$

d)  $11001101_{15} + 11001_2$   
 $= -50_{10} + 25_{10} = -25_{10}$   
 $= 1110011_{25}$

e)  $41_7 - 30_5$   
 $= 33_{10} - 79_{10} = -54_{10}$   
 $= 11001010_{25}$

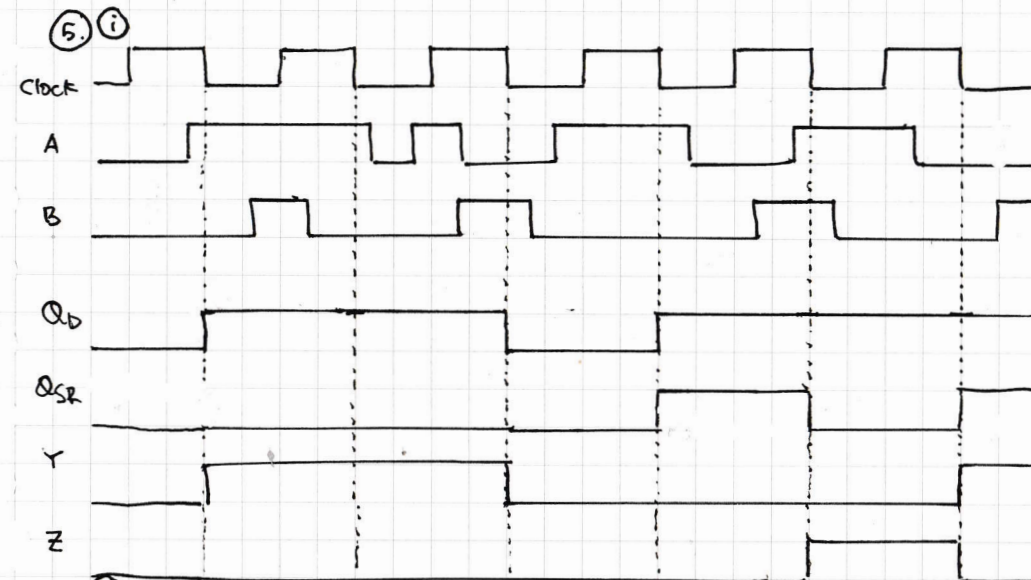
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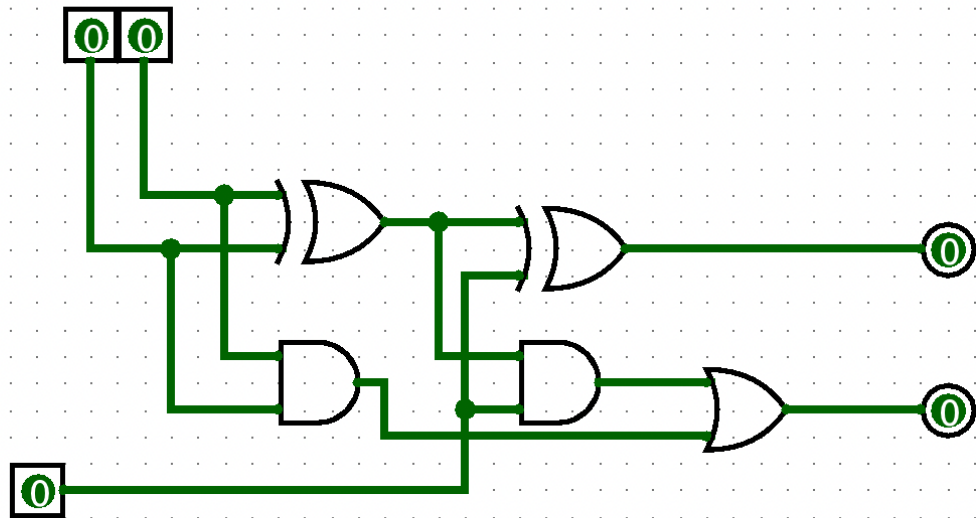
  
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- a) ④ Synchronous: perubahan terjadi berdasarkan clock pada waktu tertentu  
 Asynchronous: tidak ditentukan oleh clock

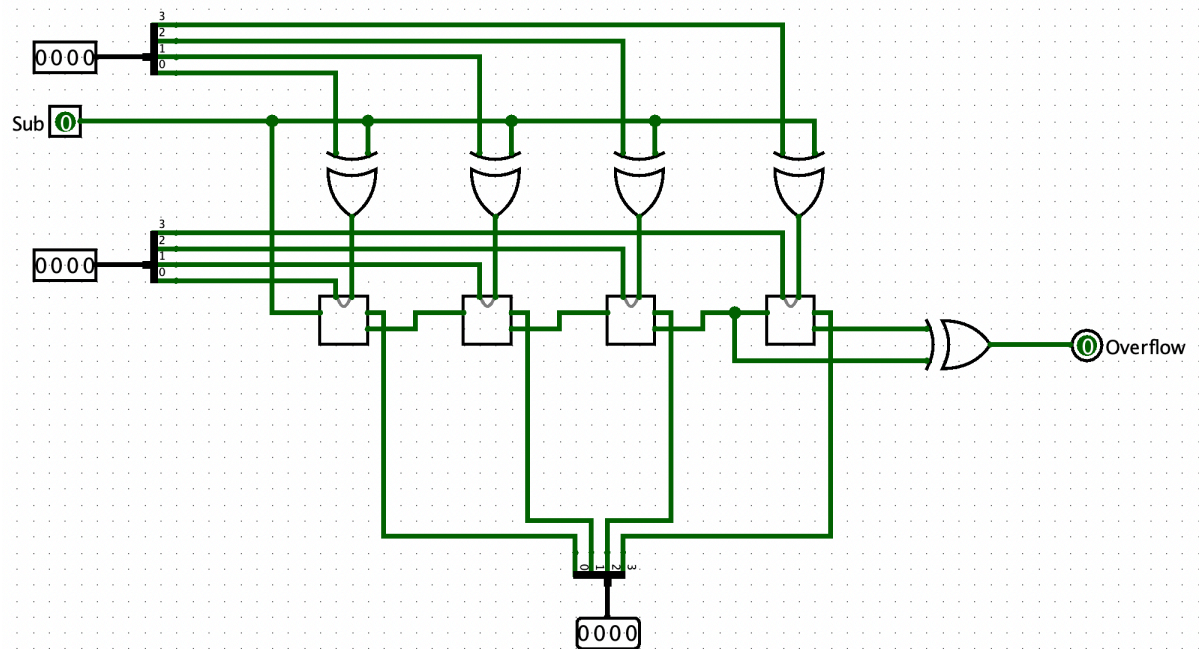
- b) Latch adalah sequential circuit yang edge level-triggered sedangkan flip-flop adalah sirkuit yang edge-triggered



### 3. One Bit Adder



### Four Bit Adder Cum Subtractor



The diagram illustrates a logic circuit for a 4-bit adder with overflow detection. The circuit includes the following components and connections:

- Inputs:** Two 4-bit inputs, both labeled `0110`, are connected to the top of a 4-bit adder block.
- Output:** The 4-bit adder block produces a 4-bit output labeled `1100`.
- Overflow Flag:** A green circle with the number `1` is labeled "Overflow", indicating that an overflow has occurred.
- Logic Components:**
  - A 4-bit adder block (represented by a square with a cross) that takes two 4-bit inputs and produces a 4-bit output.
  - A 4-bit multiplexer (MUX) with 4 data inputs (labeled 0, 1, 2, 3) and 4 outputs (labeled 0, 1, 2, 3). It is connected to the 4-bit output of the adder block.
  - A 4-bit comparator (represented by a square with a cross) that takes two 4-bit inputs and produces a 4-bit output.
  - Logic gates: Two 2-input AND gates and one 2-input OR gate are used to detect overflow. The inputs to these gates are connected to the 4-bit output of the adder block.

The diagram illustrates a 4-bit adder-subtractor circuit. It features three inputs on the left: a 4-bit register for 'B (2s Complement)' containing '0000', a 1-bit 'Subtractor' input set to '1', and a 4-bit register for 'A (2s Complement)' containing '0000'. These inputs are connected to a central 4-bit adder block, represented by a square with a curved top. The adder block has two inputs from the 4-bit registers and one from the 1-bit Subtractor. The output of the adder is a 4-bit result labeled 'A + B (Sign Magnitude)' with the value '0000'. Additionally, the adder block has an overflow output, indicated by a green line and a green circle containing '0', labeled 'Overflow'.