

8 Bit Serial in Serial Out Register

Group Members

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Objective

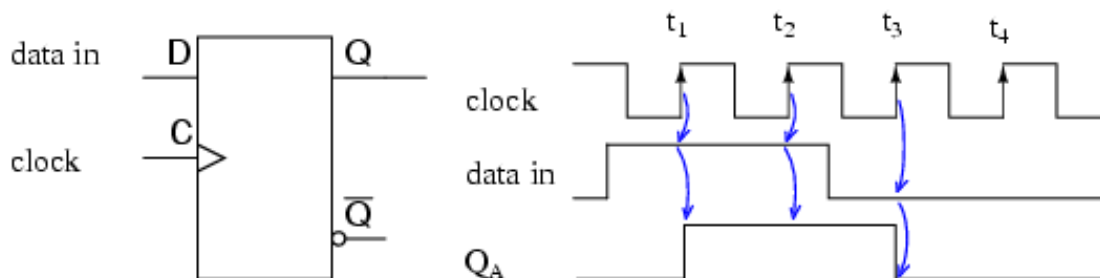
To model and simulate the operation of an 8-bit serial in serial Out (SISO) register using systemC.

Introduction

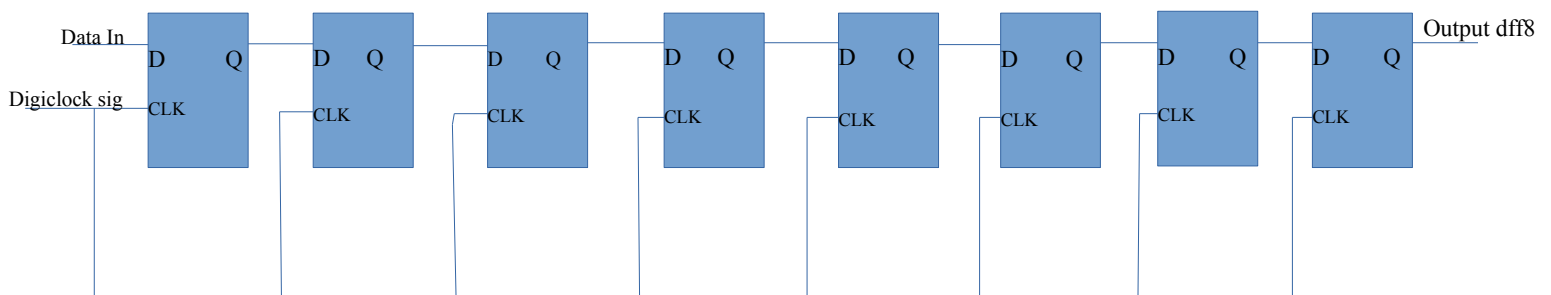
A register is a memory cell that holds data in a computer or any other computing device. An 8 bit register means that this register can hold 8 bits of data at a given time. Therefore, a serial in serial out register is a register whereby an input is fed into the register at one end in some order, and an output comes out of the end of that register in the exact same order in which they were fed into the register.

Methodology

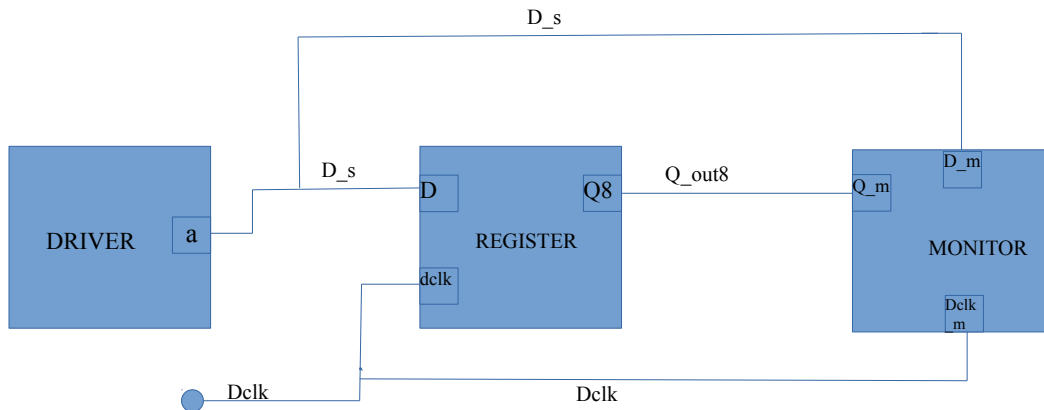
It was decided that a D-flipflop would be used to build this type of register. A D-flipflop is a device that is capable of holding one bit of data at any single time. Therefore if cascaded with other D-flip flops, may be able to hold more bits of information at any given time. The following is a schematic of a D- flip flop:



It has a data input pin (D) a clock input pin (C), and a data output (Q) . The initial output is low. Therefore, if this is a positive edge triggered D flip-flop, then when the clock goes from low to high and the data input D is high at this point, then the output will change to high, the same value as the input, else if the clock is low at this point then the output (Q) will not change. The same applies if the data signal is low when the clock is going from low to high, the output will change from high to low if it was high, or will remain low if it was already low. Thus by virtue of the output (Q) remaining the same despite the change in clock from high to low until the next clock cycle, we say that this flip flop “stores data.” Therefore to create our register, we cascaded 8 of these flipflop forming the following circuit.



From this circuit, we were able to see how the data from one D flip-flop will flow into the next. And from that, we were able to design a model of computation as below:



Driver Module

The input to register is produced from here. It is communicated through the D_s signal

Register Module

This module consists of the implementation of the register using the flip flops. The D flip-flops were cascaded at this point in order to allow for data transfer from one flip-flop to the next. The clock sensitivity of the D flip-flop (ie. Which clock edge the output of the D flip-flop, Q, responds to) was also configured here.

Monitor

This was used to monitor the timing diagrams of the input to the register, the clock signal and the output of the register to determine if the simulation was working properly.

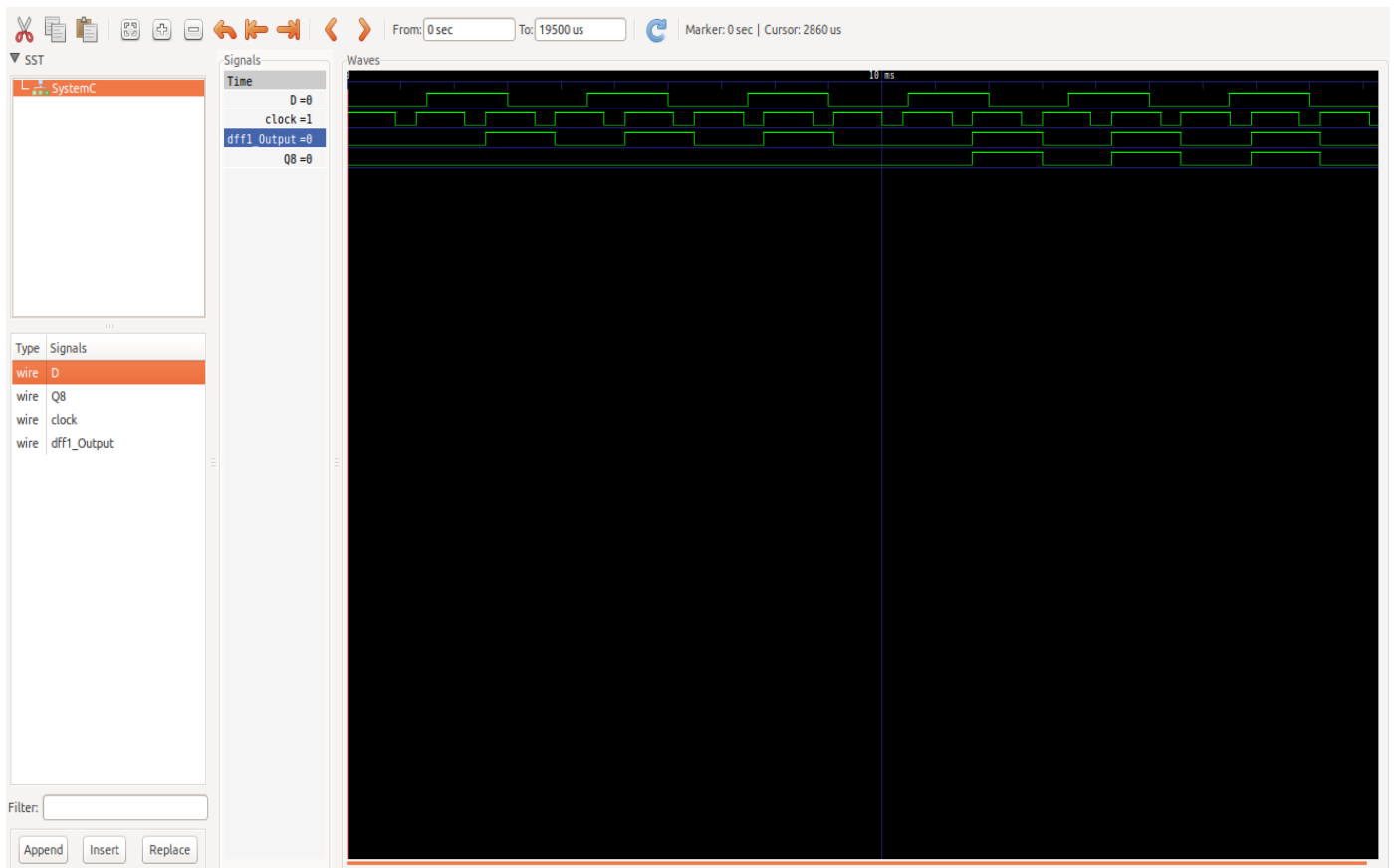
From the above model we were then able to easily develop our SystemC code.

Results

The command line output:

```
Info: (I703) tracing timescale unit set: 1 ns (trace.vcd)
at 11700 us D is: 1 Q8 is: 1
at 13 ms D is: 0 Q8 is: 0
at 14300 us D is: 1 Q8 is: 1
at 15600 us D is: 0 Q8 is: 0
at 16900 us D is: 1 Q8 is: 1
at 18200 us D is: 0 Q8 is: 0
gtkwave trace.vcd
```

The trace file:



Discussion

From the final output of the register, it is clear that the first input appears here after 8 complete clock cycles and that the output only changes to the value of the input *only* when the clock moves from low to high.

Conclusion

We thus concluded that our objective was met as we were able to model and simulate the functioning of an 8 bit SISO register.

References

1. SystemC: From the Ground Up , 2010 ed
D.C. Black, J. Donovan, B. Bunton, A. Keist