Computer Architecture - Homework 3 Report

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StudentID:B11901164 Name:陳秉緯

**Part1. Add new components to gem5 config.**

* **1-1: Implement L2 cache in gem5 config**
* **1-2: Draw and analyze the program results based on the config**

Part1-1. Show screenshots of your program running successfully (refer to P.11) (15%)

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Part1-1. Show screenshots of your program and cache summary (refer to P.12) (15%)

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| <program summary> |
| <L1 cache summary> |
| <L2 cache summary> |

Part1-2. Draw a graph based on the different hardware config (refer to P.13-14). (40%)

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| --- |
| <L1-I cache size> |
| <L1-D cache size> |
| <L2 cache size> |
| <L1-I associativity> |
| <L1-D associativity> |
| <L2 associativity> |

**Part2. Analyze and find the optimal config based on the application**

* **Cache Size: 1KB ~ 128KB**
* **Associativity: 1 ~ 8**

Part2-1. Find the optimal config settings for this program. (10%)

|  |  |  |
| --- | --- | --- |
| Config | Cache size (KB) | Associativity |
| L1-I cache | 32 | 8 |
| L1-D cache | 64 | 8 |
| L2 cache | 1 | 8 |

|  |  |
| --- | --- |
| Performance | Score |
| 1287574000 | 12 |

※ Save your optimal config in gem5\_args.conf

Part2-2. Explain why this config achieves optimal performance ? (20%)

1. L1-I Cache and L1-D Cache size and associativity:
   * These sizes are large enough to accommodate most of the frequently accessed instructions and data.
   * The high associativity (8-way) reduces conflict misses, allowing the cache to store data more effectively.
2. L2 Cache size and associativity:
   * The optimal L1 cache sizes are already sufficient to hold most data, leading to fewer L2 accesses.
   * The high associativity (8-way) reduces conflict misses, allowing the cache to store data more effectively.