**Computer-Aided VLSI System Design**

TetraMAX® Lab: Automatic Test Pattern Generation (ATPG)

**Objectives:**

In this lab, you will learn:

How to generate single stuck-at fault test patterns for our simple ALU

**Download Files from CEIBA website**

1. Create a work directory and copy the lab files into it
2. check if you have these files:

|  |  |
| --- | --- |
| **Filename** | **Description** |
| *ALU\_syn\_dft.v* | Scan-ready gate level netlist for the simple ALU |
| *ALU\_syn\_dft.spf* | STIL format test protocol file (generated by DFT Compiler) |
| *atpg.tcl* | Reference script in this lab |

1. Check the contents of these files.

**Invoke Tetramax**

To invoke Tetramax, first include the following C shell script

**source /usr/cad/synopsys/CIC/tmax.cshrc**

And then, you can do either one

**tmax -nogui** (command mode)

**tmax &** (GUI mode)

In this Lab, we will use the command mode. You are welcome to try the GUI mode. In the GUI mode, you can type in your commands in the command line, located at the bottom of the window.

**STEP 1: Read Input Files**

Read in your design and cell library

**read\_netlist ALU\_syn\_dft.v**

Read in cell library in Verilog format

**read\_netlist <your library path>/tsmc13.v**

NOTE: unlike the design compiler, Tetramax does not take the library in .ddc

format. Instead, Tetramax reads library in Verilog format.

The location of tsmc13.v is at:

**/home/raid7\_2/course/cvsd/CBDK\_IC\_Contest/CIC/Verilog/tsmc13.v**

**STEP 2: Build Model**

1. This step builds a model of your design for ATPG.

**run\_build\_model ALU**

Question: How many violations do you see? \_\_\_\_\_\_\_\_

1. To probe further for the violations, type

**report\_violations -all**

Examine these violations,

Question: What causes these violations? \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

NOTE: You may see some warning messages. Should you ignore these warning messages? Try to explain these warning messages.

**STEP 3: Run DRC**

The spf file tells the ATPG how to operate the circuit in test mode.

This step run design rule checking. Please type,

**run\_drc ALU\_syn\_dft.spf**

Question: Does our design pass all rules? \_\_\_\_\_\_\_\_\_

**STEP 4: Set fault list**

Specify the fault model. We use stuck-at fault model in this lab.

**set\_faults -model stuck**

Inject all faults into the circuit under test

***add\_faults -all***

**STEP 5: Run ATPG**

To obtain the maximum test coverage while minimizing the number of patterns, we can set the ATPG options as follows.

**set\_atpg -abort\_limit 100 -merge high**

**run\_atpg -auto\_compression**

Question: How many total faults do we have? \_\_\_\_\_\_\_\_\_\_\_\_\_

**STEP 5 Review Results**

To get a summary of your ATPG results, type

**report\_summaries**

Question 1: How many faults are detected? \_\_\_\_\_\_

Question 2: What is the fault coverage? \_\_\_\_\_\_

Question 3: How many test patterns do we have? \_\_\_\_\_\_

Question 4: Which fault(s) are not detected? \_\_\_ Do you know why? \_\_\_\_

The default test coverage is obtained by using uncollapsed fault list. To use the collapsed fault list, type

**set\_faults -report collapsed**

**report\_summaries**

TetraMAX ATPG defines test coverage and fault coverage as follows:





To display fault coverage in addition to test coverage with the summary report type

**set\_faults -fault\_coverage**

**report\_summaries**

**STEP 7 Save Patterns**

To see your test patterns, type

**report\_patterns -all**

Save your patterns into files. There are many formats supported by TetraMAX. WGL (Waveform Generation Language), and STIL (Standard Test Interface Language) are two of the popular formats. Depends on the test equipment you use, you can choose other different formats. Although ATPG should give us “correct” patterns, it is always good to verify the patterns. TetraMax can also generate script shell script for either NCVerilog or VCS to simulate patterns. Use –nc or –vcs option to generate shell script for the STIL format patterns.

**write\_patterns ALU\_syn\_ATPG.wgl -format WGL**

**write\_patterns ALU\_syn\_ATPG.stil -format STIL -vcs**

Question: How many files do you get by typing the last command? \_\_\_\_\_\_

Try to run Verilog simulations and see if you get correct results.

**Checkpoints:**

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your ATPG results.
2. Answer the questions in this lab.

**END of LAB**

Creator:

1st Edition: Chien-Mo Li, 2001

2nd Edition: Yu-Lin Chang, 2004

3rd Edition: Jui-Hsin Lai(Larry), 2008

4th Edition: Bing-Chuan Bai, 2010

5th Edition: Bing-Chuan Bai, 2011

6th Edition: Kuan-Yu Liao, 2012

7th Edition: Chieh-Fu Chu, 2013

8th Edition: Kuan-Yen Huang, 2015

9th Edition: Po-Wei Chen, 2018