**Computer-Aided VLSI System Design**

STA Lab : Static Timing Analysis

**Objectives:**

In this lab, you will learn:

1. How to use STA tools to analyze the timing of synchronous digital ASICs.

2. How to fix these problems of the timing violations.

**Environment Setup:**

1. Source the license file:

**source /usr/cad/synopsys/CIC/primetime.cshrc**

**Download files from course website**

1. Create a work directory and copy the lab files into it.
2. Check if you have these files.

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| **Filename** | **Description** |
| *ALU\_syn.v* | Gate level Verilog code for the simple ALU |
| *ALU.spef* | Time and RC information file for the simple ALU |
| *ALU\_pt.script* | Script to run PrimeTime |
| *ALU\_syn.script* | Script to run Design Vision (including generating *ALU.spef*) |
| *.Synopsys\_dc.setup* | Synopsys DFT Compiler setup file (same format as Design Vision). Define search paths, library name etc. |

**Invoke PrimeTime STA tool**

To invoke PrimeTime, you can do either one

**pt\_shell** (command mode)

**primetime &** (GUI mode)

We encourage everybody to use command mode because:

a. The command mode helps you to keep a record of what you have done.

b. The command mode runs more efficiently than GUI mode.

c. The command mode helps you to lookup the manual/reference quickly.

In spite of the above advantages, command mode sometimes is not as good as GUI mode in terms of debugging the schematic problem. We will use command mode throughout this Lab. You are welcome to try the GUI mode by yourself.

**Start Operating PrimeTime STA tool**

***STA Environment Setting for TSMC 0.13um Technology:***

1. Set search path *(If it has not been set up yet)*

**set search\_path ". /home/raid7\_2/course/cvsd/CBDK\_IC\_Contest/CIC/SynopsysDC/db"**

2. Set link library

**set link\_path "\* typical.db fast.db slow.db"**

***Read Gate level Netlist Files and Link design:***

1. Type these lines to read in CIC .18 library and your gate level netlist.

**read\_verilog ./ALU\_syn.v**

2. Link all designs

**link\_design ALU**

Note, you have to check the search path and include library, if you get the error message after step 2.

***Read Timing and RC information:***

Reads leaf cell and net timing and RC information from a file in SPEF Format and uses that information to annotate the current design.

**read\_parasitics ALU.spef**

*Note: The file can be get during synthesis with “write\_parasitics” comment.*

***Set Operating Conditions:***

**set\_operating\_conditions typical -library typical**

***Set Design Constraints:***

This step tells the Dft Compiler how many scan chains you want. You can also specify the names of scan related pins (scan\_enable, scan\_in, scan\_out). We will let Dft Compiler to choose the pin names for us.

1. Specify the clock name, period, and clock characteristic

**create\_clock -period 10 -waveform {0 5} [get\_ports clk]**

**set design\_clock [get\_clock clk]**

**set\_clock\_uncertainty 0.5 $design\_clock**

**set\_clock\_latency -min 1.5 $design\_clock**

**set\_clock\_latency -max 2.5 $design\_clock**

**set\_clock\_transition -min 0.25 $design\_clock**

**set\_clock\_transition -max 0.30 $design\_clock**

**set\_propagated\_clock $design\_clock**

2. Set wire load model

**set\_wire\_load\_model -name "ForQA" -library "typical"**

3. Set wire load mode

**set\_wire\_load\_mode top**

4. Report

**report\_design**

**report\_reference**

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| Questions:  How many reference cells will you have? \_\_\_\_\_.  And total area size = \_\_\_\_\_\_\_\_. |

***Timing analysis and report possible problems:***

This step checks your scan specification for consistency. Please type the following commands to set the input/output delay:

**set\_input\_delay 1.5 [get\_ports inputA] -clock $design\_clock**

**set\_input\_delay 1.5 [get\_ports inputB] -clock $design\_clock**

**set\_input\_delay 1.5 [get\_ports instruction] -clock $design\_clock**

**set\_input\_delay 1.5 [get\_ports reset] -clock $design\_clock**

**set\_output\_delay 1.5 [get\_ports alu\_out] -clock $design\_clock**

And then check the timing:

**check\_timing**

**report\_timing**

**report\_bottleneck**

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| Questions:  Does the design meet the timing requirement? \_\_\_\_\_\_\_\_.  Find the critical path: Start-point = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  End-point = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |

Change the setting and check the timing again:

**create\_clock -period 2 -waveform {0 1.0} [get\_ports clk]**

**report\_timing**

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| Questions:  Now, does the design meet the timing requirement? \_\_\_\_\_\_\_\_.  Is it the setup time violation or the hold time violation? \_\_\_\_\_\_\_\_.  If all other setting is the same, what is the maximum clock period for the design to meet the timing requirement? \_\_\_\_\_\_\_\_ ns.  Try to modify the setting and verify the number you get with STA tool. Do you succeed? \_\_\_\_\_\_\_\_. |

Change the setting and check the timing again:

**create\_clock -period 10 -waveform {0 5.0} [get\_ports clk]**

**set\_output\_delay 8 [get\_ports alu\_out] -clock $design\_clock**

**report\_timing**

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| Questions:  Now, does the design meet the timing requirement? \_\_\_\_\_\_\_\_\_\_\_.  Where is the new critical path: Start-point = \_\_\_\_\_\_\_\_\_\_\_\_\_  End-point = \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |

***Reports:***

1. Show the types of checks being done (setup, hold, min pulse width, recovery, removal and so forth)

**report\_constraint**

**report\_constraint -all\_violators**

**report\_analysis\_coverage**

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| Questions:  How many timing violations are there in the design? \_\_\_\_\_\_\_\_\_\_ |

2. Change the setting and check the report again:

**set\_clock\_uncertainty 0.0 $design\_clock**

**report\_constraint**

**report\_constraint -all\_violators**

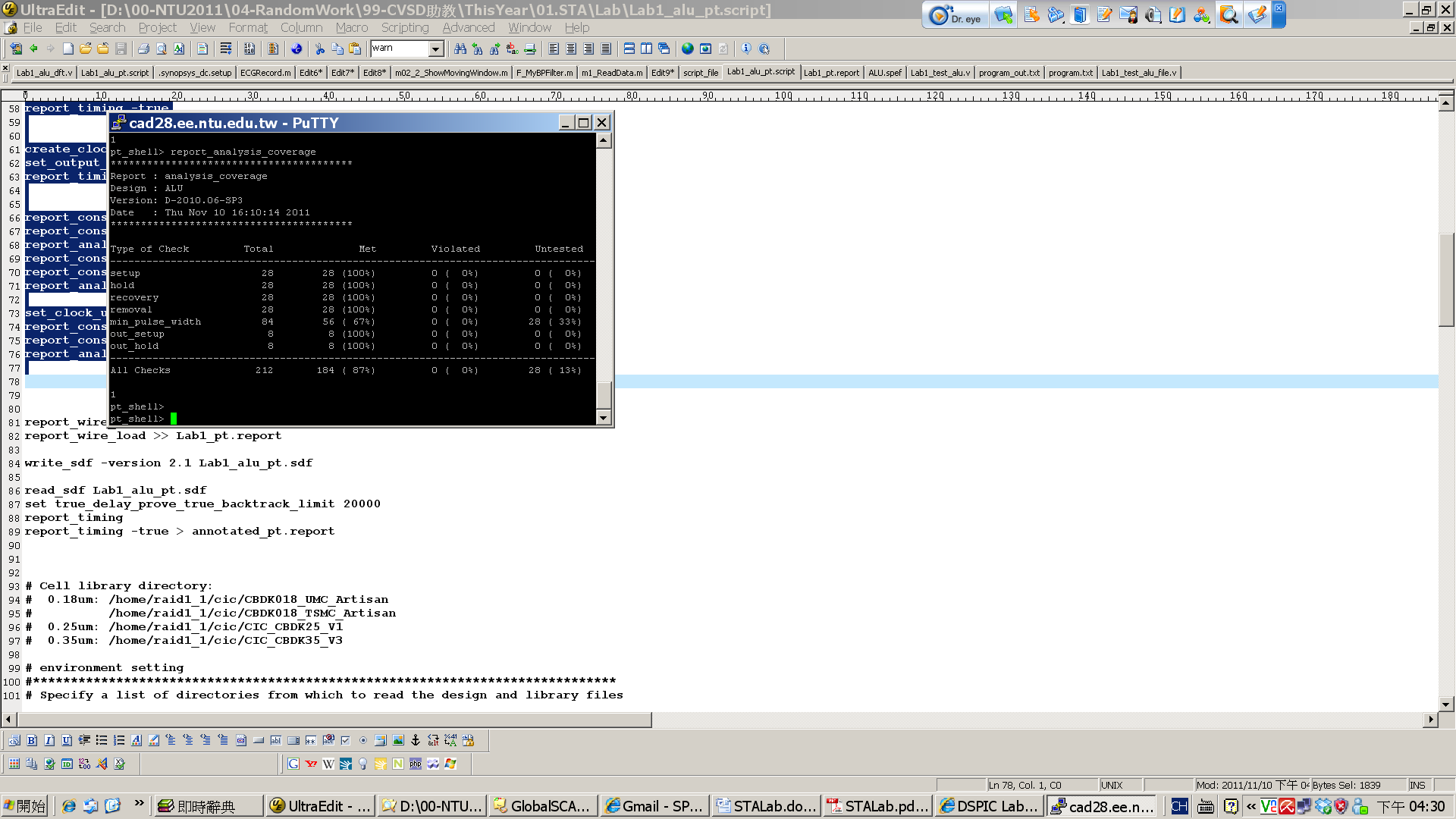
**report\_analysis\_coverage**

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| Questions:  Why are the hold-time violations fixed? Think about the clock setting in the previous synthesis Lab and try to explain. Note that the synthesis script can be referred in “*ALU\_syn.script*.” \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ |

**Checkpoints:**

Please check with TAs before leaving this lab to make sure the following goals are accomplished and to get credits.

1. Show your final STA results as follows.



2. Show your answers of the questions in this lab document.

**END of LAB……………………………………………………………………………….**

Creator:

1st Edition: Huai-Yi Hsu, 2002

2nd Edtion: Yu-Lin Chang, 2004

3rd Edition: Yu-Lin Chang, 2006

4th Edition: Jui-Hsin Lai (Larry), 2008

5th Edition: Fu-Chen Chen, Chieh-Li Chen 2009

6th Edition: Yung-Lin Huang 2010

7th Edition: Tung-Chien Chen 2011

8th Edition: Shuo-Ren Lin 2012

9th Edition: Shin-Yann Ho 2013

10th Edition: Kuan-Hua Tu 2016