2017

Final Report

TEST TOOL SIGNAL GENERATOR FOR EVA BENCHTEST

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Version 1

NXP SEMICONDUCTORS N.V. | Gerstweg 2, 6534 AE Nijmegen

Final Report

----Test tool signal generator for EVA benchtest

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Summary

NXP Semiconductors N.V. is a company to produce a vast range of product, including In-Vehicle Network. To make sure the products work well, the company NXP designed a test tool named EVA to test the devices produced by NXP. On the EVA, different kinds of boards can be installed in order to test different kinds of chips. And one of the boards, which calls signal generator board, is used to generate eight channels of square waveform. But malfunction can also happen on EVA, so the company need test tools to test different components of EVA, including the signal generator board. The signal generator board can generate eight channels of square waveforms and the company need a test tool to test the duty cycle, frequency and voltage of all eight channels of waveforms.

This report describes the design method and design result of a test tool to test the duty cycle, frequency, and voltage of the square waveform of the signal generator board by using a microcontroller, analog comparators and digital-analog converters.

Contents

1. Introduction

In this chapter, there will be the introduction of client----NXP Semiconductors N.V. After that, the problem will be analyzed.

1.1 Introduction of the company

NXP Semiconductors N.V. is a company to produce a vast range of product, for example, ARM processors, In-vehicle network, NFC chips and RF chips. In 1980s NXP (Philips) invented the I^2C interface and is still an important supplier of I^2C products. NXP is also the leader of secure connectivity solution for embedded applications such as the secure connected vehicle, end-to-end security & privacy and smart connected solution markets.

It was founded in 1953 by Philips (as part of Philips) and became an independent company in 2006. In 2016 purchased NXP shares, and maybe Qualcomm will take over NXP at the end of 2017. Its headquarter is in Eindhoven, the Netherlands. The company has about 31000 workers in more than 33 countries. (NXP Semiconductors N.V., 2017)

Electronics make up 80% of the innovation cars. And NXP has more than 60 years of automotive experience. It aims to make driving safe and enjoyable, make communication energy efficiency and secure. (NXP Semiconductors N.V., 2017)

1.2 Problem analysis

The company NXP Semiconductors N.V. developed a testbench, which names EVA, to test devices produced by the company. EVA consists of 3 parts: backplane (Fig 1.1), motherboard and daughterboard. In the backplane of EVA, there are some dedicated boards, for example, IO board, ADC board, DAC board and signal generator board (Fig 1.2). And the backplane will work as the interface between the computer and boards via an I2C interface.

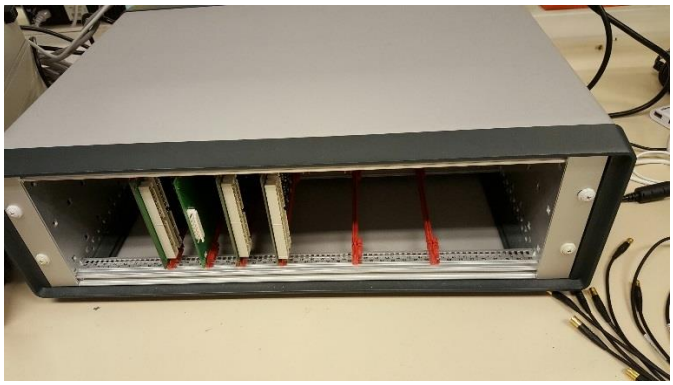


Fig 1.1 Backplane

EVA is used in several branches of NXP, like Shanghai, Kaohsiung, and Bangkok, to analyze the failed devices from the customers, EVA is critical in this analysis.

The failed device will be tested on the EVA to measure customer problems first. Then the failed devices will be opened, and the circuit of the devices will be probed. The reason why a device failed is not always clear. It may be the problem in manufacture like unclean environment, may be the problem on costumers' ESD environment.

The quality of electronic devices used in automotive should be very high, almost comparable to military quality. For example, all devices are designed to be able to work with a wide supply voltage and temperature range from -40°C to 150°C, sometimes to 175°C. Normal consumer electronics (like mobile phones) can work only from 0°C to 85°C. A failed device can cause some problems not only for customers but also for NXP. The return can be sorted into three types.

1. A failed device is detected after the manufacture of the module, production line failure
2. A failed module is detected after the manufacture of the car on which the module is installed, zero km failure
3. The driver find some problems on his car, in which the module is installed, field failure

The final type is the most serious type because it can be dangerous to users of the car and its very harmful to the reputation of the car manufacturer and NXP, so it is very important for NXP to prove to the car manufactures that NXP knows what the problem is, whether it will happen again and how to avoid it if it can happen again, so, analysis and therefor EVA is very important.

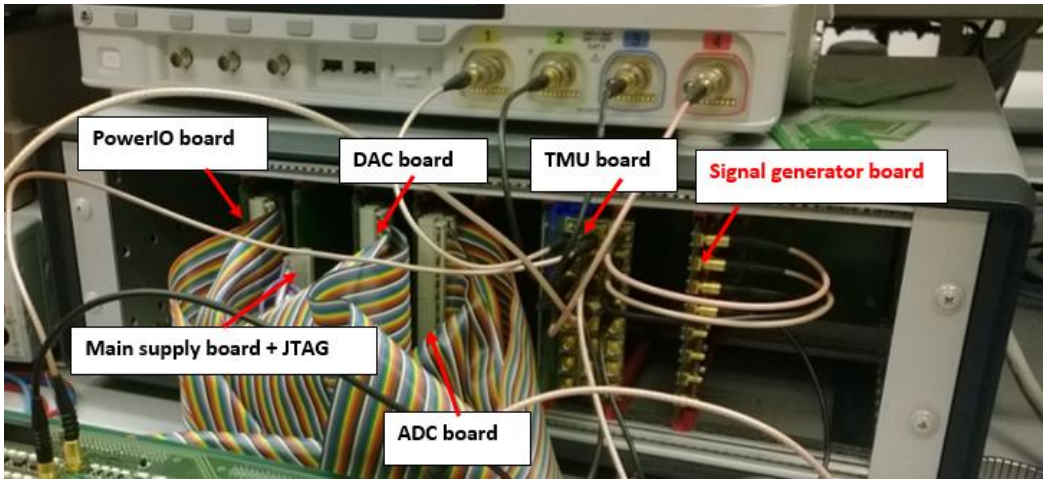


Fig1.2 Backplane and some boards

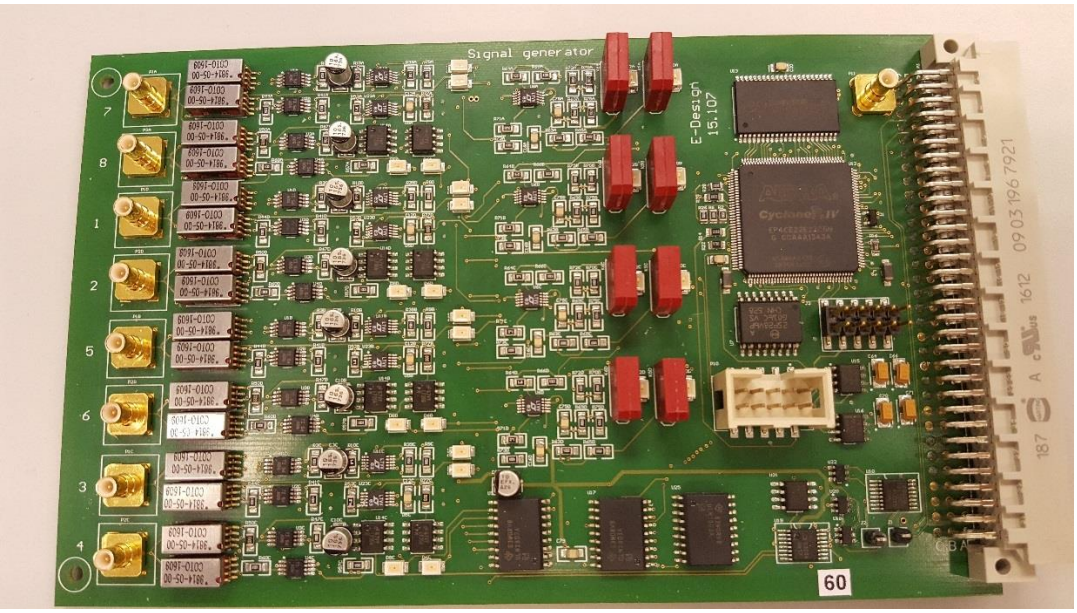


Fig 1.3 Signal generator board

But EVA may also fail. EVA contains a self-test application to test the setup itself. If the self-test is failing, then the engineer should repair the setup. Once a problem happens on, e.g. the signal generator board (see Fig 1.3) then the engineer will replace this board and run the self-test again until it passes. After passing the self-test, EVA can be used again, the replaced board can be repaired later. The signal generator board has some complex circuitry on it. To assist the engineer with his troubleshooting some hardware and software is required. This project will describe the design of a test tool to help the engineer and to fulfill a full automatic signal generator test.

The signal generator has eight output channels, and each channel can produce a square wave with an amplitude of max 10V. The whole board is controlled by an I^2C bus.

This project should be done in NXP Semiconductors in Nijmegen before June 2017.

2. Research questions

In this chapter, there will be the main question of the research. And the main question will be divided into some sub questions. The goal of all the research will be described.

2.1 Main question

What kind of testing tool, which consists of testing board and software, can be used to test the output voltage, frequency and duty cycle of 8-channel signal generator board without the EVA?

2.2 Sub questions

1. What is the detail function of the signal generator board?
2. What is the voltage supply of the signal generator board?
3. What kind of circuit can test the duty cycle of the signal generator board?
4. What kind of circuit can test the frequency of the signal generator?
5. What kind of circuit can test the peak-to-peak voltage of the signal generator?
6. What is the way to exchange data between computer and testing board?
7. What interface can be used to exchange data between components on the testing board?
8. What is the definition of good user interface?

2.3 Research goal

Following the requirements of client, the testing tool should consist of both hardware and computer software. Hardware should be a PCB board which can connect to the computer through USB cable. And the software should be programmed in language Delphi. Finally, a prototype should be built to prove the function of the testing tool.

3. Theoretical framework

In this project, the research is mainly about two aspects: the principles of the testing target and useful technologies for this project. The research is relative to the sub questions. After that, there will be an introduction of some components and technologies which may be used in this project.

3.1 The signal generator board (testing target)

In this chapter, the principle of the signal generator board (testing target) will be introduced. Some components and technologies mentioned in the introduction will be in traduced individually.

3.1.1 Signal generator

The function generator is used to generate simple repetitive waveforms. Normally, it used an analog circuit to generator waveforms, without the digital controller. Early function generators tended to rely on analog oscillator circuits that produced the waveforms directly. Modern function generators may use digital signal processing techniques to generate the waveforms digitally and then convert them from the digital into an analog format.

Many function generators can only generate low-frequency waveform because the requirement is not that high. However, it is possible to apply it in high frequency. (Poole, 2017)

3.1.2 The signal generator board (testing target)

The principle of the target device is different from the common signal generators. It focuses on the square wave. As Fig 2.1 shows, on the generator board, there is a digital- analog- converter, which is used to generate the peak- peak voltage, which is the amplitude of the waveform. FPGA (see 2.1.3) generates a PWM to control the frequency and duty cycle of the square wave. The output of DAC (see 2.1.8) and the PWM from FPGA will go to an operational amplifier, which works as an analog comparator (see 2.1.7), and the output of the operational amplifier will be a square wave ranged from 0V to 5V. The output of the operational amplifier will go to 2 ways; one will double the output, the other will keep the output the same. The FPGA will turn on one way as the final output by turning on the relay. 2 ways will not be open at the same time. The FGPA can receive commands from an I2C bus (see 2.1.5). RAM (see 2.1.4) is used for the storage of FPGA on this board. There is also a JTAG (see 2.1.6) port on the board, and users can program the FPGA through this port.

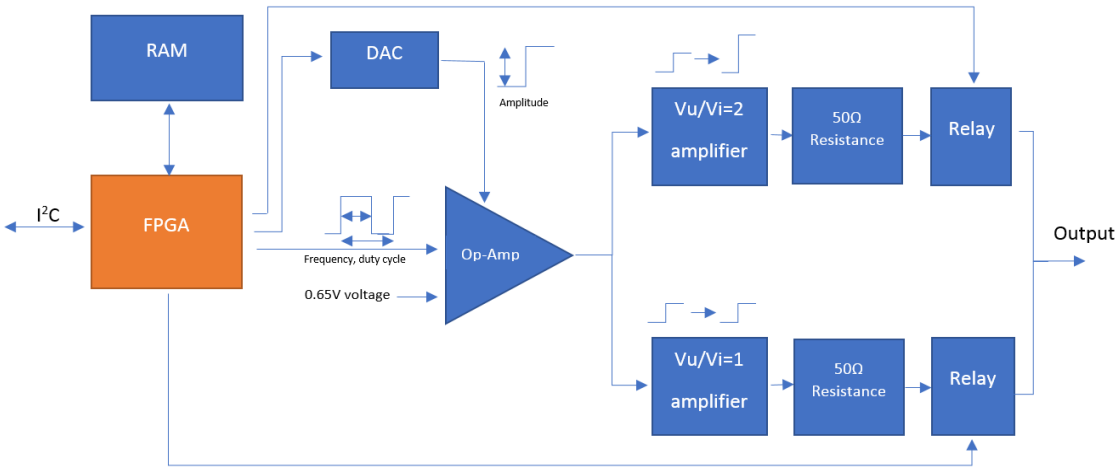


Fig 3.1 structure of a channel of the signal generator board

3.1.3 FPGA Cyclone IV EF4CE22E22C6N

Field Programmable Gate Arrays (FPGAs) are built based on a matrix of configurable logic blocks (CLBs). The configurable logic blocks are connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing. The FPGA will lose the program after power off. (Xilinx Inc, 2017)

FPGA is widely used in building the prototype and small amount production. It is flexible, users can use it to design different kind of circuit. And it is easy to use because users can use integrated circuit hardware description, such as VHDL, to build the circuit.

FPGA is an ideal fit for many different markets because of its programmable nature. As the industry leader, Xilinx provides comprehensive solutions including FPGA devices, advanced software, and configurable, ready-to-use IP cores. Its products are used for markets and applications such as ASIC Prototyping, Aerospace & Defense, Audio, Automotive… (Xilinx Inc, 2017)

Altera's developed a new FPGA device family called Cyclone IV to extends the Cyclone FPGA series leadership in providing the market's lowest-cost, lowest-power FPGAs, now with a transceiver variant. Cyclone IV devices are targeted to high-volume, cost-sensitive applications, enabling system designers to meet increasing bandwidth requirements while lowering costs. It is not a very powerful.(Altera Corporation, 2017)

As Fig 2.1 shows. This FPGA is used in the signal generator as the controller of the output waveforms. Its variables are stored in the RAM, and it can communicate with DAC to control the amplitude of output and output a waveform to the op-amp to control the frequency and duty cycle. It can also control the relays to control whether the output will be doubled.

3.1.4 RAM IS61WV10248BLL

The ISSI IS61WV10248ALL is a kind of high-speed, low power, 1M-word by 8-bit CMOS static RAM. The IS61WV10248ALL is fabricated using ISSI's high-performance CMOS technology. This is an 8M

RAM, in the signal generator, it is used by an FPGA to store variables. (Integrated Silicon Solution, Inc, 2017)

Fig 3.2 RAM IS61WV10248BLL

3.1.5 I^2C bus

The I^2C bus is a widely-used bus used for communication between a master (or multiple masters) and one or more slave devices. But there can be only one master at once time. Fig 3.3 illustrates how many different peripherals may share a bus which is connected to a processor through only two wires. But all the device should use the same ground. I^2C is widely used in the embedded system because the wiring is simple compared with other ways of communication. Most of the microcontroller support I^2C in hardware and its speed can be changed. In this project, I^2C will be used to communicate with signal generator board. And the communication between some components will also use it. In this signal generator, it is used for the communication between FPGA and DAC, FPGA and external device. And it can also be used in this project for the communication between components on the test board. (Texas Instruments, 2017)

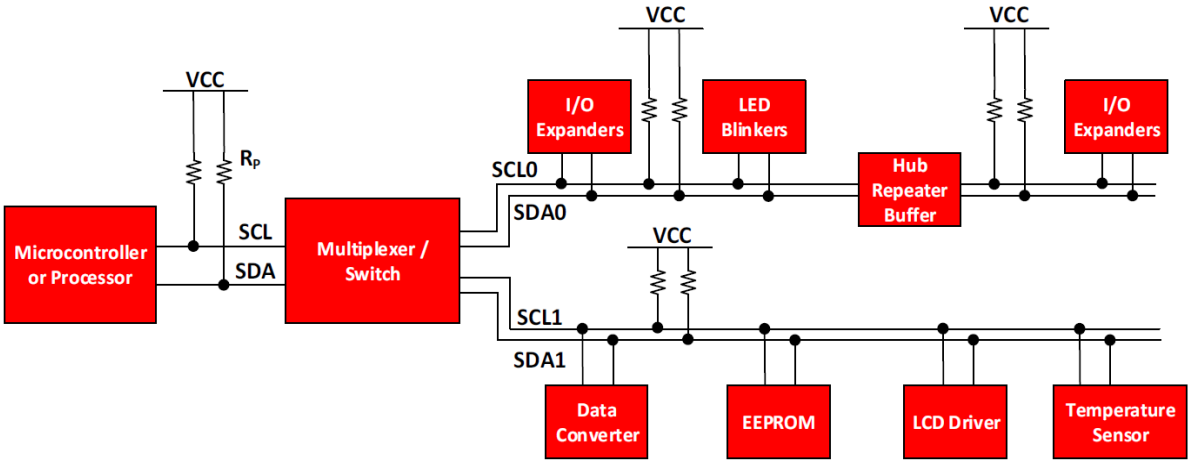


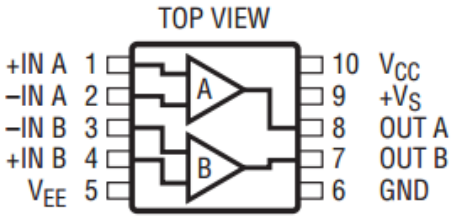
Fig 3.3 example I^2C bus

3.1.6 JTAG

It is developed as an industry standard in 1990. This is a serial bus with four signals: Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI), Test Mode Select (TMS), and Test Data Output (TDO). This bus is usually used in the embedded system to programming flash memory of systems deployed in the field and everything in-between. In this project, JTAG is used for the programming of the FPGA on the signal generator board (testing target). And it is commonly used for the programming of MCU so that it may be used on the test board. (Corelis, 2017)

3.1.7 Analog comparator

LT1715 is a kind of dual comparator with Independent Input/Output Supplies. Its rising time is 4ns, and the input frequency can be 150MHz. If the positive input is a higher voltage than the negative input, the output voltage is equal to Vs. if lower, the output is GND. On the signal generator board, the FPGA controls comparators to output a square waveform. On the test tool, it can be used with DAC to detect the voltage of waveform.



(Linear Technology, 2017)

Fig 3.4 Top view of LT1715

3.1.8 DAC (Digital-to-Analog Converter)

DACs have many applications in direct digital synthesis (DDS) and software defined radio (SDR). Nyquist rate DACs typically convert digital data into analog signals by simply switching and adding data. By toggling the switches according to input data, current or voltage is changed. Although some successful high-speed DACs have been developed, there are still many uses of conventional approaches. MOSFETs or BJTs used as switching devices have severe limits, such as capacitance charging, carrier recombination or transit delay preventing high-speed operation. And now there is a new kind of design for DAC based on microwave circuit principles, which uses Schottky instead of diode samplers. In this project, the output of the DAC, which is an analog signal, can be used as the negative input of a comparator (see Fig 3.5) to check if the positive input is higher than a certain voltage and then get the peak-to-peak voltage of waveform. This method can be used to test the voltage. (Sun & Der Weide, 2006)

Now, there is an existing system in which a DAC is connected to an operational amplifier, and the amplifier can be turned off by a controller. In this system, the output voltage can be controlled by the DAC, and the controller can make the output voltage equal to DAC or high-Z. (Silicon Labs, 2017)

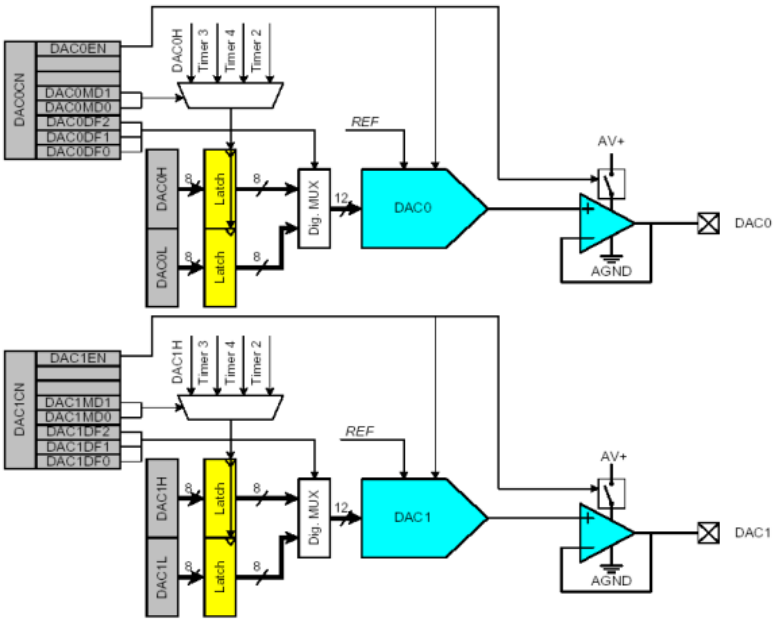


Fig 3.5 An existing system using DAC and amplifier (Silicon Labs, 2017)

3.2 LPC MCU (Microcontroller Unit)

LPC is a series of 32-bit ARM processor developed by NXP Semiconductors. It is widely used in industry. It is famous for its reliability and efficiency. Some of the MCU in this series have the function pin-interrupt, which can be used to detect the change of digital signal. The highest working frequency is from 30MHz to 180Mhz. MCU of this series supports at least one channel of SPI and I^2C interface on hardware. It can also be used to count the time between falling edge and rising edge (about the duty cycle) or count the number of rising edge in a certain time (about the frequency). (NXP Semiconductiors, 2017)

The pin interrupt of MCU can be used to detect the rising edge and falling edge. The edge detection will compare the voltage level with the voltage level in the previous clock cycle. If the logic of two voltage is different, there is a change on the voltage level (an edge). (W.Valvano, 2017)

3.3 SWD (Serial Wire Debug)

It is developed as a 2-pin alternative to a traditional JTAG interface. It provides the interface to debug and trace functionality on processor cores and System on Chip (SoC) devices. There are two pins on the SWD interface (SWCLK and SWDIO). It can make use of the full clock cycle for data transfer, from rising edge to rising edge of the Serial Wire clock. Overlaying SWD over JTAG provides a way for the users to change their ways of debugging without changing their test hardware. Although the Serial Wire Debug is not directly compatible with JTAG, it can be used to connect to prevails JTAG devices, and provide additional benefits (e.g. clock and power isolation) over a direct, daisy-chained JTAG architecture. In this project,

SWD can be used to upload the program to MCU and debug because all LPC MCUs support SWD. (ARM, 2017)

Nowadays, the increasing complexity of embedded system requires a new tool for development, testing and security analysis. SWD can be used for low-level access (In-Circuit-Emulation and On-Chip-Debug) into ARM-Cortex. (Cedro, Kuzia, & Grzanka, 2012)

3.4 555 timer

555 timer is a kind of integrated circuit which is widely used as the timer. It is easy to use, high accuracy and cheap. Now, there are three main operation modes for 555 timer: Monostable, Astable, and Bistable. In the Monostable mode, the 555 timer will generator a one-shot high voltage pulse when getting a low voltage pulse on the input pin. In the astable mode, the timer will generate a square wave. In the bistable mode (or called Schmitt Trigger), the output will be set to high after a high voltage on the input pin. And the output will be reset after a low voltage on the reset pin.

In this project, 555 timer can be used to count a certain time, which may be useful in testing the duty cycle and frequency.

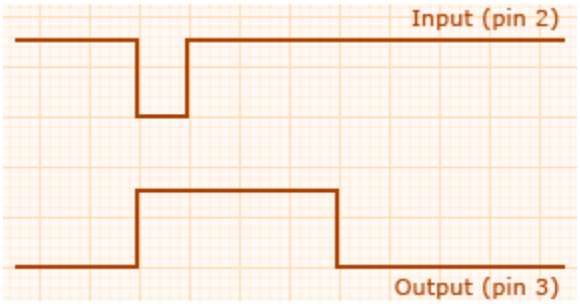


Fig 3.6 Waveform of monostable mode

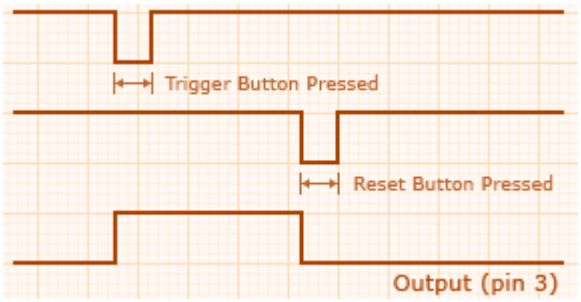


Fig 3.7 Waveform of bistable mode

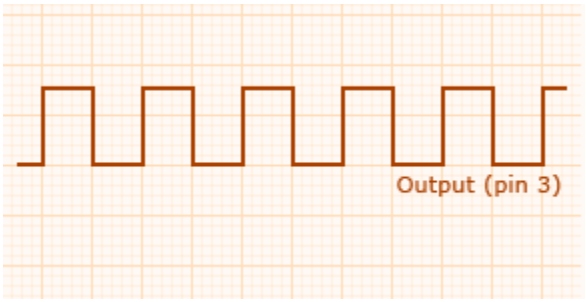


Fig 3.8 Waveform of astable mode

As Fig 3.9 shows. When a negative pulse is given to the trigger input (pin 2) of the Monostable mode 555 Timer oscillators, the internal comparator, (comparator No1) detects this input and “sets” the state of the flip-flop, set the output from a “LOW” state to a “HIGH” state. This action turns “OFF” the discharge transistor connected to the pin 7. Therefore the short circuit across the external timing capacitor is

removed. Time of high voltage (t) can be changed by changing the resistance of R1 and the capacitance of C1. The relation of high-voltage time and R1 C1 can be described by using the formula: t=1.1*R1*C1.(Electronics-tutorials, 2017)

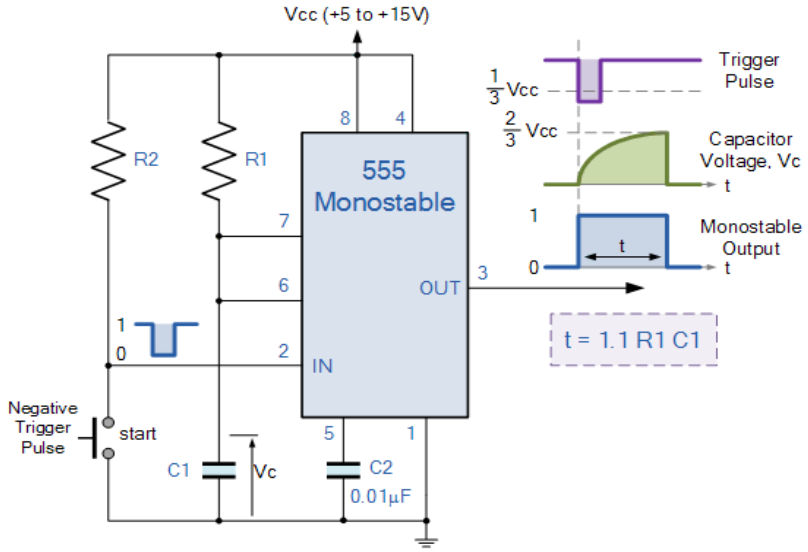


Fig 3.9 Structure and application of monostable 555 timer (Electronics-tutorials, 2017)

3.5 PLL (Phase Locked Loop)

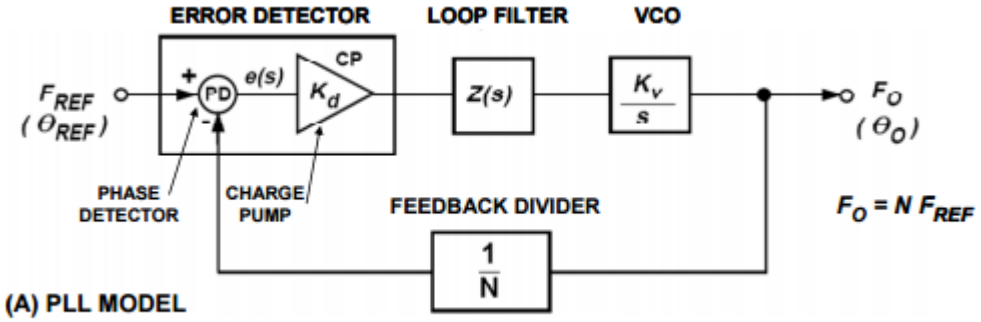


Fig 3.10 model of PLL

A phase-locked loop is a feedback system which can be used to generate a high frequency. It consists of a voltage controlled oscillator (VCO) and a phase comparator. The oscillator maintains a constant phase angle following a reference signal. In this project, in order to make the range of frequency which can be tested larger, a higher frequency may be supplied to the components, so PLL may be useful. (Analog Device, 2017)

3.6 USB (Universal Serial Bus)

USB is a new kind of interconnection standard which is commonly used between personal computers. It allows more than one (up to 127) device to connect. USB is a low-cost, easy solution with a high transfer rate to 12Mbs. USB is usually used for the connection between a computer and more than one peripheral. In this project, USB is useful for the computer to output and input data. (Vijaya, Valupadasu, & RamaRao Chunduri, 2011)

Now, USB-Based Measurement instrument has become more and more popular in the application. In this technology, the USB data can be changed into isolated RS-485 based Synchronous Data Link Control (SDLC) connection. The Measurement system consists of a USB connected Measurement Unit and a laptop computer. The data from the measuring tool can be transferred to the laptop. The transfer rate is normally 2Mbps~10Mbps. (Chen Pei, Liu, & Han, 2009)

3.7 SPI (Serial Peripheral Interface)

Serial Peripheral Interface (SPI) is an interface bus usually used for exchanging data between microcontrollers and other peripherals such as shift registers, sensors, and SD cards. It uses separate clock and data lines, along with a select line to choose the device you wish to talk to. SPI can operate at very high speeds (millions of bytes per second), which may be too fast for some devices. It is possible to use SPI to communicate with more than one device, but there can be only one master at the same time. In this project, SPI may be used for the communication between components on the PCB board.

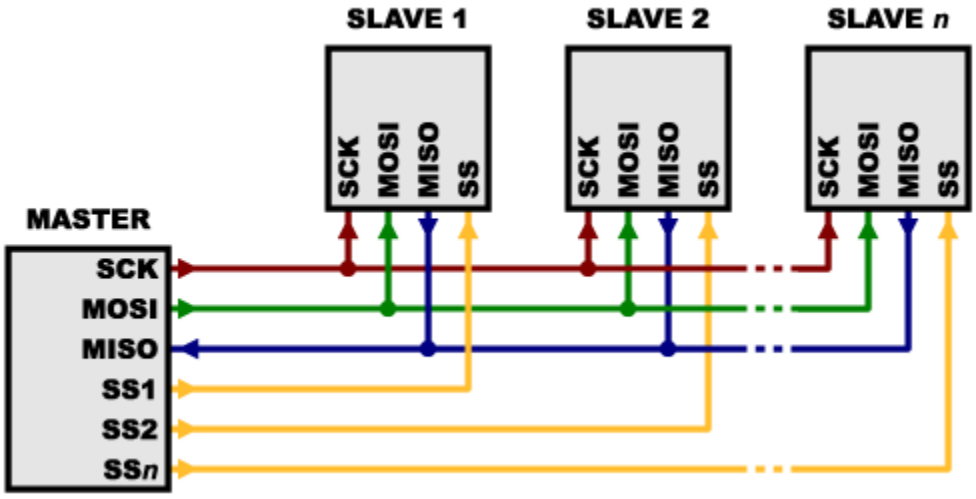


Fig 3.11 structure of SPI (MIKEGRUSIN, 2017)

There exists an existing connection between the S3C2440, which is an ARM9-based 32-bit embedded MCU made by Samsung, and the ADS1274, a high-speed analog-to-digital converter, allowing simultaneous

sampling of four channels made by Texas Instruments. By using fast interruption (FIQ), mass data between high-speed A/D converting and SPI serial interface can be achieved. (Du, He , & Tang, 2009)

3.8 Delphi

Delphi is a very powerful Object Pascal IDE. It is widely used for computer programming on both 32-bit and 64-bit Windows. Now it is also can be used for Android programming, IOS programming, and IoT programming. On NXP, a lot of previous programs and libraries are programmed on Delphi, so it is easier to program on Delphi and it is easier for workers in NXP to maintain the programs in Delphi. (Embarcadero Technologies, Inc., 2017)

3.9 User interface design

User Interface (UI) Design focuses on the possible command of users and what users want to see. It is very important to make UI easy to access, understand, and use to facilitate those actions. There are some important points about how to make a good UI:

1. Keep the interface simple: avoid unnecessary elements and are clear in the language they use on labels and in messaging
2. Create consistency and use common UI elements: components on the different part of a website (or software) should be arranged in the same pattern if possible
3. Be meaningful in page layout: Consider the spatial relationships between items
4. Strategically use color and texture, use the same style in all part of the website (or software)
5. Inform the user with some important information such as actions, changes in state, or errors
6. Think about the defaults, make the defaults value the most common-used value users will use (Usability, 2017)

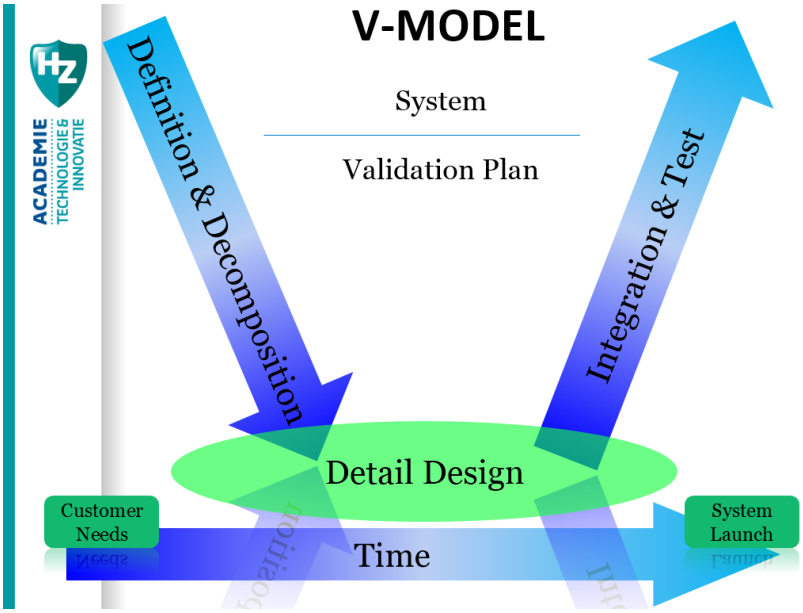
4. Research method

In this project, the V-model will be used. There will be 6 phases in V-model in this project: Project description phase, System design phase, Sub system design phase, Components phase, Sub system building/testing phase, System building/testing phase. All sub questions will be answered in these phases. The activities and deliverables for each phase will be listed.

4.1 Methodology

V- model means Verification and Validation model. Just like the waterfall model, the “V” is a sequential path of execution of processes. Every phase must be finished one by one following the order. The test plans are built with the design of system and sub systems. The V-model is useful for small to medium sized projects where requirements are clearly defined and fixed. The V-model is useful when technical resources are available with needed technical expertise.

(ISTQB Exam Certification, 2017)



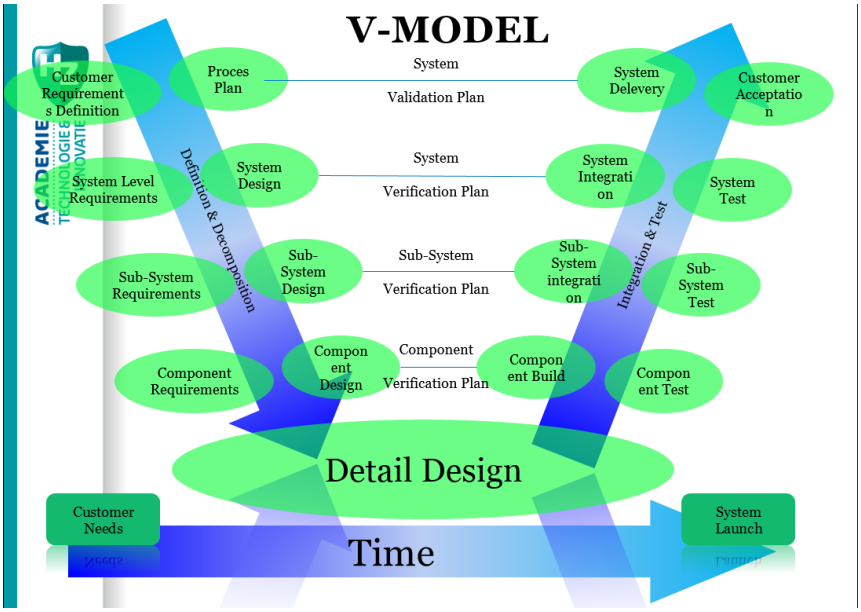


Fig 4.1 Process of V-model

(Verhage & Haak)

4.2 Justification

In this project, V-model will be used, because it is a system design. The hardware part is of some independent functions (for example test voltage, test duty cycle, test frequency), which can be designed and tested independently. The software can also be divided into some sub systems, for example, the GUI can be designed independently. And using V-model in software can make the program easier to maintain. Besides, there are already existing technologies and components which can be used to solve the problem, for example, analog comparator. So, V-model is the best methodology in this project.

4.3 Phases

In this chapter, there are descriptions of each phase. And for each phase, there are specific actions which will be done and deliverables which will be finished at the end of the corresponding phase.

3.3.1 Project description phase

In this phase, the requirements and wishes should be gotten from the client (in-company mentor). And research of the signal generator board and some existing test tools needs to be done. Some necessary knowledge should be gotten to understand the assignment and build the requirements which are specific, measurable, achievable, time- based and realistic.

In this phase, the sub questions 1,2 will be answered.

Action	Deliverables
Communicate with in-company mentor to get the requirements and wishes	Requirements and wishes
Do research on existing test tool	Research proposal
Do research on testing target	
Choose a methodology	
Make a timetable	
Make clear the preconditions and boundaries	

3.3.2 System design phase

In this phase, a clear description of the system should be made, including inputs and outputs of system. After that, a test plan should be made following the description. Finally, the whole system should be divided into some independent sub systems.

Action	Deliverables
Make a description	Description of the system
Make a test plan	Test plan of the system
Divide the system	Some sub systems

3.3.3 Sub system design phase

In this phase, clear descriptions for each sub systems should be made, including inputs and outputs of each sub system. After that, test plans for each sub systems should be built.

Action	Deliverables
Make description	Description of each sub systems
Make test plans for each sub system	Test plan of each sub system

3.3.4 Components phase

In this phase, the design of functions will start. First, the research to choose some existing electrical components. After that, the design of each hardware functions will be finished based on the research. And there should also be some research on the existing program or library. Base on the research of software, some code or some small program will be written to achieve the functions of software.

In this phase, sub questions 8 will be answered.

Action	Deliverables
Choose the components	List of components

3.3.5 Sub system building/testing phase

In this phase, the components from components phase will be combines into some sub systems. The sub systems will be tested following the corresponding test plan. If a sub system fails in the test, it need to be built again or the project will go back to previous phases. After this phase, there will be workable sub systems.

In this phase, sub questions 3,4,5,7 will be answered.

Action	Deliverables
Combine components	Workable sub systems
Do the tests	
	Test reports

3.3.6 System building/testing phase

In this phase, the student will combine the sub systems in to a whole system and test it. If the system fails in the test, it need to be built again or the project will go back to previous phases. After this phase, there will be workable sub systems.

In this phase, sub question 6 will be answered.

Action	Deliverables
Combine sub systems	A workable system
Do the test	
	A test report

5. Result

The result of this project is a test tool consisting of a PCB board and computer software. The hardware uses Digital-to-analog converters, operation amplifiers and analog comparators to process the input waveform and uses a microcontroller to read the processed waveform. Users can control the test and see the result from the computer software.

5.1 Power system

There is only one power supply for the test board----12V. On the test board, the voltage will be transformed into 3.3V, -12V, -5V and 5V to satisfy the command of components on the test board and testing target.

5.1.1 Structure of power system

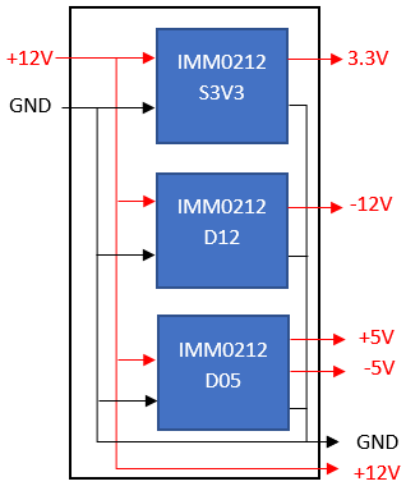


Fig 5.1 power system

Fig 5.1 shows the structure of power supply for the hardware board and testing target. The input voltage should be 12V. Three DC-DC converters will transfer the input voltage into 3.3V, -12V, +5V and -5V.

5.1.2 Demand and supply volume of current

Voltage	Supply volume of current	Demand of current	Detail of demand
3.3V	606mA	27mA	LPC824: 5mA DAC6578SPWR: 2mA Pull-up:20mA
+5V	200mA	5mA	Signal generator board: 5mA
-5V	200mA	20mA	LM2901PW: 10mA*2
-12V	83mA	20mA	Signal generator: 20mA
+12V	Depend on the volume of outer supply	660mA	Signal generator: 600mA LM2901PW: 5mA*2 LM324AM: 50mA*2

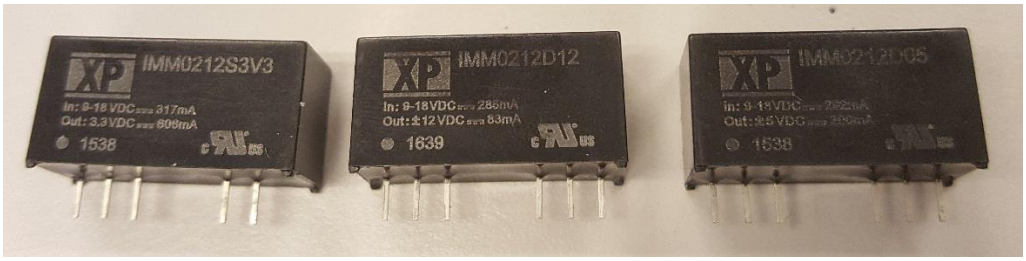


Fig 5.2 IMM0212S3V3, IMM0212D12 and IMM0212D05

Based on the voltage demand and current demand, IMM0212S3V3, IMM0212D12 and IMM0212D05 are chosen to transform the voltage. They can provide enough current and have a long MTBF(1Mh). They are in the same serial IMM02 which is manufactured by XP Power and they have the same footprint and similar parameters. So, it will be easier to maintain it.

5.2 Testing system (duty cycle, frequency, and voltage)

In the beginning, there are duty cycle testing system, frequency testing system and voltage testing system. And finally, they are combined into the testing system. This system is able to test the square waveform and send the data to the communication system. But it cannot judge whether the board works well or not, which will be done on the computer.

5.2.1 Idea of test

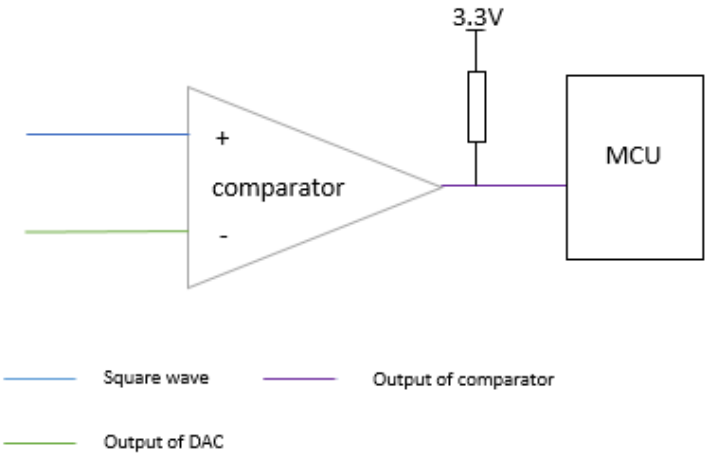


Fig 5.3 Analog comparator

Fig 5.3 shows the wiring of the analog comparator. The positive input is the signal which needs to be tested. The negative input is the voltage generated by DAC. The output of the comparator is shown below.

Situation of inputs	Output
Positive input > Negative input	3.3V
Positive input < Negative input	GND

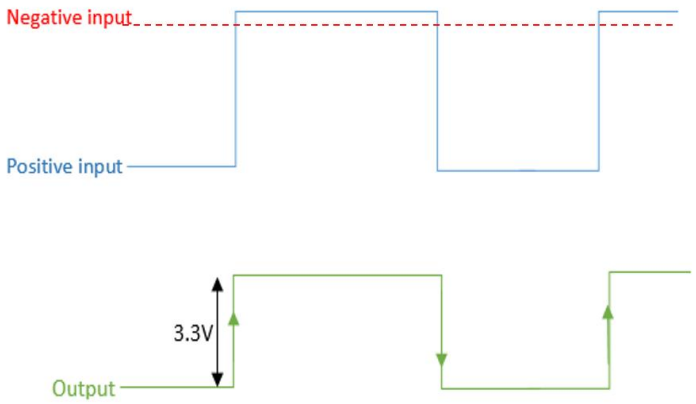


Fig 5.3 Low voltage test of the voltage test

The first step to test the peak-to-peak voltage of a channel is the low voltage test. First, as Fig 5.3 shows, the DAC will make the negative input of comparator a little bit lower than the desired peak-to-peak voltage. And the output should be a square waveform with the peak-to-peak voltage of 3.3V. And the MCU will detect edges.

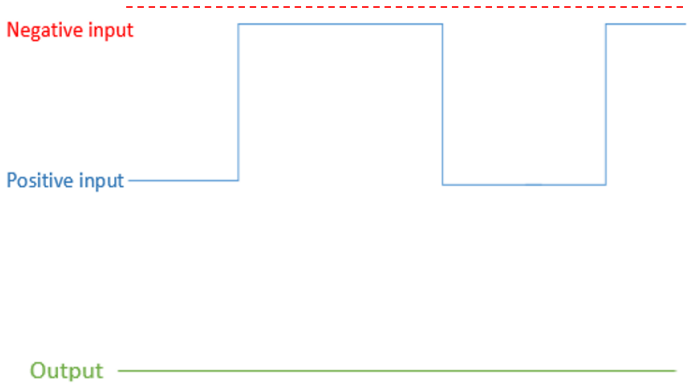


Fig 5.4 High voltage test of the voltage test

If the signal generator board passes the low voltage test, then the second step----high voltage test. As Fig 5.4 shows, DAC will make the negative input a little higher than the desired voltage. At this time, the output should be constant low and MCU cannot detect any edge. If the channel passes both low voltage test and high voltage test, it passes the voltage test.

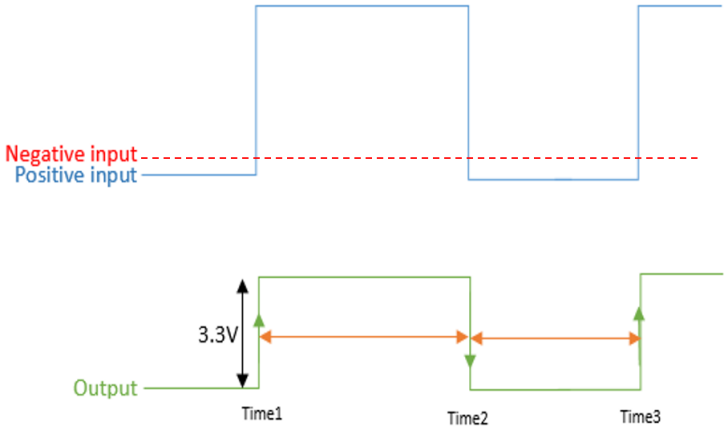


Fig 5.5 Frequency and duty cycle test

As Fig 5.5 shows, to test the frequency and duty cycle, DAC will make the negative input voltage a little higher than the ground. And the output should be a square waveform with the peak-to-peak voltage of 3.3V. And the MCU will detect the edge of the output and store the value of timer on rising edges and falling edge (Time1, Time2, and Time3). The duty cycle can be calculated by using the formula below:

$$d = \frac{Time1 - Time2}{Time1 - Time3} \qquad (4\text{-}1)$$

And the frequency can be calculated by using the formula below:

$$f = \frac{F}{(Time1 - Time3)} \qquad (4\text{-}2)$$

$$f(Hz): frequency\ of\ the\ tested\ waveform$$

$$F(Hz): frequency\ of\ the\ timer\ in\ MCU$$

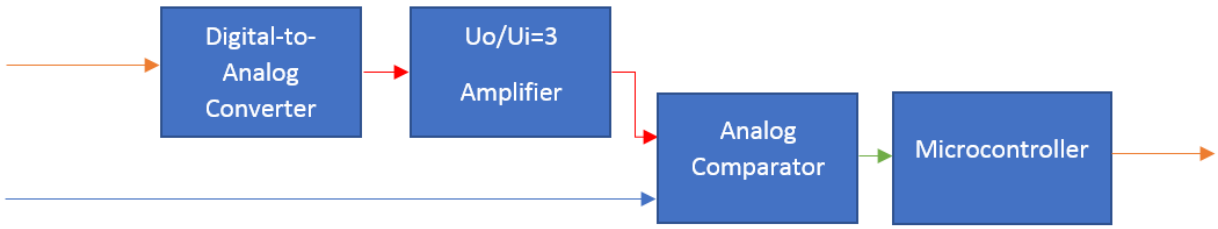


Fig 5.6 Structure of test system

Fig 5.6 shows the structure of the real design: a DAC generate the voltage between 0V and 3.3V. And the amplifier will amplify the voltage to 3 times. The analog comparator will compare the two inputs and output the result of compare to a microcontroller.

5.2.2 Choice of components

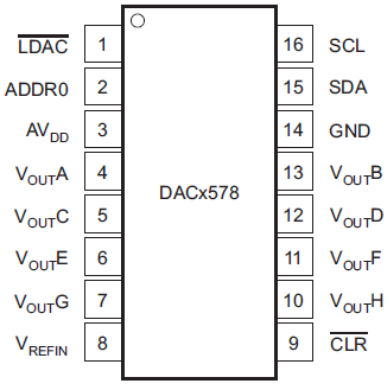


Fig 5.7 the layout of the pins of DAC6578SPW (Texas Instruments, 2017)

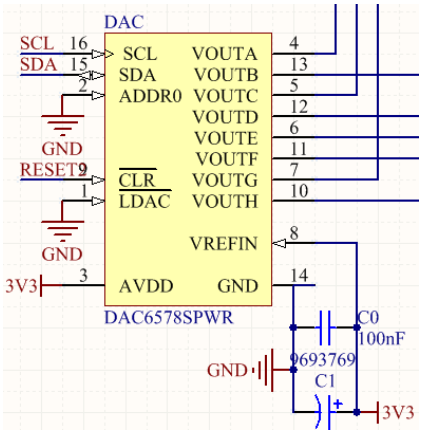


Fig 5.8 Wiring of DAC6578SPW

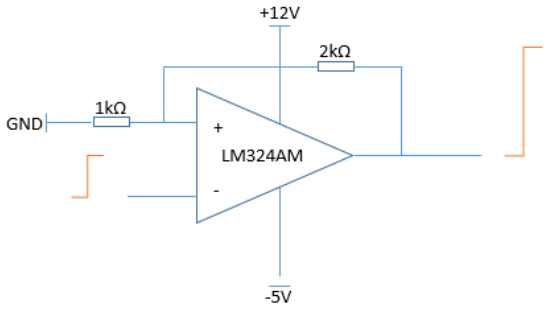


Fig 5.9 Structure of Uo/Ui=3 Amplifier

DAC6578SPW is chosen as the DAC in this system. It is an 8-channel DAC. The I2C interface can control it. In this project, it can generate a voltage from 0V to 3.3V. Fig 1.6 shows the wiring of DAC. The address pin (ADDR0) is connected to ground, so its address is 100100 in binary. LDAC pin is connected to ground, so the voltage will change immediately after sending of data. The reference voltage is 3.3V, and the resolution is 3.223mV. There are two capacitors between VREFIN and GND to make the reference voltage stable.

Fig 5.9 shows the way to amplify the output voltage of DAC to 3 times. LM324AM is a 4-channel Operational amplifier.

5.2.3 Software of microcontroller LPC824

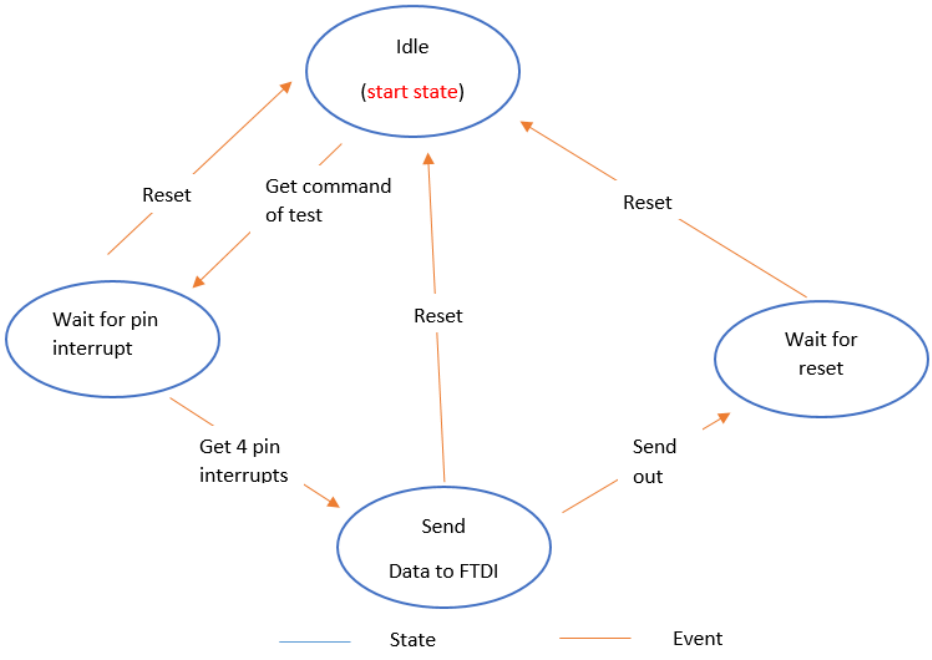


Fig 5.10 Structure of software on LPC824

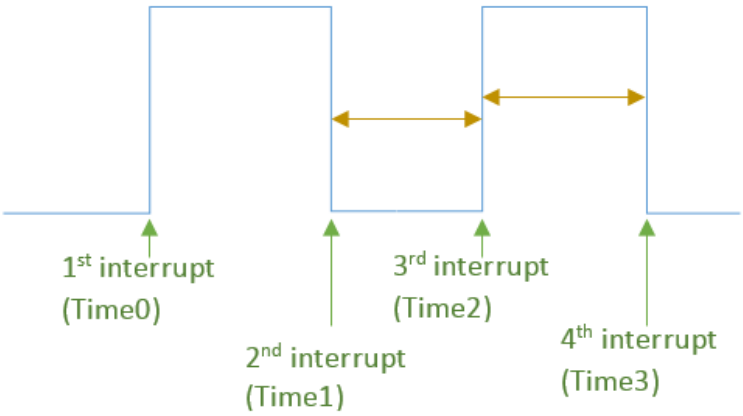


Fig 5.11 Pin interrupt

As the Fig 5.10 shows, the starting state is idle, in which the microcontroller will wait for the command from the computer. After receiving the command, the microcontroller will begin to wait for the pin interrupts on the corresponding pin following the command. As the Fig 5.11 shows, the microcontroller will record the time of every interrupt. After getting 4 pin interrupts, the microcontroller will calculate the time between 2nd interrupt and 3rd interrupt (Time1-Time2) and the time between 3rd interrupt and the 4th interrupt (Time2-Time3). And the controller will send the result of the calculation to the computer. The time between 1st and 2nd interrupts will not be used because it is not accurate sometimes.

If the microcontroller did not receive any pin interrupt, it will continue waiting without sending back anything. Every time, before sending a command to the microcontroller, the computer will reset the microcontroller to make sure the microcontroller is in the idle state (the start state).

5.3 Communication system

In this project, the computer communicates with components on the board and testing target via the FT4232 mini module. The computer can communicate with FT4232 mini module by USB. And the FT4232 can communicate with other components and testing target. Two pins of FT4232 work as reset signal which can reset LPC824 and DAC.

5.3.1 Structure of communication system

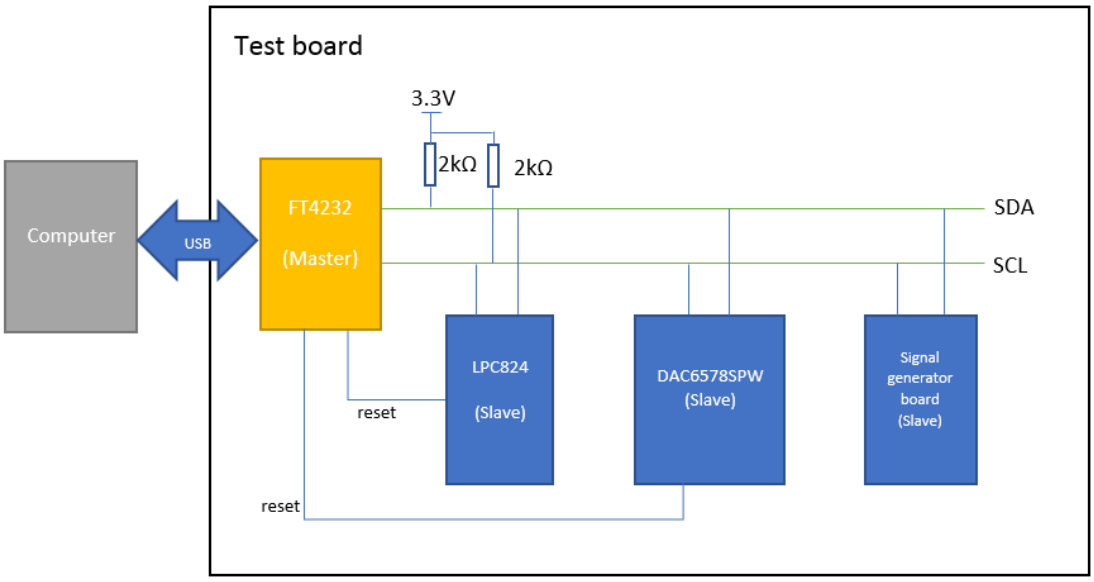


Fig 5.13 Communication system of test tool

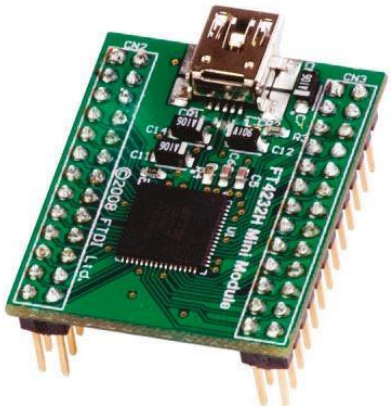


Fig 5.14 FT4232H mini module

Fig 5.13 shows the data transfer of the test tool. The computer will communicate with FT4232 via USB. There is a USB port type-c port on it. And the module can communicate with LPC824, DAC6578SPW and signal generator board via an I^2C interface. The SDA and SCL of the I^2C are pulled up to 3.3V by using resistors of 2kΩ. And two pins of the module are used as GPIO to reset LPC824 and DAC6578SPW.

There are existing drivers and libraries in programming language Delphi for the communication between computer and FT4232.

5.3.2 Format of data from the master to the slaves

In the bit 0: LSB bit7: MSB

the format of sending commands to LPC824 is below:

Byte 0 (from master)	Byte 1 (from master)	Byte 2 (from master)	
bit 7: bit0	bit 7: bit 0	bit7: bit 4	bit3: bit 0

0010 0010	Reserved	Channel number

There are 8 channels of output on the testing target and only one channel can be tested at one time. The channel number is the channel to be tested.

The format of sending commands to DAC6578SPW to change the output voltage is below:

Byte 0 (from master)	Byte 1 (from master)		Byte 2 (from master)		Byte 3 (from master)
bit 7: bit0	bit 7: bit 4	bit 3: bit 0	bit 7: bit 2	bit 1: bit 0	bit 7: bit 0
1001 0000	0000	Channel n	Reserved	Output voltage	

Channel n is the number of the channel whose voltage will be changed. Channel n can be from 0000 to 1111 in binary, which means channel A to channel H. The Output voltage is a 10-bit binary number, which will change the voltage of channel n. The relation between Output voltage and the real voltage is given below:

$$Real\ voltage(V) = \frac{3.3V * Output\ voltage}{1023} \qquad (4\text{-}3)$$

There are exiting program library for the communication between computer and testing target via FT4232.

5.3.3 Format of data from the slaves to the master

bit 0: LSB bit7: MSB

the format of data from LPC824 is below:

Byte 0 (from master)	Byte 1 (from slave)		Byte 2 (from slave)		Byte 3 (from slave)		Byte 4 (from slave)		Byte 5 (from slave)	
bit 7: bit0	bit 7	bit 7: bit0	bit 7	bit 7: bit0	bit 7	bit 7: bit0	bit 7	bit 7: bit0	bit 7	bit 6: bit0
0010 0011	0	Data 1	0	Data 2	0	Data 3	0	Data4	0	Data 5

On the LPC824, the result of calculation is a 60-bit, but only the last 35 bits are useful is the testing frequency is above 1Hz. In this project, the result will be sent 7 bits by 7 bits. Data 1 is highest and Data 5 is lowest.

5.4 Computer software system

The software is written in programming language Delphi. In this program, 3 existing libraries are used: D2XXUnit.pas, DSI2C.pas, and Frequency_Generator.pas. D2XXUnit.pas, DSI2C.pas are developed by the manufacturer of the FT4232 module to control the module to work in the I2C interface. Frequency_Generator.pas is developed by the client NXP.

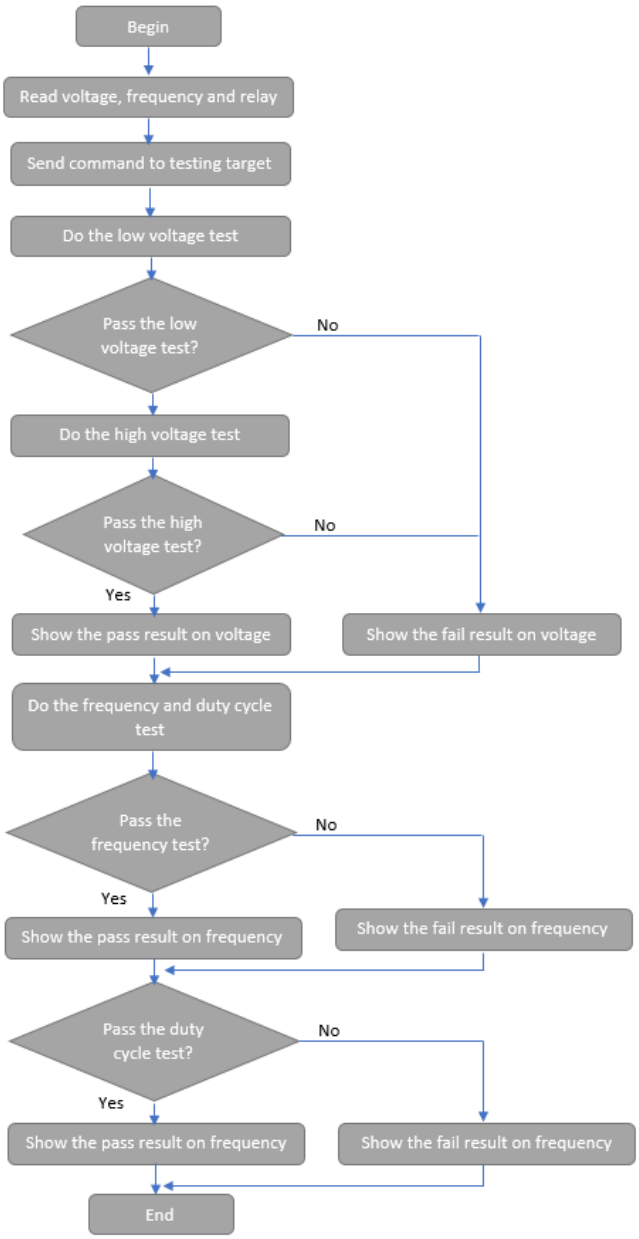


Fig 5.15 Test of a channel

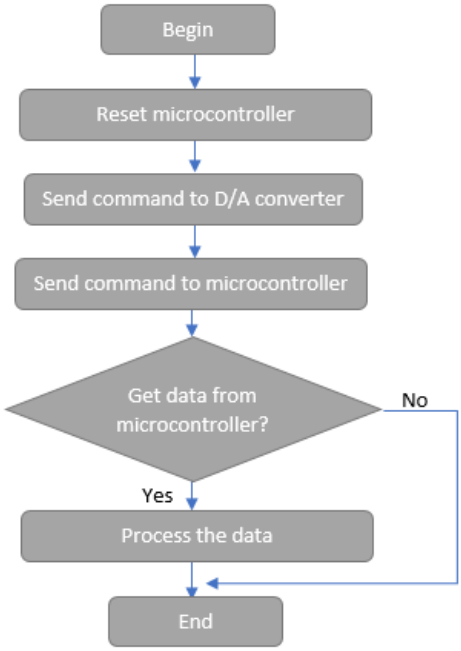


Fig 5.16 Process of a test

Fig 5.15 is the flow chart of the test for each channel and Fig 5.16 is the flow chart for each test. First, the computer will read the test voltage, test frequency and the channel of the relay from the user interface. After that, the command will be sent to the testing target. The first test is the low voltage test, in this test, the computer should get the time of interrupt from PCB board. If the channel of the testing target passes the low voltage test, then it will be tested in the high voltage test. The channel of the testing target, which passes both low voltage and high voltage test, passes the voltage test.

After the voltage test, the software will do the frequency and duty cycle test and check the test result.

For each test, the computer will reset the microcontroller and send commands to D/A converter and microcontroller. After that, if the computer gets the data from the microcontroller, it will process the data. If not, it will end the test after waiting for about half a second.

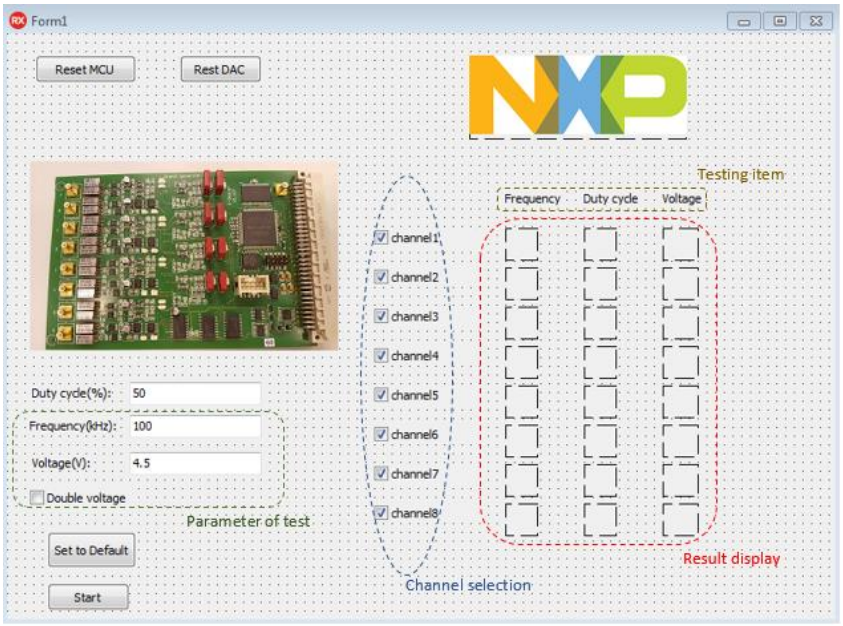


Fig 5.17 Graphic user interface

Fig 5.17 shows the graphic user interface, users can do the test and see the test result through it. On the left part is the parameters of the test. The user can change the frequency and voltage of test, but the number of frequency should be from 1Hz to 300kHz and voltage from 2V to 4.5V. If the checkbox Double voltage is checked, the output channel will be changed to 2-time amplifier channel, and the real testing voltage will be two times of the editbox (see 2.1.2). The editbox “Duty cycle” is read only.

On the middle part, users can choose the channels they want to test; all channels are chosen by default. There are three testing items, and the result will be shown on the red rectangular: green tick means the corresponding item of the corresponding channel works well, the red cross means malfunction.

Clicking the “Start” button will start the test and clicking “Set to Default” button will set all the parameters of the test and channel selection to default.

5.5 Hardware system

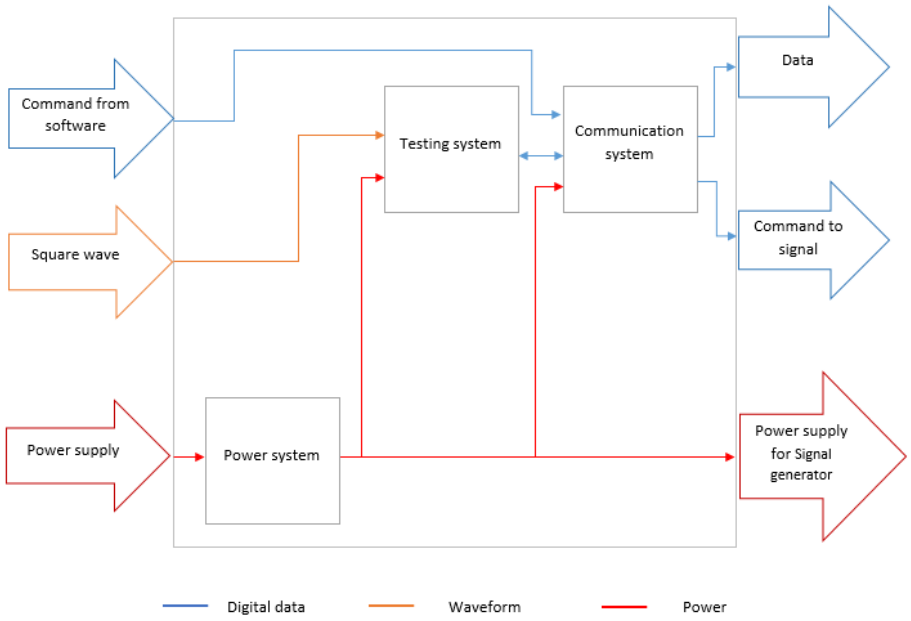


Fig 5.18 Hardware system

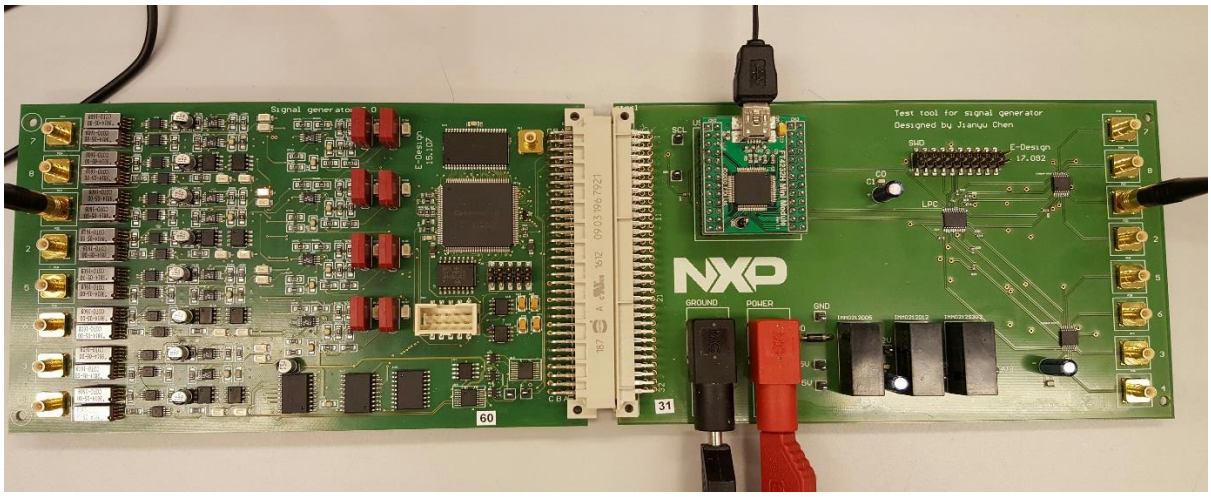


Fig 5.19 Testing target (left) and test board (right)

Fig 5.18 shows the structure of test board. The power system transforms the input voltage to different kinds of voltage for testing system, communication system and the testing target. The communication system exchanges data between the computer, the testing system and the testing target.

The right board in Fig 5.19 is the final testing board, it can connect with testing target via DIN 96 port.

6 Discussion

In this project, there are more than one ways to do the test. For example, 555 timer and counter can be used to test the frequency and integrator can be used to test the voltage and duty cycle. The most important reason for choosing the final testing way is that it can test frequency, voltage and duty cycle by using the same components so that the structure will be simple and the cost will be low. On the other hand, this testing way can test the board accurately.

There are also more than one solutions for the communication between test board and computer. For example, Bluetooth, SPI or UART. And some microcontrollers have the USB port so they can communicate with the computer via USB directly. The FT4232H module is used because it can transform USB to I2C and GPIO at the same time. I2C is necessary for this project because it is the interface for the testing target. What is more, this module is often used in the company, they have a lot of experience of using it and existing library to control it, so it is easier to design and maintain.

In this design, the clock of the timer is the internal clock of microcontroller, to improve the accuracy of testing frequency and duty cycle, a more accurate external clock can be used. The maximum testing frequency is 300kHz. In order to test the voltage of higher frequency, a comparator of higher speed and MCU of higher speed can be used. In order to increase the testing speed, the software on computer and MCU can be modified to test more than one channels at the same time (it is possible in theory).

7 Conclusions and recommendations

After working for a semester, a test tool is built. The hardware of the test tool is a board which uses Digital-to-Analog converters, operation amplifiers, and analog comparators to process the square waveform. The output of the process will be a square waveform of 3.3V peak voltage or a constant low signal. The output of the process can be read by a microcontroller LPC824. The computer software is written by programming language Delphi; users can control the test and see the test result on the software. The computer and the hardware should be connected by an USB cable. It can test all eight channels one by one.

The test tool can be used to test the voltage (with the deviation of ±0.3V), duty cycle (with the deviation of ±1%) and frequency (with the deviation of ±1%) of all eight channels. It can test the frequency from 1Hz to 300kHz and voltage from 2V to 9V. Users can use a computer to control the test tool and get the test result through a graphic user interface.

There are some recommendations for the client: The 12V power supply of this board, which may influent the accuracy of the test, had better be stable. From the test, 1A is enough for the normal use, but the current requirements for the starting will be higher. So, a power supply of 2A output current is recommended. In the test, the computer software is run on the computer with 64-bit Windows 7 Enterprise SP1 operating system, this operating system is recommended. The test board is sensitive to static electricity, so it is recommended to use the test tool in ESD (Electro-Static Discharge) environments.

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Appendix I Schematics and PCB

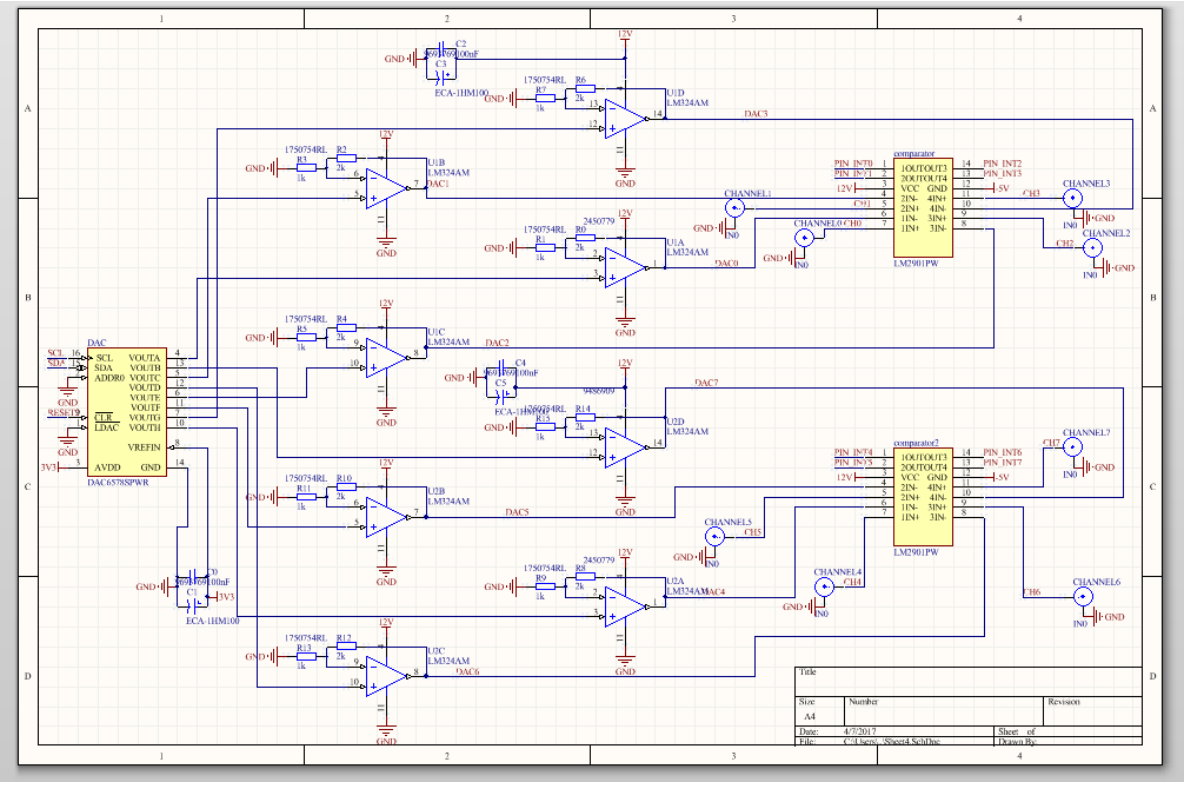

Fig 4 Schematics

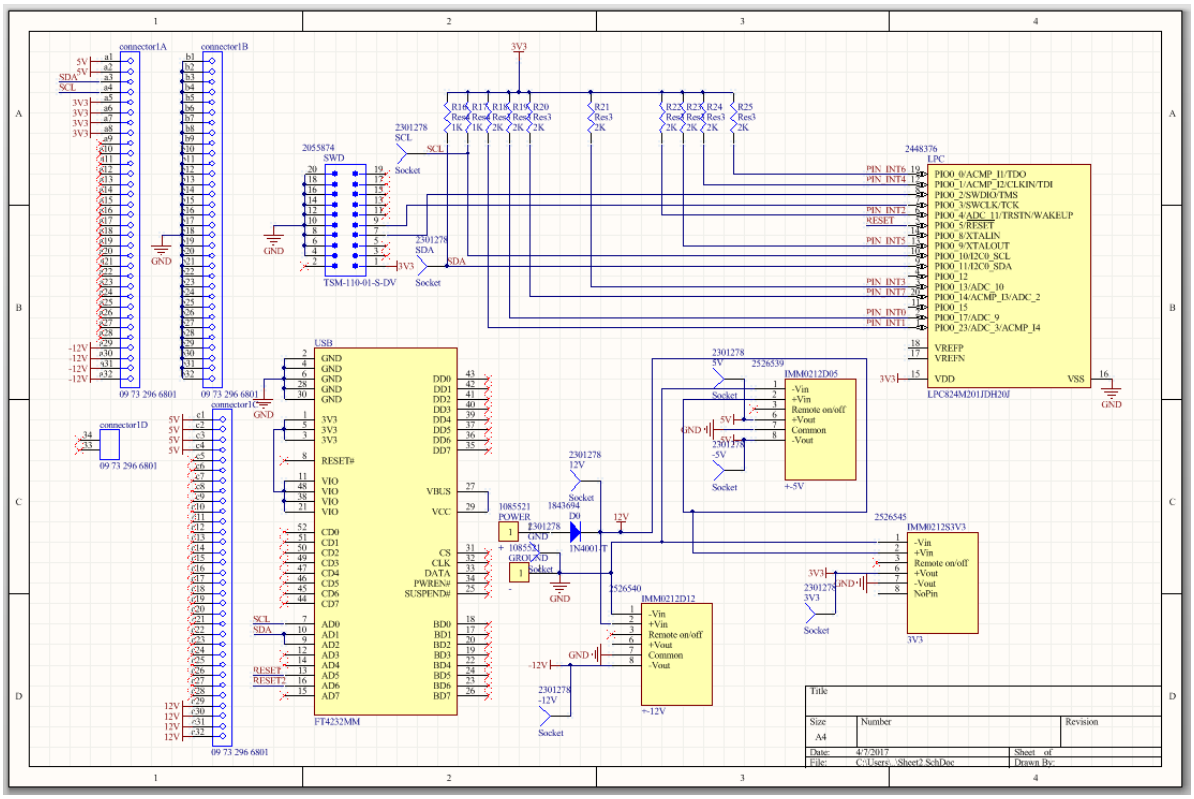

Fig 5 Schematics

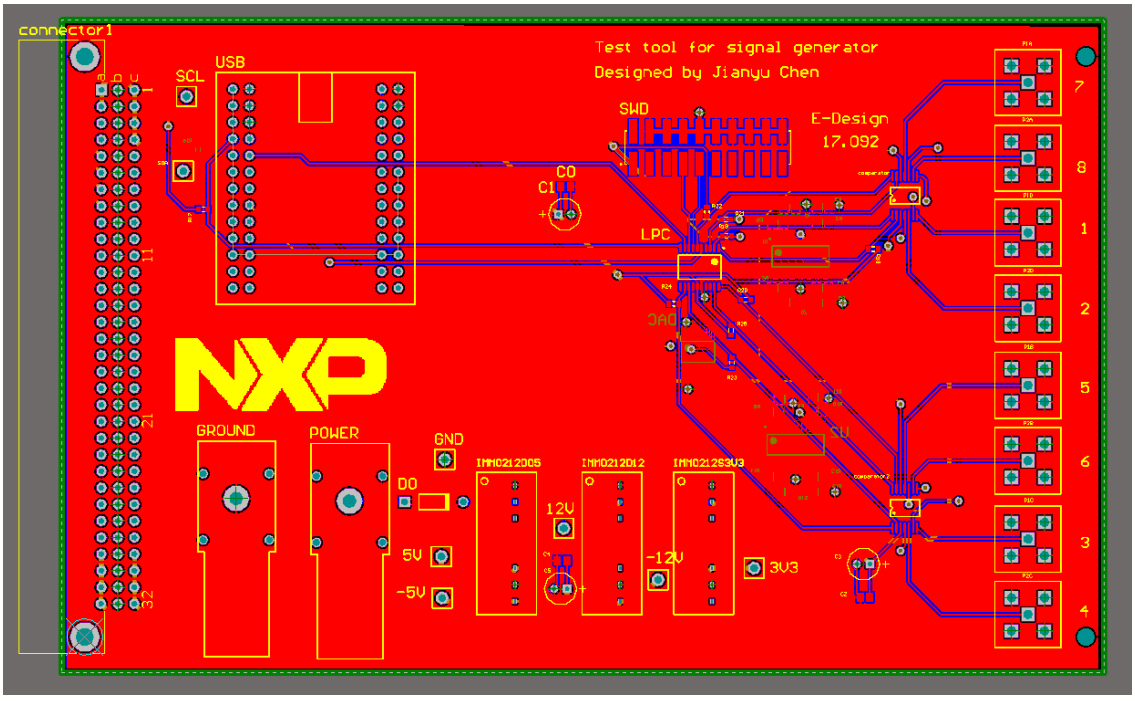

Fig 6 Design of PCB

Appendix II Test plan

1. Test plan of system

1. Aim

The aim of this test plan is to make sure that the testing tool can test the signal generator board.

2. Functionality to be tested

The student will use the testing tool to test the function of changing voltage, changing duty cycle, changing frequency for a signal generator board.

3. Hypotheses

The testing board can test the function of changing voltage, changing duty cycle, changing frequency for a signal generator board.

4. Actual actions during the test

The operator connects the PCB board to a computer.

The operator opened the testing software.

The operator connects the signal generator to the testing board.

The operator starts the software.

The operator change the voltage to 3V, duty cycle to 30% frequency to 10kHz and start test.

The operator makes the note of the result shown on the screen.

The operator change the voltage to 6V, duty cycle to 70% frequency to 1kHz and start test.

The operator makes the note of the result shown on the screen.

5. Predicted conclusion

The testing tool shows the correct data of voltage

The testing tool shows the wrong data of voltage

The testing tool shows the correct data of voltage but shows the wrong test result of voltage (shows the testing target generate wrong voltage)

The testing tool shows the correct data of duty cycle

The testing tool shows the wrong data of duty cycle

The testing tool shows the correct data of duty cycle but shows the wrong test result of duty cycle (shows the testing target generate wrong duty cycle)

The testing tool shows the correct data of frequency

The testing tool shows the wrong data of frequency

The testing tool shows the correct data of frequency but shows the wrong test result of frequency (shows the testing target generate wrong frequency)

2. Test plan of computer software system

1. Aim

The aim of this test plan is to make sure that the software works well.

2. Functionality to be tested

The student will use the software to send command to hardware, get some data from test board analyze the data and show correct result.

3. Hypotheses

The software can send command to hardware, get some data from test board analyze the data and show correct result.

4. Actual actions during the test

The operator connects the FT4232 module to computer and connect a LPC824 microcontroller to the FT4232 module.

The operator opened the testing software.

The operator connects the oscilloscope to the output of FT4232.

The operator flash the MCU which will return a data of correct voltage, duty cycle 50% and frequency 10kHz.

The operator change the voltage to 3V, frequency to 10kHz on the software and start test (simulate the behavior of well working signal generator board).

Read the data sent from FT4232 on oscilloscope.

5. Predicted conclusion

The software can send the data out correctly.

The software cannot send the data out correctly.

The software can get the correct data of voltage

The software cannot show the correct data of voltage

The software can show the correct data of voltage but cannot show the correct test result of voltage (shows the testing target generate wrong voltage)

The software can get the correct duty cycle

The software cannot show the correct data of duty cycle

The software can show the correct data of duty cycle but cannot show the correct test result of duty cycle (shows the testing target generate wrong duty cycle)

The software can get the correct data of frequency

The software cannot show the correct data of frequency

The software can show the correct data of voltage but cannot show the correct test result of frequency (shows the testing target generate wrong frequency)

3. Test plan of hardware system

1. Aim

The aim of this test plan is to make sure that the test board works well.

2. Functionality to be tested

The student will use the test board to get the information of square waveform.

3. Hypotheses

The hardware system can get the command from computer, do the test and send the data back.

4. Actual actions during the test

The operator connects the test board to the computer.

The operator plugs the testing target to the test board.

The operator opened the testing software which can be used to send command to board and get data back.

The operator connects the oscilloscope to the output of signal generator board.

The operator starts the program.

The operator checks whether the waveform is correct or not.

Operator check whether the test board returns the correct data.

5. Predicted conclusion

The test board can control the testing target correctly.

The test board cannot control the testing target correctly.

The test board can return the correct data.

The test board cannot return the correct data.

4. Test plan of frequency testing system

1. Aim

The aim of this test plan is to make sure that the frequency testing system can test the frequency and return correct test result.

2. Functionality to be tested

The student will use the frequency testing system to get the data of frequency of square waveform.

3. Hypotheses

The frequency testing system can send the correct data of the frequency of the square waveform.

4. Actual actions during the test

The operator connects the FT4232 module to computer and connect a LPC824 microcontroller to the FT4232 module.

The operator connected the power supply to the frequency testing system.

The operator opened the frequency testing software.

Turn on the oscilloscope and connect the oscilloscope to the SDA and SCL of I^2C

The operator connects the oscilloscope to the output of FT4232.

Check if the frequency testing system give the acknowledge to the data from FT4232.

Record the data sent from FT4232 on oscilloscope.

5. Predicted conclusion

The frequency testing system can receive the command from software correctly.

The frequency testing system cannot receive the command from software correctly.

The frequency testing system can return correct data.

The frequency testing system cannot return correct data.

5. Test plan of duty cycle testing system

1. Aim

The aim of this test plan is to make sure that the duty cycle testing system can test the duty cycle and return correct test result.

2. Functionality to be tested

The student will use the duty cycle testing system to get the data of duty cycle of square waveform.

3. Hypotheses

The duty cycle testing system can send the correct data of the duty cycle of the square waveform.

4. Actual actions during the test

The operator connects the FT4232 module to computer and connect a LPC824 microcontroller to the FT4232 module.

The operator connected the power supply to the duty cycle testing system.

The operator opened the duty cycle testing software.

Turn on the oscilloscope and connect the oscilloscope to the SDA and SCL of I^2C

The operator connects the oscilloscope to the output of FT4232.

Check if the duty cycle testing system give the acknowledge to the data from FT4232.

Record the data sent from FT4232 on oscilloscope.

5. Predicted conclusion

The duty cycle testing system can receive the command from software correctly.

The duty cycle testing system cannot receive the command from software correctly.

The duty cycle testing system can return correct data.

The duty cycle testing system cannot return correct data.

6. Test plan of voltage testing system

1. Aim

The aim of this test plan is to make sure that the voltage testing system can test the voltage and return correct test result.

2. Functionality to be tested

The student will use the voltage testing system to get the data of voltage of square waveform.

3. Hypotheses

The voltage testing system can send the correct data of the voltage of the square waveform.

4. Actual actions during the test

The operator connects the FT4232 module to computer and connect a LPC824 microcontroller to the FT4232 module.

The operator connected the power supply to the voltage testing system.

The operator opened the voltage testing software.

Turn on the oscilloscope and connect the oscilloscope to the SDA and SCL of I^2C

The operator connects the oscilloscope to the output of FT4232.

Check if the voltage testing system give the acknowledge to the data from FT4232.

Record the data sent from FT4232 on oscilloscope.

5. Predicted conclusion

The voltage testing system can receive the command from software correctly.

The voltage testing system cannot receive the command from software correctly.

The voltage testing system can return correct data.

The voltage testing system cannot return correct data

Appendix III User manual

Fig 7 Ulink2 programmer

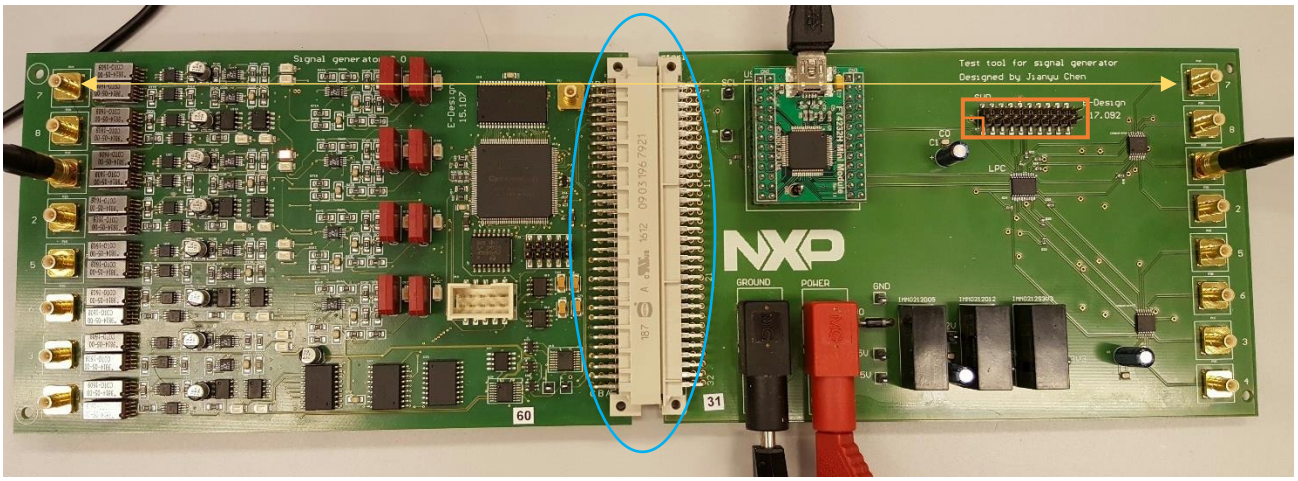

Fig 8 Testing target and test board

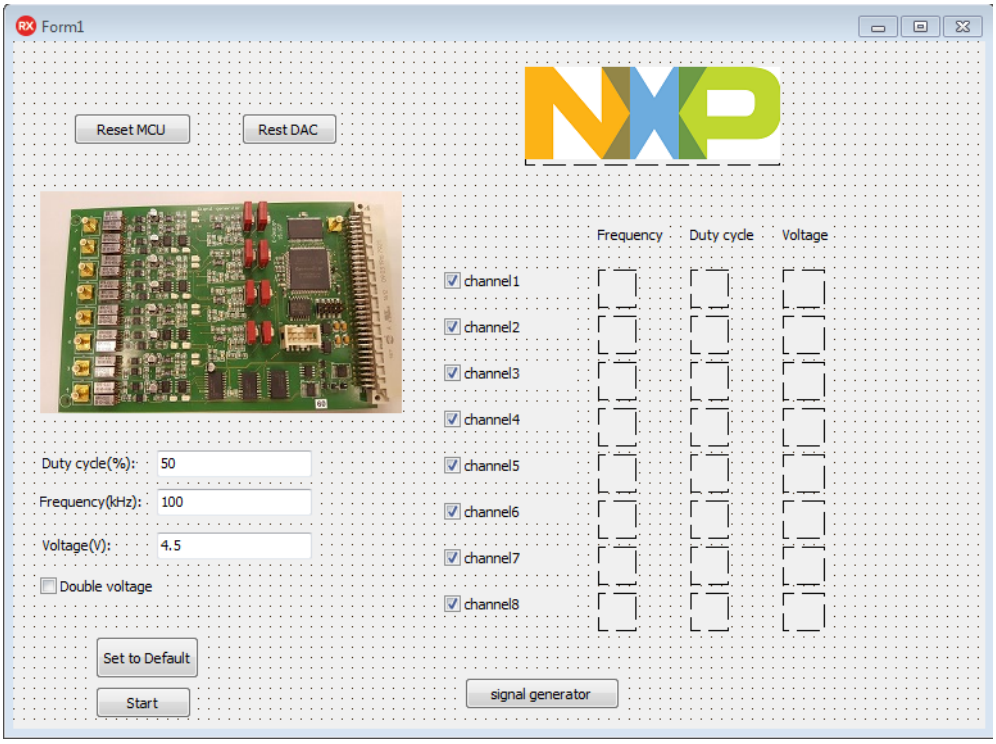

Fig 9 Graphic user interface

Before the first time of using it, the LPC824 should be programmed as below:

1. Connect the SWD programming port (the orange rectangular) on ULINK2 and test board.
2. Use the software Keil uVision5 to open the program LPC_final.c
3. Upload the program
4. Disconnect the SWD programming port

After that, the procedure of the test is below:

1. Connect the DIN96 port (the blue oval) on testing target and test board
2. Connect the USB port on the computer and test tool
3. Connect POWER and GROUND ports to a 12V power supply
4. Connect the high-speed signal port on the testing target and test board as the orange arrow shows (it is not necessary to connect all high-speed port, users can only connect the ports they want to test)
5. Turn on the power
6. Open the computer program test_tool
7. Choose the frequency, voltage and channels of testing
8. Click the start button
9. Wait for some seconds and see the testing result