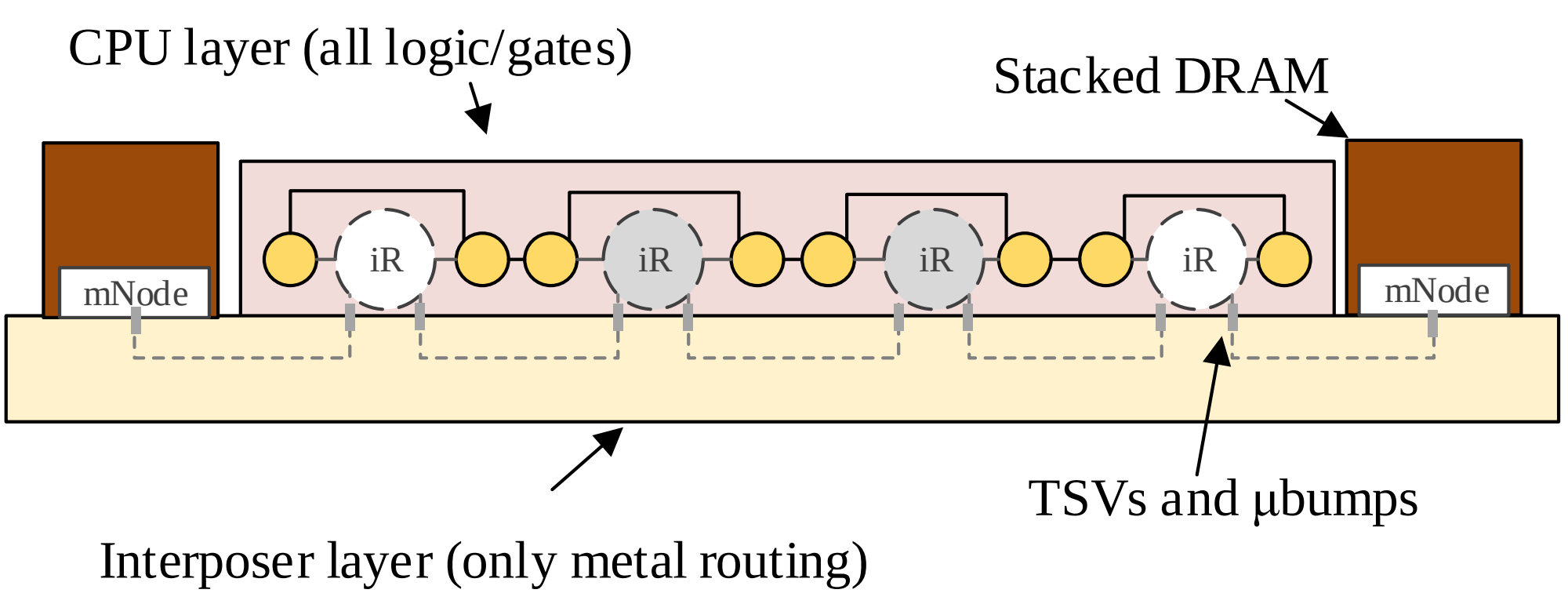
CPU layer (all logic/gates)
Stacked DRAM
iR
iR
iR
iR
mNode
mNode
TSVs and μbumps
Interposer layer (only metal routing)