

EECS 2070 02 Fall 2021

# Clock Domains and Handshaking

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Lecture 16

# 聲明

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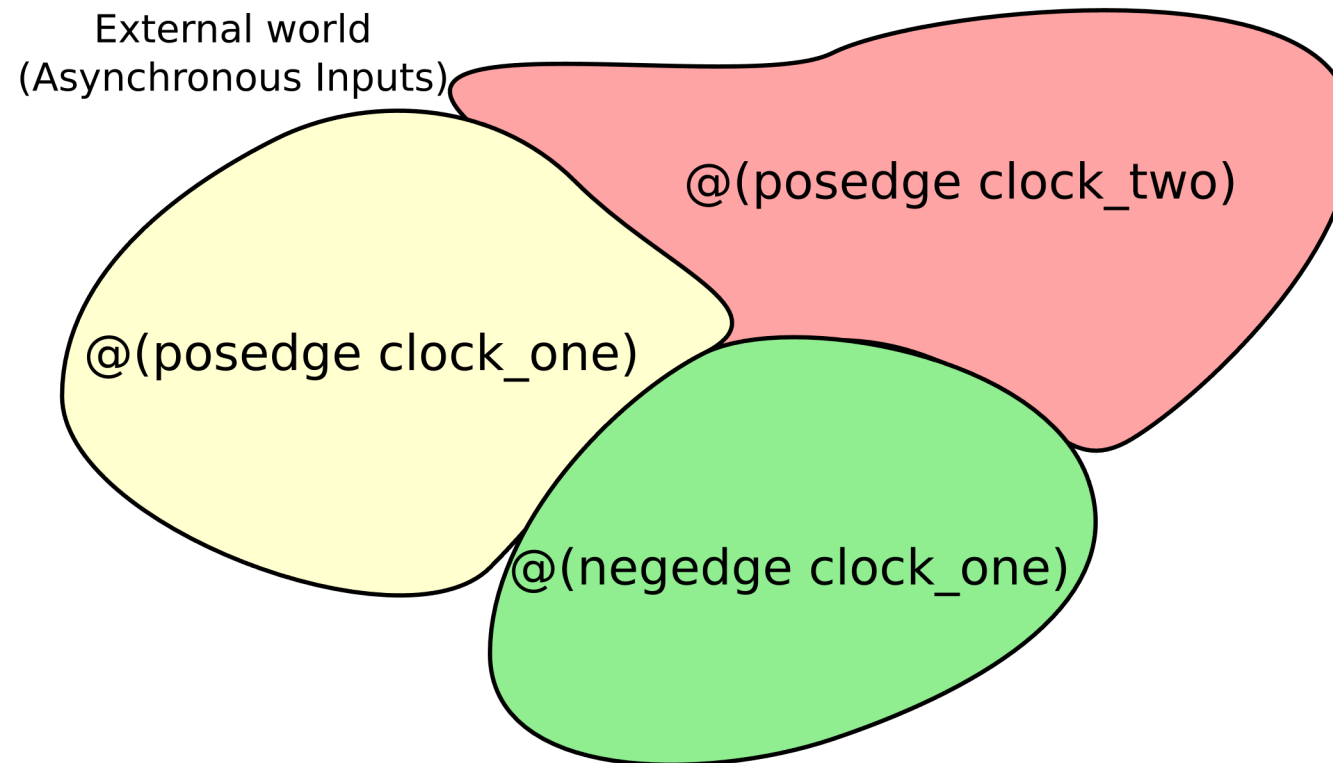
# Outline

- ⦿ Clock-Domain Crossing (CDC)
- ⦿ Handshaking

# Clock-Domain Crossing (CDC)

# Multiple Clock Domains

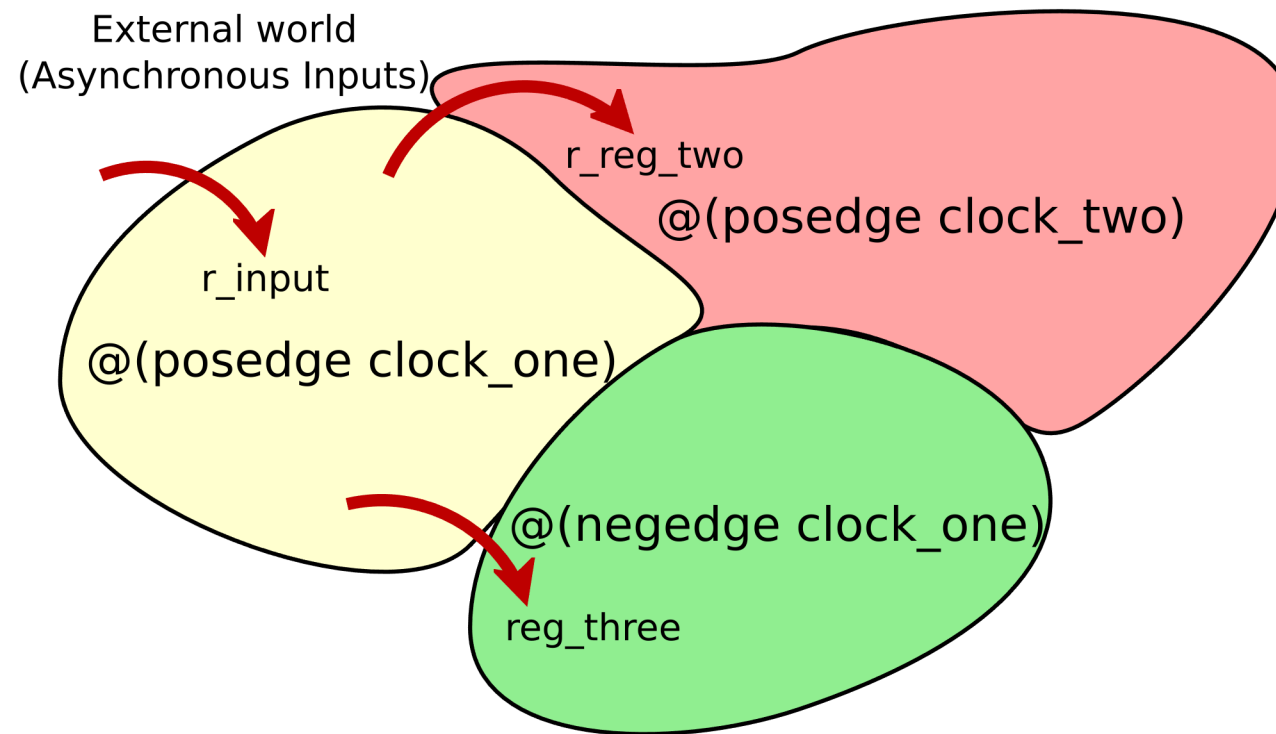
- ⦿ A “**Clock Domain**” is the portion of design that is triggered and synchronized by a single clock



Src: <https://zipcpu.com/blog/2017/10/20/cdc.html>

# Clock-Domain Crossing (CDC)

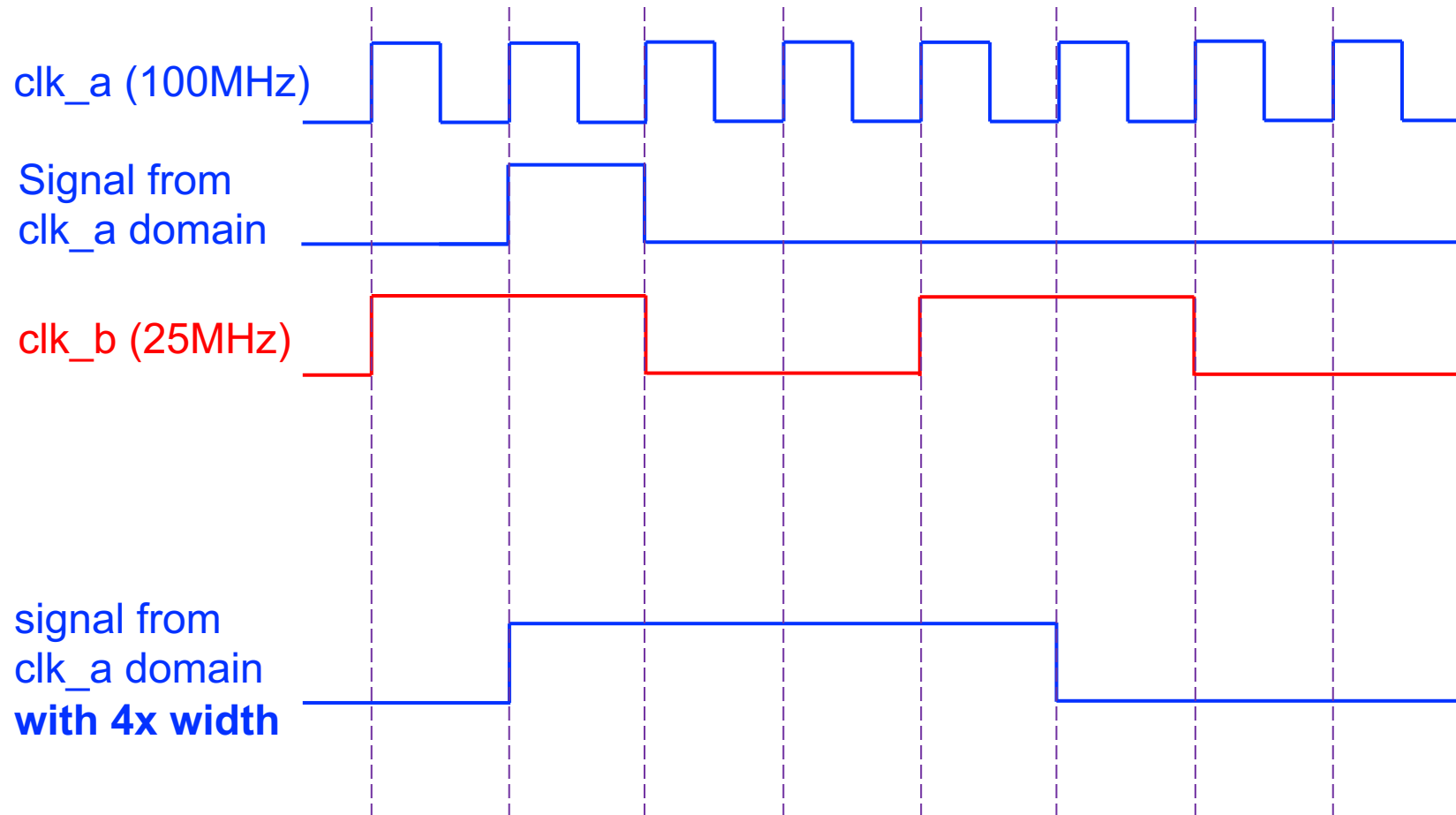
- ⦿ A design block with any inputs and outputs belonging to two or more clock domains



Src: <https://zipcpu.com/blog/2017/10/20/cdc.html>

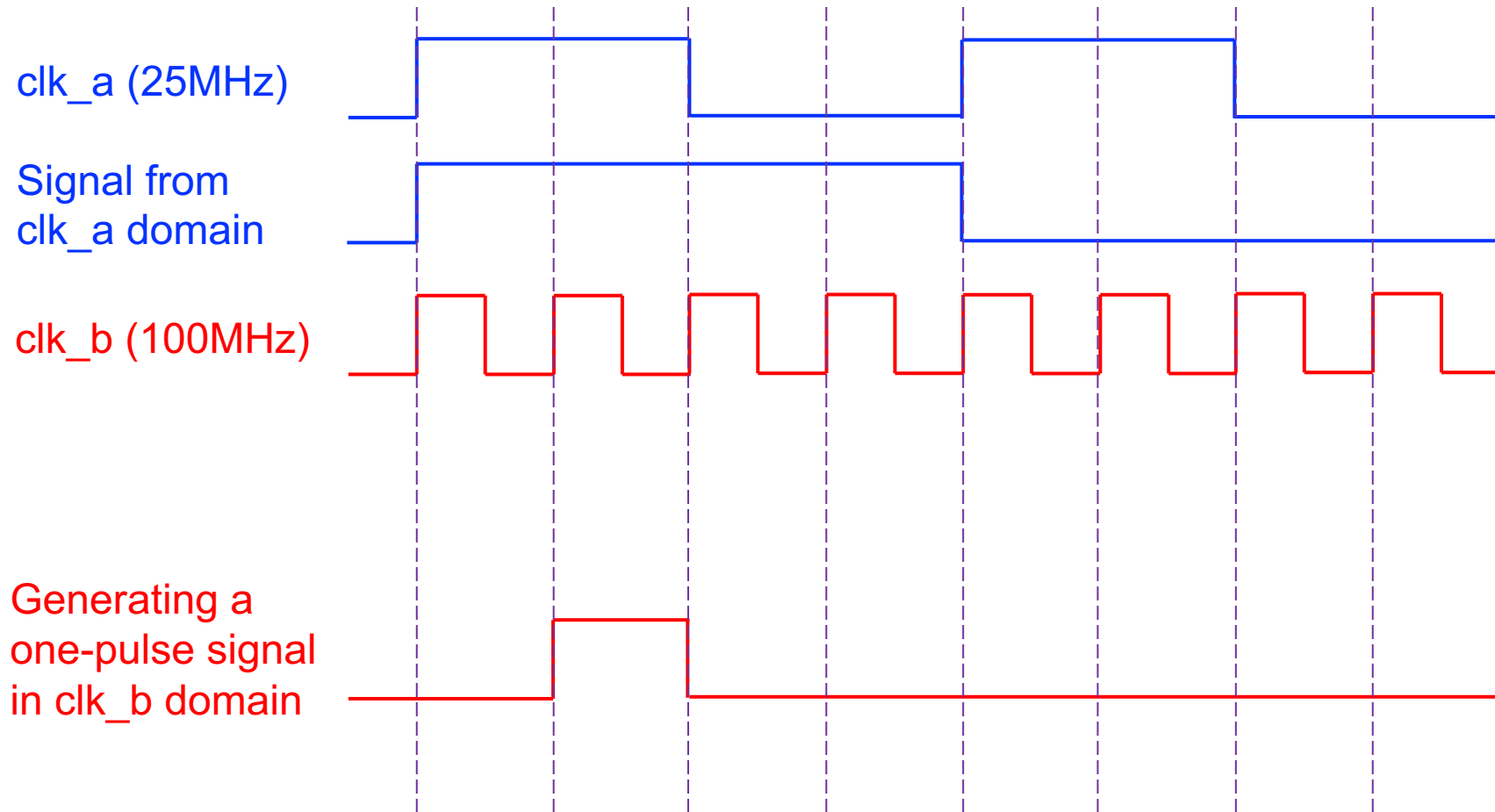
# Crossing from Faster Clock Domain to Slower Clock Domain

- Two simple *\*in-phase\** clocks



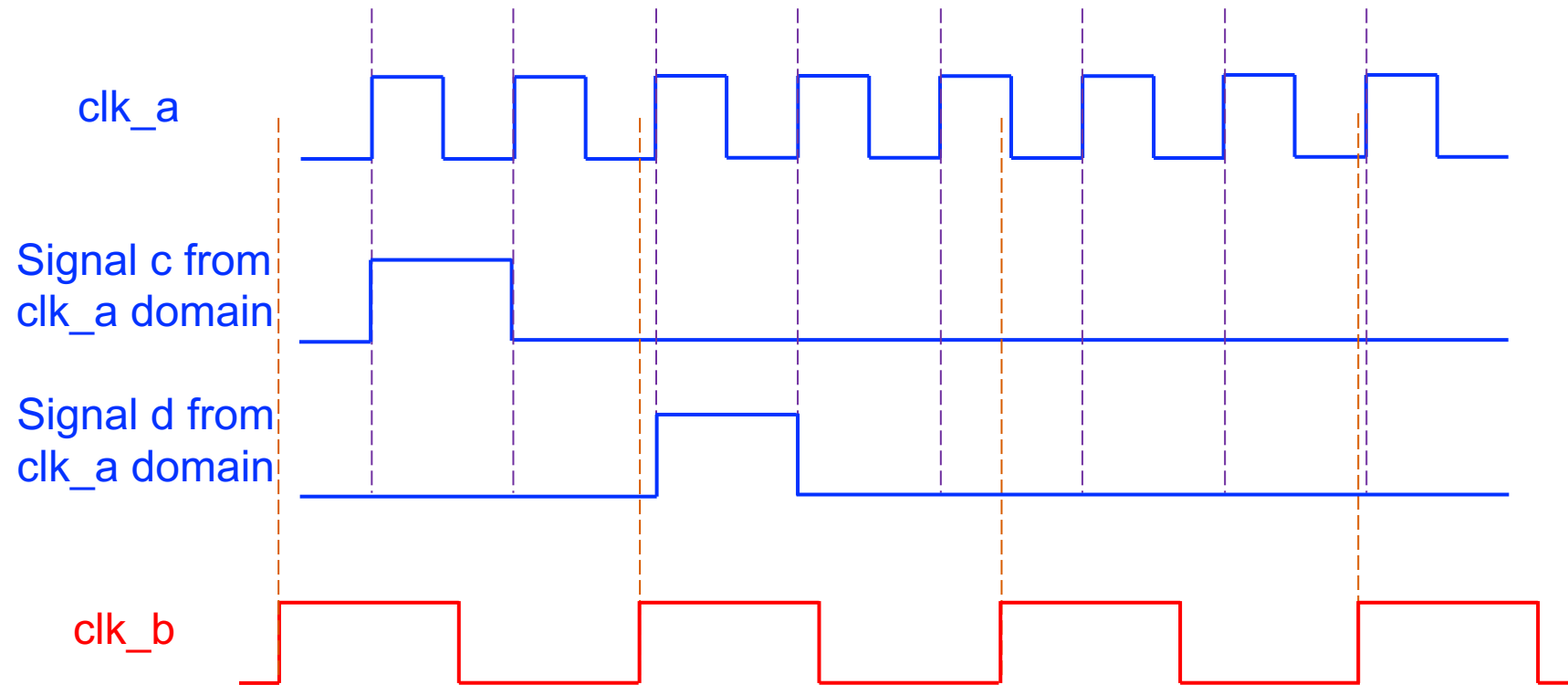
# Crossing from Slower Clock Domain to Faster Clock Domain

- Two simple *\*in-phase\** clocks





# Clocks with Arbitrary Phases and Frequencies



# Setup Time and Hold Time

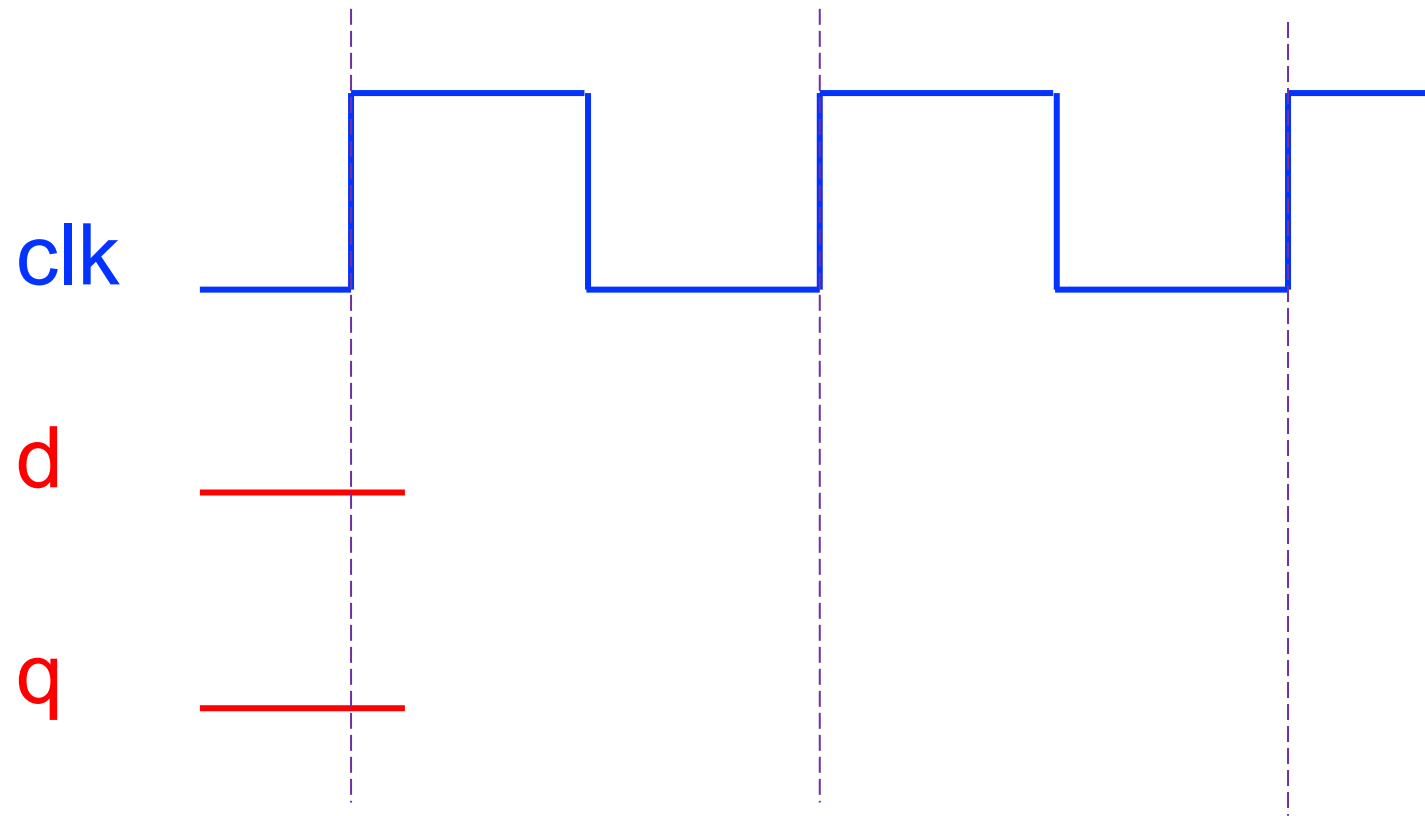
## ⦿ Setup time

- ◆ D input must be maintained at a constant value prior to the application of the positive clock pulse
- ◆ Data to the internal latches

## ⦿ Hold time

- ◆ Data input must not change after the application of the positive clock pulse
- ◆ Clock to the internal latch

# Timing for Setup Time and Hold Time





The background of the image is a dense, overlapping collection of numerous analog alarm clocks. The clocks vary in size, color (including red, blue, green, yellow, and silver), and design. Some have standard 12-hour faces, while others have different scales or features. The clocks are arranged in a way that creates a sense of a vast, complex system. A semi-transparent dark grey rectangular box is centered over the image, containing the text.

**For a typical medium-size  
system chip, there can be  
tens of clock domains.**

*Image Credit: [best-wallpaper.net](http://best-wallpaper.net)*

# Handshaking



# Asynchronous vs. Synchronous Handshaking

## ⦿ Handshaking

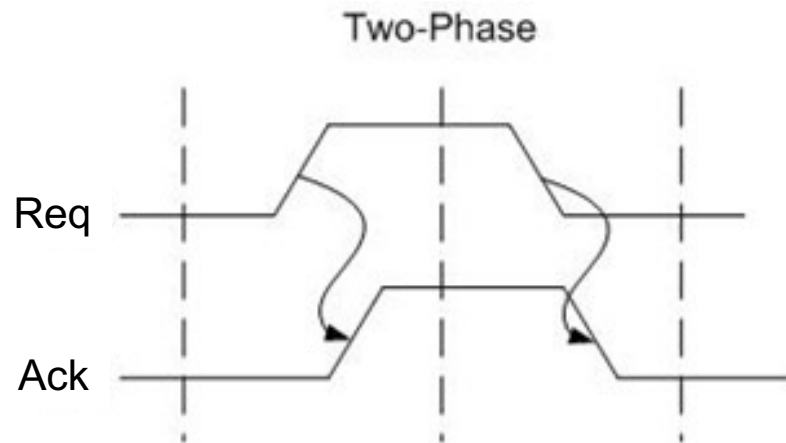
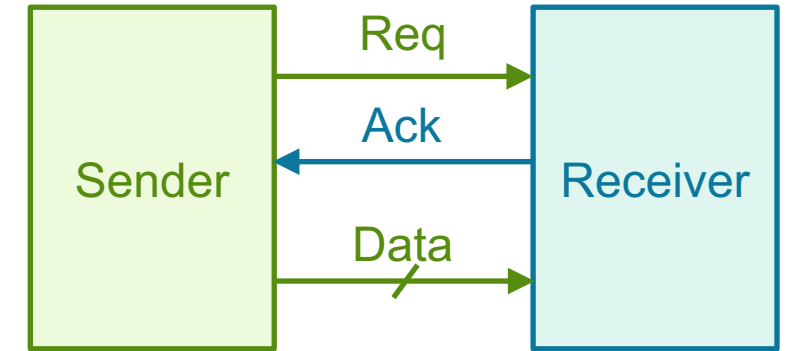
- ◆ A communication process in which two devices or systems are connected

## ⦿ Handshaking for asynchronous data transfer

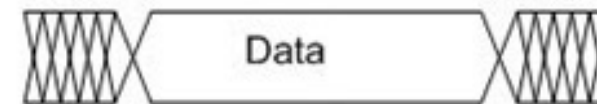
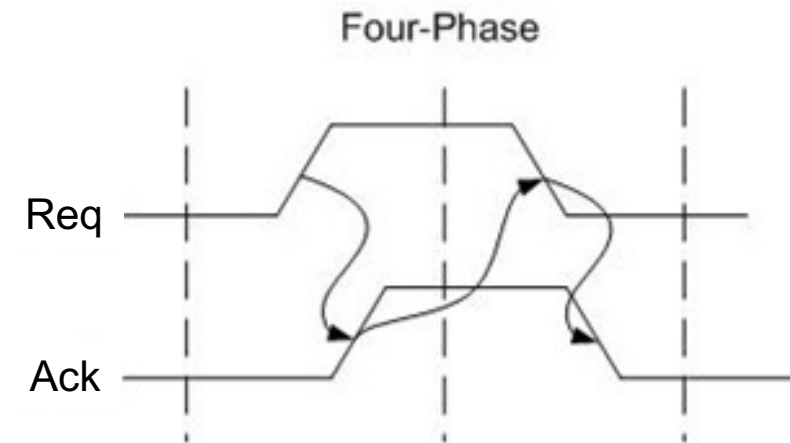
- ◆ The clock rates for sender and receiver may be quite different
- ◆ The sender needs to know whether the receiver has received the information
- ◆ Handshaking is a way to enable sender and receiver to coordinate data transfers

# Asynchronous Handshaking

- Without the synchronous clock
- Four-phase and two-phase handshaking protocol



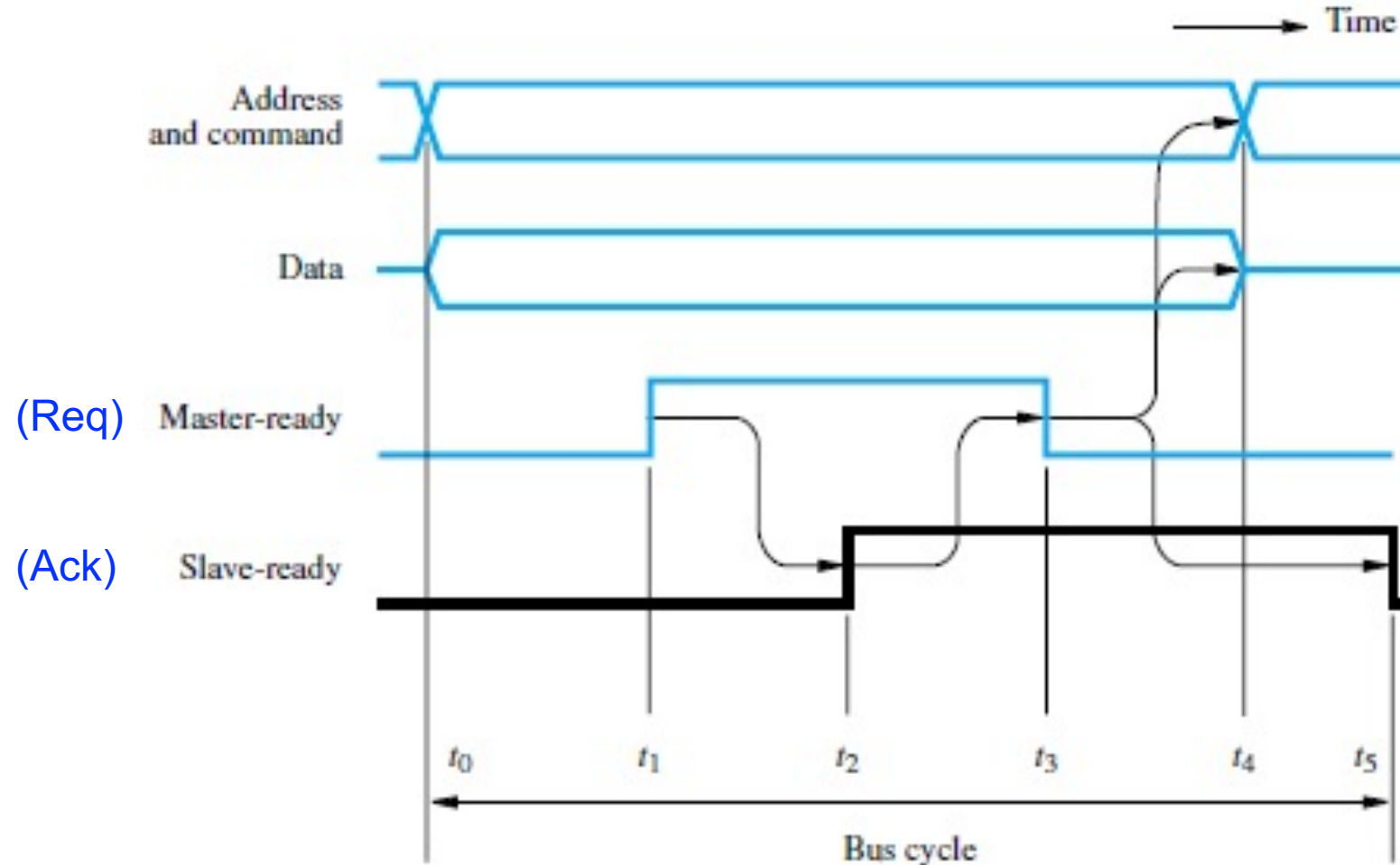
(a) 2-phase handshake protocol



(b) 4-phase handshake protocol

# Asynchronous Handshaking of Data Transfer for Output Operation

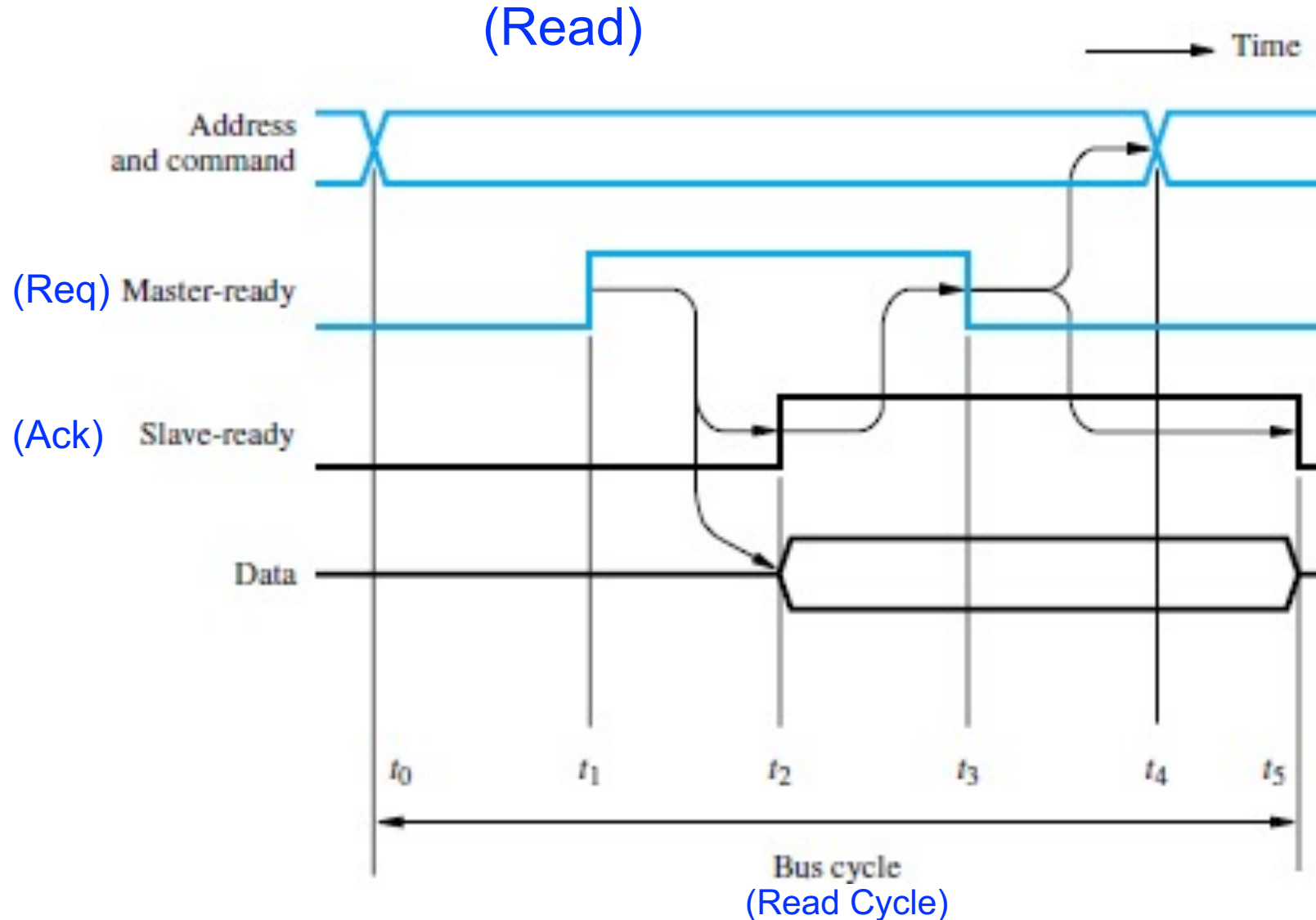
(Write)



(Write Cycle)

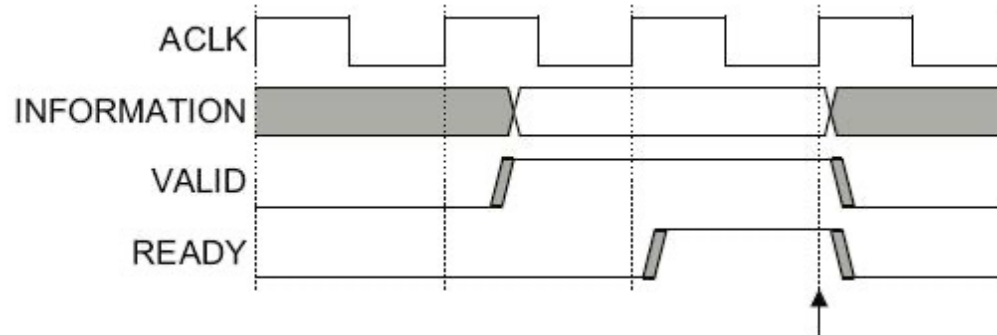


# Asynchronous Handshaking of Data Transfer for Input Operation

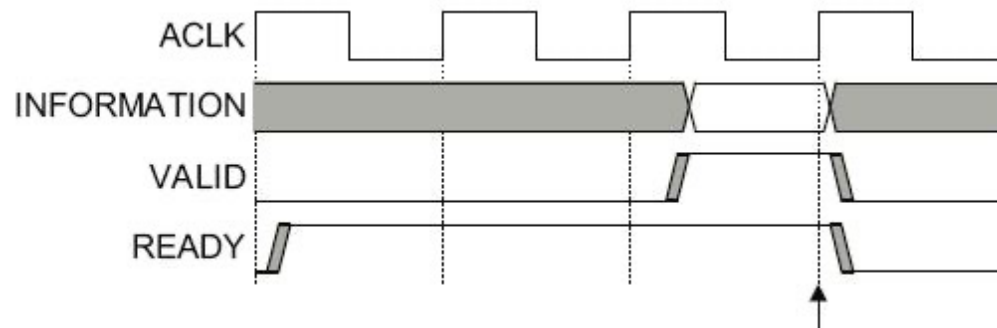


# Synchronous Handshaking

## 1. VALID before READY



## 2. READY before VALID



## 3. VALID with READY

