EECS 2070 02 Fall 2021

Improper Coding Styles

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Lecture 08

聲明

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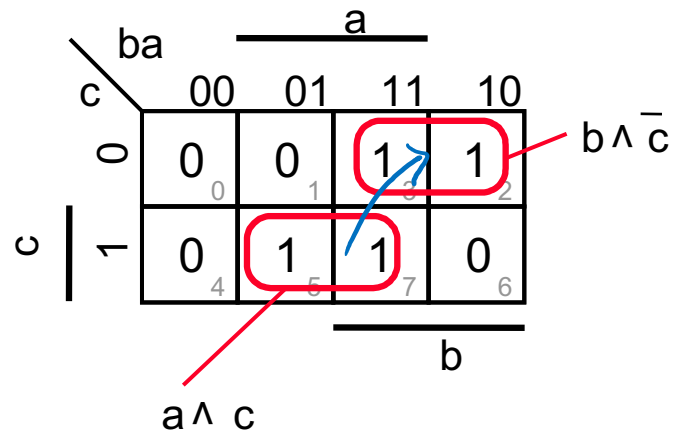
Hazards

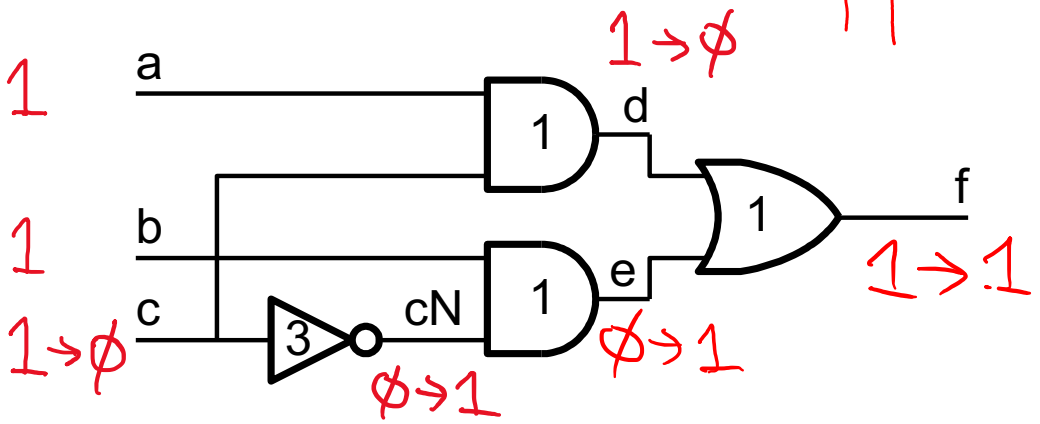
Hazards (or Glitches)

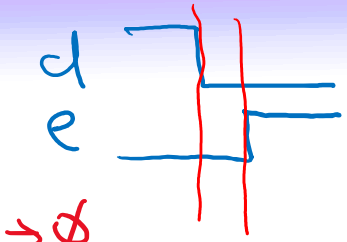
- Unwanted switching transients appearing in the output of a combinational circuit while its inputs change
- Types of hazards (assuming only a single input can change at a time and no other input will change until the circuit has stabilized)

(a) Static 1-hazard (b) Static 0-hazard (c) Dynamic hazards

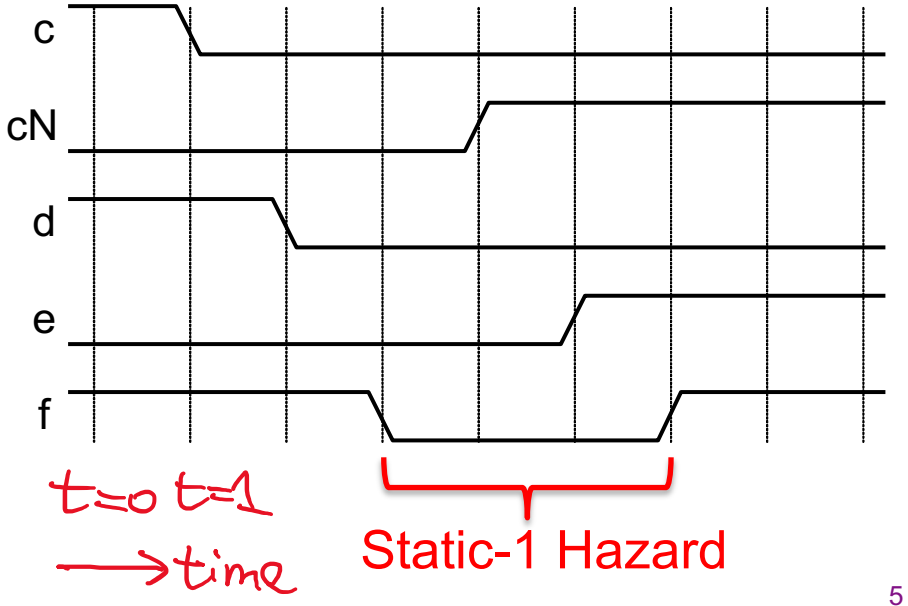
Hazards (cont)



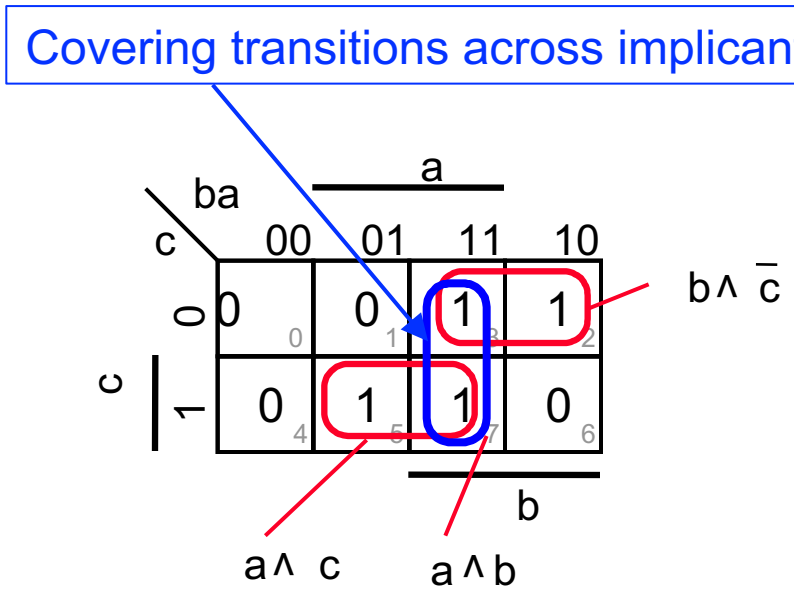


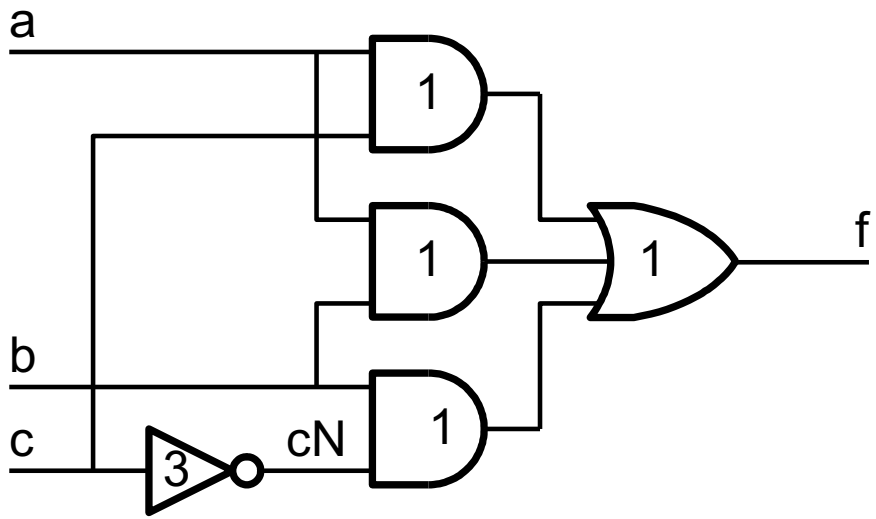


- Function output transits across two implicants
  → Possible hazards



Hazard Eliminating

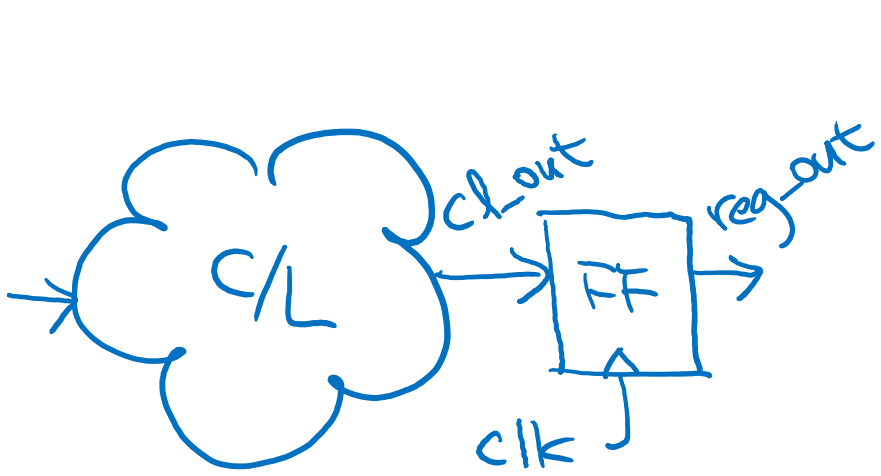


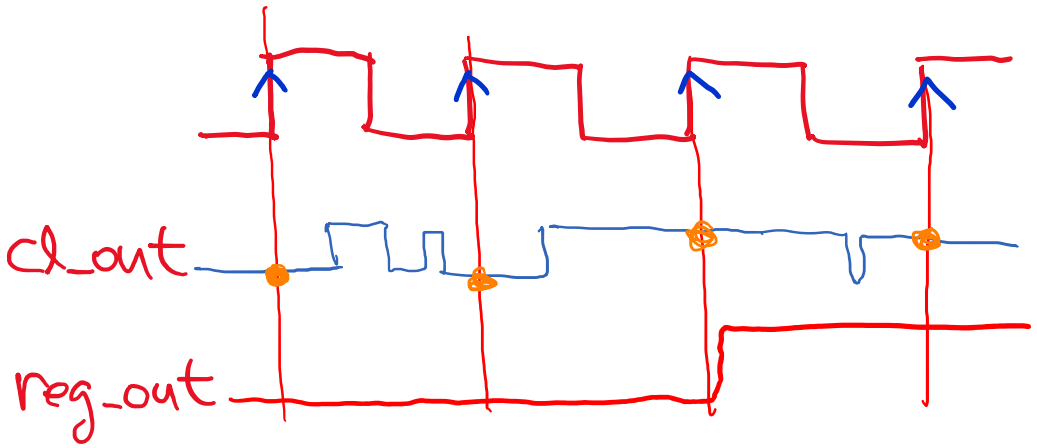


Synchronous Design vs. Asynchronous Design

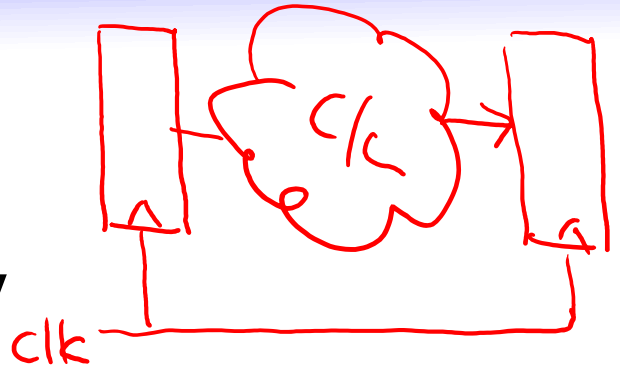
Synchronous Design

- Cycle-based





Asynchronous Sequential Circuit



- Asynchronous sequential circuit is hard to verify

```
always @(posedge en) begin
  ...
```

- We prefer synchronous, single-clock sequential blocks

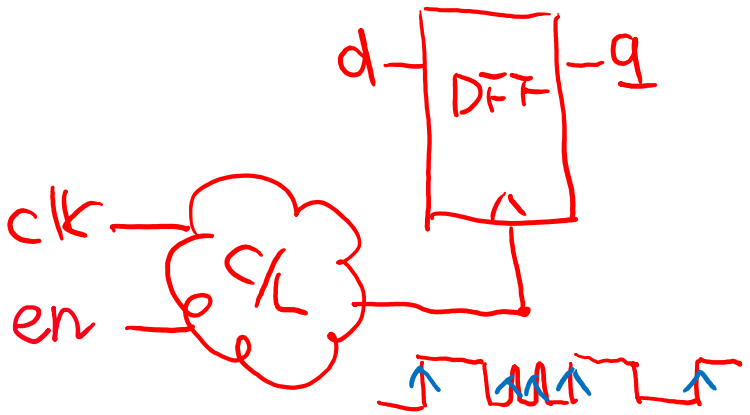
Gated Clock

- Introduces unexpected glitches to the clock signal
- Also makes the circuit asynchronous

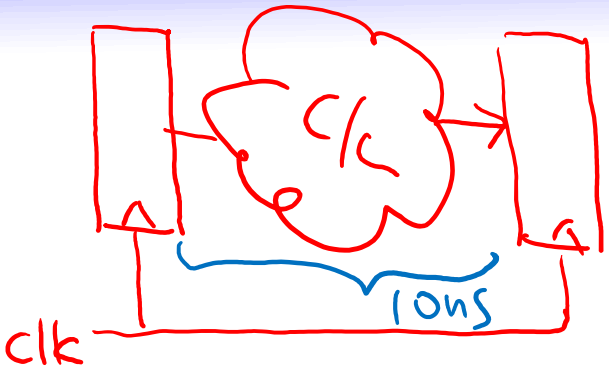
```
always @(clk or en) begin
   ...
```

```
always @* begin
   ...
   condition = clk & en;
```

```
always @* begin
   ...
   if (clk == 1) ...
```

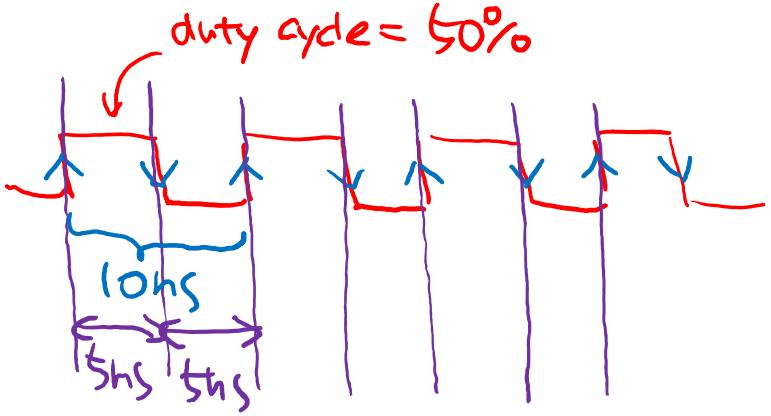


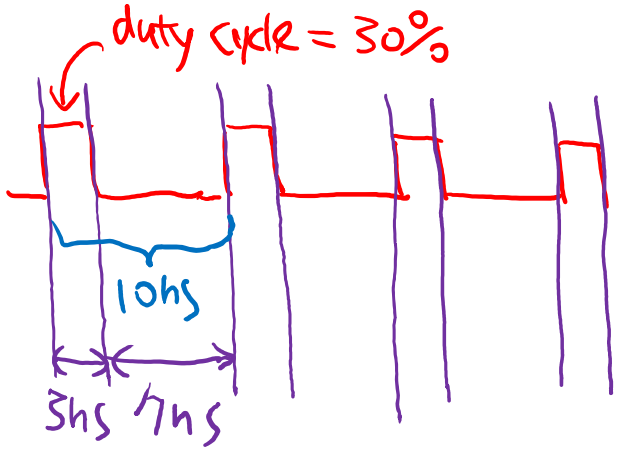
Dual Clock-edge Triggered



- Reduces the effective clock period
- Runs into trouble when the duty cycle of the clock isn't 50% as the ideal case

```
always @(posedge clk or negedge clk) begin
   ...
```





Mixed Edge and Level Triggered

- Mixed edge-triggered and level-sensitive control in an always block

```
always @(addr or posedge clk) begin
...
```

  - Syntax error for old Verilog simulator
  - Acceptable now, but restricted to

```
always @(posedge clk or reset)
   |||
always @(posedge clk or posedge reset)
```

X or Z for Outputs of Combinational Circuits

- Incorrect connection of IO ports
  - Width mismatch
  - Floating input
    - Undefined reg-type signal: **X**
    - Unconnected wire-type signal: **Z**
- Sometimes designers assign outputs as an **X** for invalid inputs on purpose
  - Not recommended for synthesizable design
  - **X** only exists in simulation, not in realistic world

```
case
  ...
  default: out = 1'bx;
endcase
```