CT Verilog Series

Fundamental Concepts for Verilog HDL

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Software Programming ≠ Hardware Description

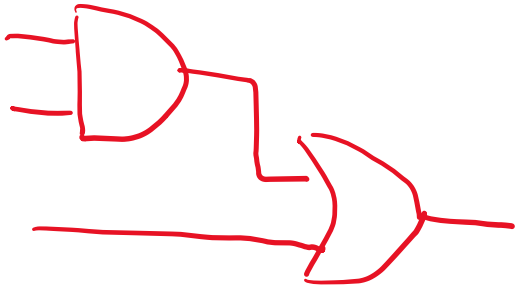
Software Programming Language

- Executed on a specific hardware
  - CPUs (central processing units)
  - DSP (digital signal processors)
  - GPUs (graphic processing units)

Hardware Description Language (HDL)

- Highly portable and readable
- High-level descriptive styles
- Hardware concurrency
- Rapid prototyping and synthesis

合成



RTL
(register transfer level)

R1 ← R2+R3

- Using HDL
  - Coding: to design/describe hardware design
    - Design first, coding second
    - Synthesizable (RTL) Verilog code
  - Simulation: to simulate the hardware behavior
    - Event-based simulation for the efficiency
    - Simulated parallel execution of instances and `always`/`initial` blocks
  - Synthesis: to implement the design with IC gates/cells, or FPGAs

Software vs. Hardware Description

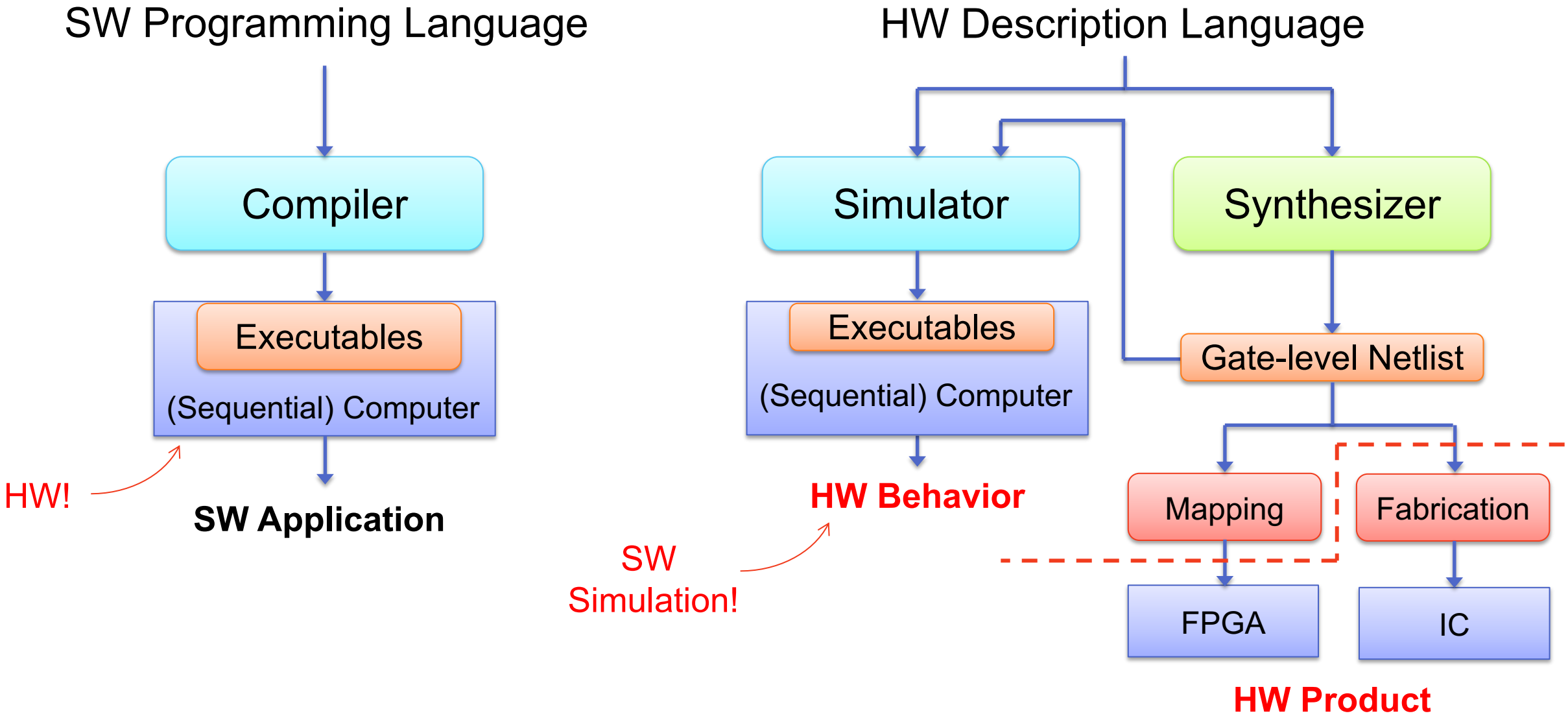
Software	Hardware
Sequential Statements	Parallel Constructs; Timing

Spatial Information

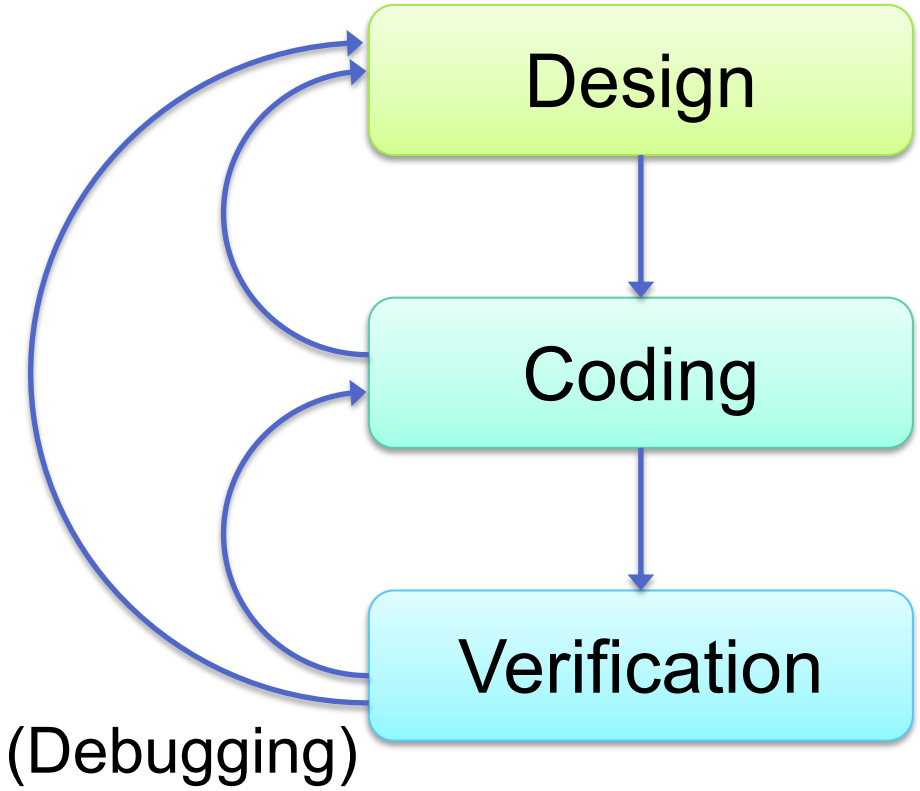
Temporal Information

- How to model the parallel behavior and timing behavior in HW Description Language?

Software vs. Hardware on Development Concept



Software vs. Hardware on Development Cycle



SW vs. HW

Flowchart, Block Diagram
Finite-State Machine, etc.

Coding Style,
Revision Control

Test Patterns (Testbench; Test Stimulus)
Regression Test

Summary for Logic Design Modeling and Implementation

- Plan your design first with block diagrams (and finite-state machines) and then construct Verilog codes
- Verilog RTL coding philosophy is not the same as software programming
  - Every Verilog RTL construct has its own logic mapping (for synthesis)
  - You have to understand the concepts of Verilog simulation
  - You have to write synthesizable RTL codes