EECS 2070 02 Fall 2021

FPGA Utilization with Vivado

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Lecture 17

聲明

- 本課程之內容 (包括但不限於教材、影片、圖片、檔案資料等)，僅供修課學生個人合理使用，非經授課教師同意，不得以任何形式轉載、重製、散布、公開播送、出版或發行本影片內容(例如將課程內容放置公開平台上，如 Facebook, Instagram, YouTube, Twitter, Google Drive, Dropbox 等等)。如有侵權行為，需自負法律責任。

Overview of Artix-7 35T FPGA

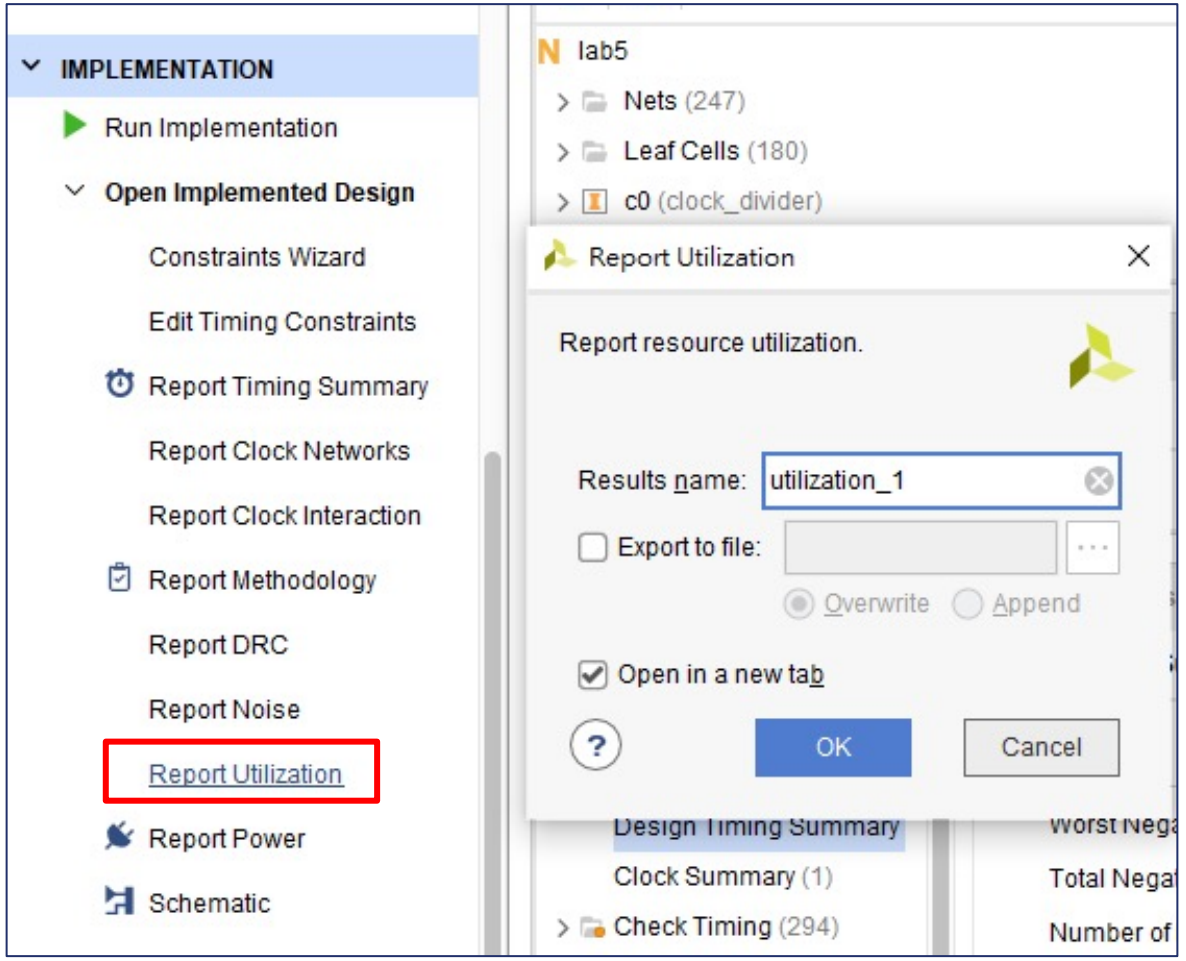
- Part number: XC7A35T-1CPG236C
- 33,280 logic cells in 5200 slices
  - Each slice contains four 6-input LUTs and 8 flip-flops
- 1,800 Kbits of fast block RAM
- 90 DSP slices
- Five clock management tiles
  - Each with a phase-locked loop (PLL)
- Internal clock speeds exceeding 450MHz

Some References

- Vivado Design Hub - Design Flows Overview
  - https://www.xilinx.com/support/documentation-navigation/design-hubs/dh0002-vivado-design-flows-overview-hub.html
- Vivado Design Hub – Logic Synthesis
  - https://www.xilinx.com/support/documentation-navigation/design-hubs/dh0018-vivado-synthesis-hub.html
- Vivado Design Suite User Guide
  - Getting started: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2020_1/ug910-vivado-getting-started.pdf
  - Synthesis: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2020_1/ug901-vivado-synthesis.pdf
  - Design Analysis and Closure Techniques: https://www.xilinx.com/support/documentation/sw_manuals/xilinx2020_1/ug906-vivado-design-analysis.pdf
    - P.186: Report Utilization

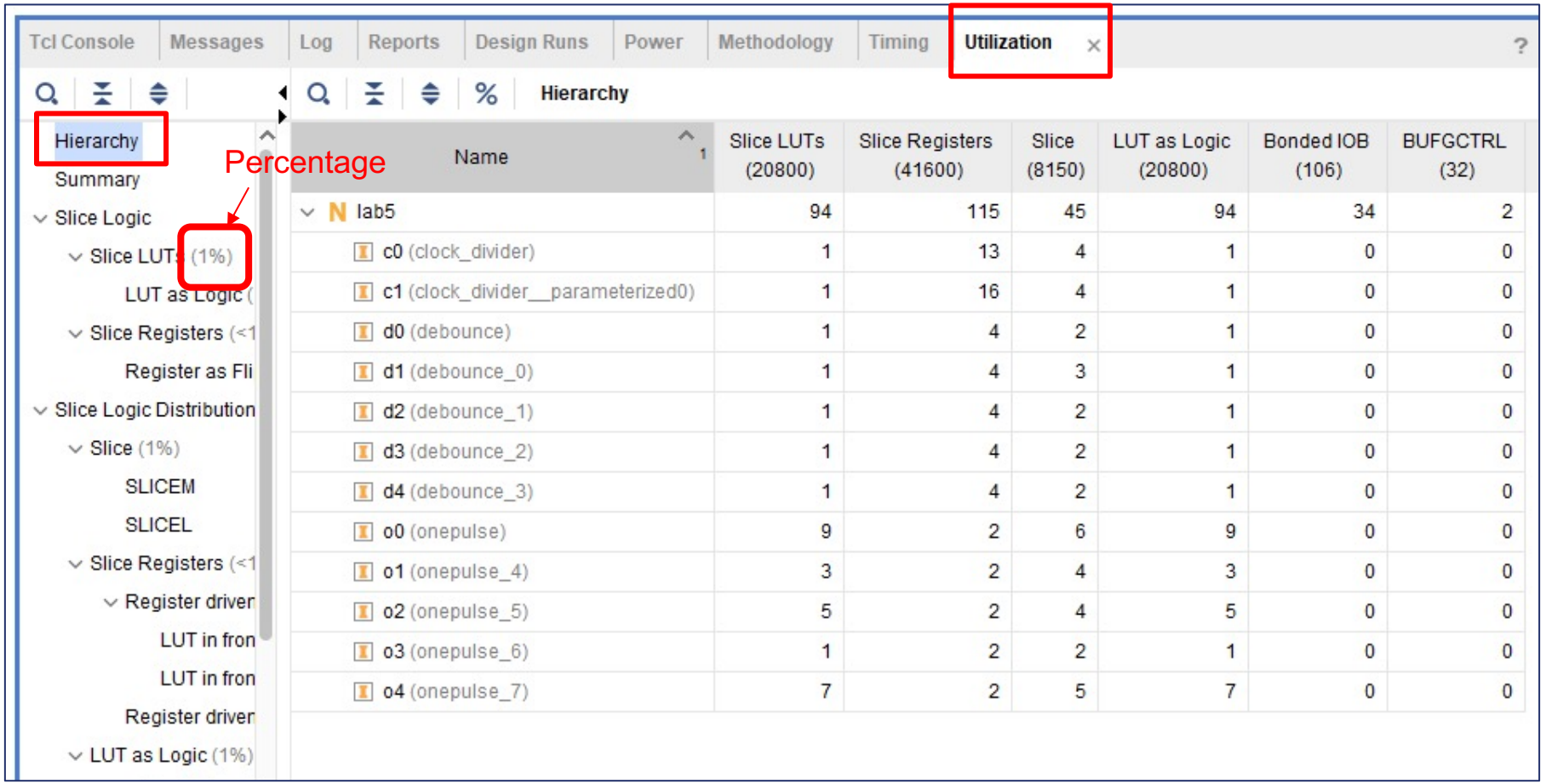
Report Utilization

- After “Run Implementation”



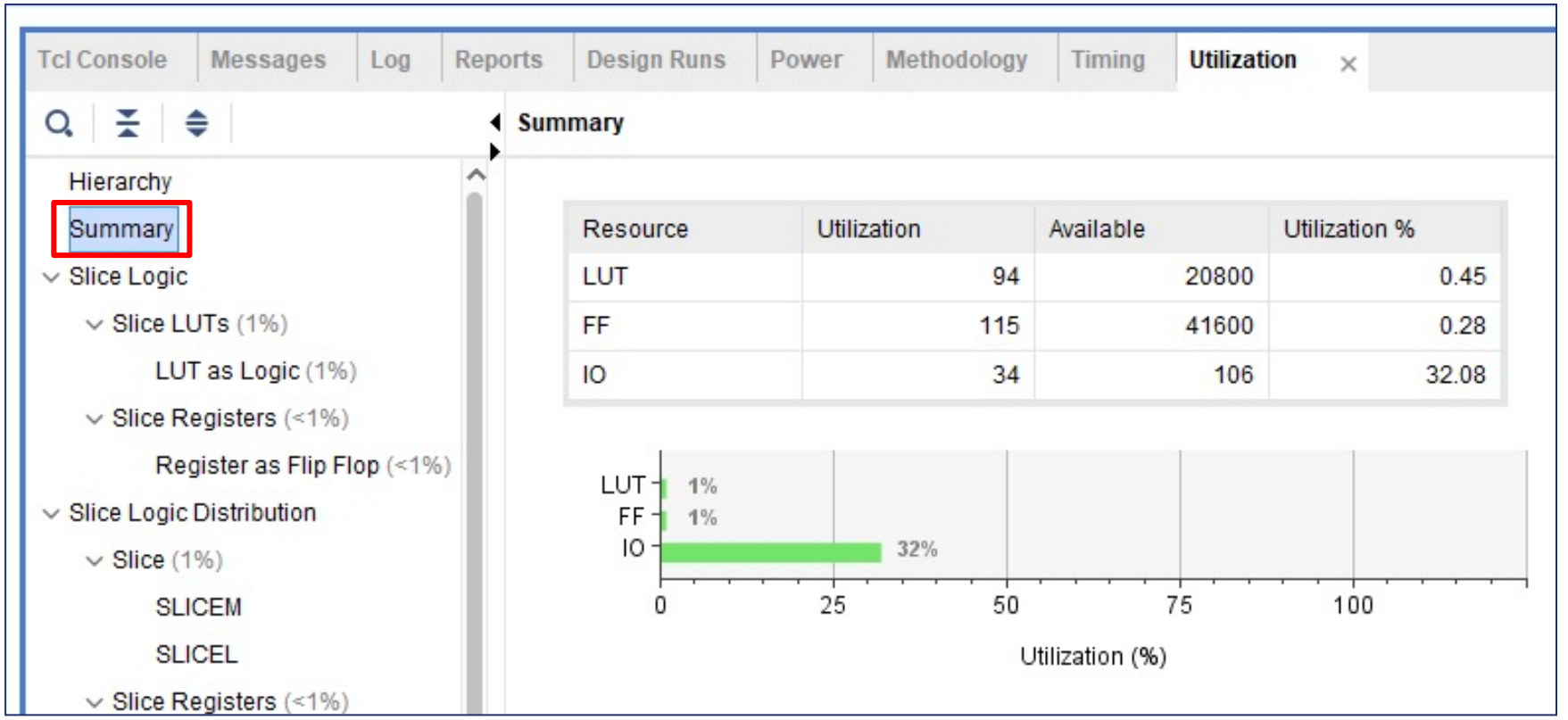
Utilization Overview

- Hierarchy view

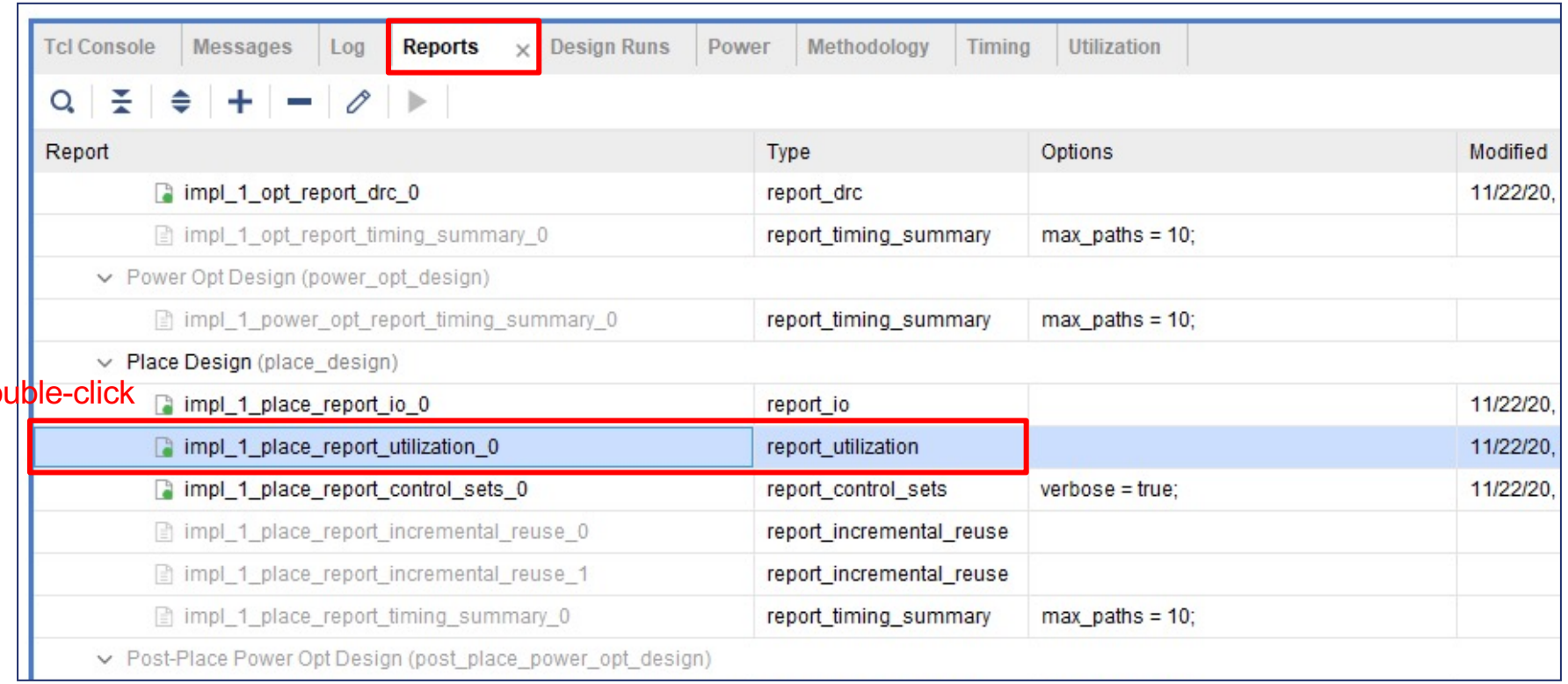


Name	Slice LUTs (20800)	Slice Registers (41600)	Slice (8150)	LUT as Logic (20800)	Bonded IOB (106)	BUFGCTRL (32)
lab5	94	115	45	94	34	2
c0 (clock_divider)	1	13	4	1	0	0
c1 (clock_divider__parameterized0)	1	16	4	1	0	0
d0 (debounce)	1	4	2	1	0	0
d1 (debounce_0)	1	4	3	1	0	0
d2 (debounce_1)	1	4	2	1	0	0
d3 (debounce_2)	1	4	2	1	0	0
d4 (debounce_3)	1	4	2	1	0	0
o0 (onepulse)	9	2	6	9	0	0
o1 (onepulse_4)	3	2	4	3	0	0
o2 (onepulse_5)	5	2	4	5	0	0
o3 (onepulse_6)	1	2	2	1	0	0
o4 (onepulse_7)	7	2	5	7	0	0

Summary View



Report


Tcl Console
Messages
Log
Reports
Design Runs
Power
Methodology
Timing
Utilization
Report
Type
Options
Modified
impl_1_opt_report_drc_0
report_drc
11/22/20,
impl_1_opt_report_timing_summary_0
report_timing_summary
max_paths = 10;
Power Opt Design (power_opt_design)
impl_1_power_opt_report_timing_summary_0
report_timing_summary
max_paths = 10;
Place Design (place_design)
Double-click
impl_1_place_report_io_0
report_io
11/22/20,
impl_1_place_report_utilization_0
report_utilization
11/22/20,
impl_1_place_report_control_sets_0
report_control_sets
verbose = true;
11/22/20,
impl_1_place_report_incremental_reuse_0
report_incremental_reuse
impl_1_place_report_incremental_reuse_1
report_incremental_reuse
impl_1_place_report_timing_summary_0
report_timing_summary
max_paths = 10;
Post-Place Power Opt Design (post_place_power_opt_design)

Report

- You can find the report at somewhere like lab5/lab5.runs/impl_1/lab5_1_utilization_placed.rpt

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	94	0	20800	0.45
LUT as Logic	94	0	20800	0.45
LUT as Memory	0	0	9600	0.00
Slice Registers	115	0	41600	0.28
Register as Flip Flop	115	0	41600	0.28
Register as Latch	0	0	41600	0.00
F7 Muxes	0	0	16300	0.00
F8 Muxes	0	0	8150	0.00

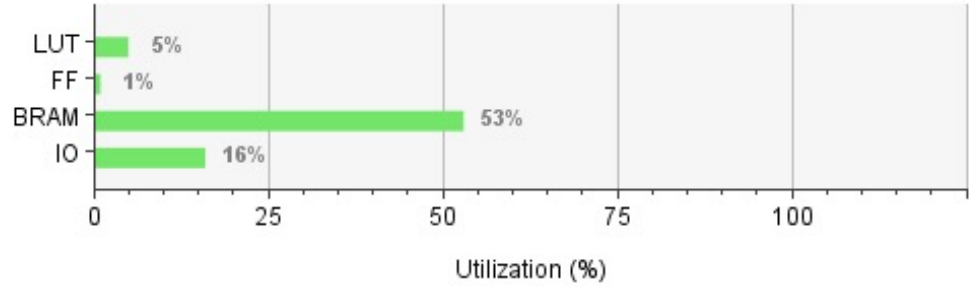
2. Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	45	0	8150	0.55
SLICEL	36	0		
SLICEM	9	0		
LUT as Logic	94	0	20800	0.45
using O5 output only	0			
using O6 output only	59			
using O5 and O6	35			
LUT as Memory	0	0	9600	0.00
LUT as Distributed RAM	0	0		
LUT as Shift Register	0	0		
Slice Registers	115	0	41600	0.28
Register driven from within the Slice	96			
Register driven from outside the Slice	19			
LUT in front of the register is unused	17			
LUT in front of the register is used	2			
Unique Control Sets	10		8150	0.12

Ex: VGA Example (Lab7-2)

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)
top	1100	92	18	373	1100	26.5	17	2
blk_mem_gen_0_inst (blk_	84	11	18	45	84	26.5	0	0
clk_wiz_0_inst (clock_divide	1	22	0	6	1	0	0	1
mem_addr_gen_inst (mem	172	27	0	75	172	0	0	0
split_1pulse (one_pulse)	0	2	0	1	0	0	0	0
split_debounce (debounce)	1	4	0	2	1	0	0	0
vga_inst (vga_controller)	350	22	0	230	350	0	0	0

Resource	Utilization	Available	Utilization %
LUT	1100	20800	5.29
FF	92	41600	0.22
BRAM	26.50	50	53.00
IO	17	106	16.04



Sample Report

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs	1100	0	20800	5.29
LUT as Logic	1100	0	20800	5.29
LUT as Memory	0	0	9600	0.00
Slice Registers	92	0	41600	0.22
Register as Flip Flop	75	0	41600	0.18
Register as Latch	0	0	41600	0.00
F7 Muxes	18	0	16300	0.11
F8 Muxes	0	0	8150	0.00

Sample Report

2. Slice Logic Distribution

Site Type	Used	Fixed	Available	Util%
Slice	373	0	8150	4.58
SLICEL	275	0		
SLICEM	98	0		
LUT as Logic	1100	0	20800	5.29
using O5 output only	2			
using O6 output only	876			
using O5 and O6	222			
LUT as Memory	0	0	9600	0.00
LUT as Distributed RAM	0	0		
LUT as Shift Register	0	0		
Slice Registers	92	0	41600	0.22
Register driven from within the Slice	69			
Register driven from outside the Slice	23			
LUT in front of the register is unused	12			
LUT in front of the register is used	11			
Unique Control Sets	9		8150	0.11

Report: VGA Sample

3. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	26.5	0	50	53.00
RAMB36/FIFO*	26	0	50	52.00
RAMB36E1 only	26			
RAMB18	1	0	100	1.00
RAMB18E1 only	1			

4. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	90	0.00

Summary

- Refer to FPGA architecture and its basic components (e.g., slice, LUT, BRAM, DSP)
- You may check the utilization report for different labs (especially Labs 5, 6, 7 and 8)
- There are limited resources
  - True for any practical hardware (software) implementation
  - Skilled designers can manage to realize efficient designs