# CHENFENG ZHAO

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## RESEARCH INTERESTS

Computer Architecture, High-Performance Computing, Graph Partition, Machine Learning Acceleration, Hardware and Software Co-design, System-on-Chip, FPGA.

## EDUCATION

**Washington University in St. Louis** — Saint Louis, MO, USA
Ph.D. in Computer Engineering — Sep 2018 - Present
Advisor: Prof. Xuan 'Silvia' Zhang & Prof. Roger Chamberlain

**University of Electronic Science and Technology of China** — Chengdu, China
MSc in Microelectronics and Solid-State Electronics — Sep 2015-Jul 2018
Advisor: Prof. YiWen Wang

**University of Electronic Science and Technology of China** — Chengdu, China
BEng in Integrated Circuit Design and Integrated Systems — Sep 2011- Jul 2015

## PROJECTS

**High-Level Synthesis for Graph Neural Network Acceleration** — Feb 2022 – present
*Build a High-Level Synthesis (HLS) benchmark suite for various Graph Neural Network (GNN) models*

- Build, train and execute GNN models based on Pytorch and DGL to generate input data.
- Build and optimize HLS benchmarks for GNN acceleration on Xilinx Vitis.
- Deploy and implement GNN HLS benchmarks on Xilinx U280 FPGA Board.

**Near-Data Processing for Graph Processing** — Mar 2020 – Jun 2022
*Apply Near-Data Processing (NDA) technique to accelerate domain-specific applications*

- Proposed an end-to-end hardware/software co-designed framework, including graph partitioning algorithms, programming model, High-Level Synthesis (HLS) hardware generators and graph representation, for near-memory architectures to accelerate graph processing applications.
- Built full-system bare-metal NDA simulation platform based on multiple 3D memory cubes.

**Near-Data Processing for Data Integration** — July 2019 – Mar 2020
*Apply NDA technique to accelerate data-integration applications*

- Extended cycle-accurate simulation system (Gem5) for Near-Data Processing.
- Implemented various characterization methodologies for data integration applications.
- Proposed a Near-Data Processing system to improve applications' performance and energy-efficiency.

**Module-Supported SOC Chip Designing (taped out)** — Sep 2016 – Apr 2018
*Designed an ARM Cortex-M3 processor-based SoC, including peripherals such as CAN, GMAC, SPI, ADC, SMC, and an FPGA configuration module. Corresponding functions completed through software collaboration*

- Completed SoC architecture design, simulation and prototyping, including IP interconnection with Perl script, CPU customization, memory, reset, debug, and interrupt systems.
- Designed Selectmap IP core using Verilog HDL to configure multiple Xilinx 7 Series FPGAs at speeds 8-32 times higher than traditional SCI configuration modules. Verification undertaken on the Kintex-7 FPGA prototyping platform using C, Keil and Vivado.
- Designed the clock domain crossing module, making CPU and AHB system peripherals work at different clock frequencies, greatly reducing SoC power consumption.

- Programmed Micron PC28F00BM29EWHA flash algorithms using C, and verified it on the prototype platform, enabling hex files to be downloadable to external Flash via Keil and Ulink.
- Designed code bus matrix to realize memory address remap, allowing the system to boot from different memories selected by the internal address remapping register and external boot pins.
- Wrote scatter files to realize scatter loading function to greatly improve SoC performance by making the CPU automatically transport read-only data from embedded flash and external flash to high-speed SRAM.

**Hardware and Software Co-Design Based on PCI Interface** Jun 2016 - Jul 2016
*Through PCI bus and PLX9054, completed large-scale data transmission between PC and FPGA.*

- Designed hardware system based on PCI interface protocol and PLX 9054 using Verilog HDL to realize large-scale data transmission.
- Programmed host computer software using C++, according to PCI protocol, PCI 9054 technical reference manual and SDK library functions.
- Verified software and hardware systems on Altera's CycloneII FPGA platform & host computer, which realized PCI target single and burst transfer mode for large-scale data transmission.

## TEACHING EXPERIENCE

**Washington University in St. Louis** Aug 2020 - Jan 2021
*Teaching Assistant - ESE 461 Design Automation for Integrated Circuit Systems*
**Washington University in St. Louis** Aug 2019 - Dec 2019 & Aug 2020 - Dec 2020
*Teaching Assistant - CSE 560 Computer Architecture*
**University of Electronic Science and Technology of China** Mar 2017 - Apr 2017
*Teaching Assistant - Comprehensive FPGA Course Design*
**University of Electronic Science and Technology of China** Jun 2016 - Jul 2016
*Teaching Assistant - Electronic Design Automation Technology*

## AWARDS

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|---|---|
| Postgraduate Student Union Department Star | 2015-2016 |
| Outstanding Postgraduate Student | 2015-2016 |
| 3 * The First-Class People's Scholarship | 2012-2013,2013-2014,2015-2016 |
| 2 * The Second-Class People's Scholarship | 2011-2012, 2016-2017 |

## SKILLS

**Programming Languages**
Python, C/C++, HLS C, Shell, Verilog HDL, VHDL, Makefile, ARM Assembly, OpenCL, TCL
**Software**
Linux, GEM5, Docker, Git, MATLAB, Pytorch, GCC/G++, Vitis, Verdi, VCS, ISE/Vivado, Quartus

## PUBLICATION

1. Darko Ivanovich, **Chenfeng Zhao**, Xuan Zhang, Roger D Chamberlain, Amit Deliwala, Viktor Gruev. "Chip-to-chip Optical Data Communications using Polarization Division Multiplexing." 2020 IEEE High Performance Extreme Computing Conference (HPEC). IEEE, 2020.

2. **Chenfeng Zhao**, Xuan Zhang, and Roger D. Chamberlain. "Executing Data Integration Effectively and Efficiently Near the Memory." IEEE Design & Test (2021).

3. **Chenfeng Zhao**, Roger D. Chamberlain, Xuan Zhang, "Graph Partitioning for Near Memory Processing," An In-Memory Architectures and Computing Applications Workshop (iMACAW), 2022.

4. **Chenfeng Zhao**, Roger D. Chamberlain, Xuan Zhang, "SuperCut: Communication-Aware Partitioning for Near-Memory Graph Processing," Computing Frontiers (CF), 2023.