Chenfeng Zhao

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Education

Washington University in St. Louis **Sep 2018 - Present**
Ph.D. in Computer Engineering, co-advised by Prof. Xuan Zhang & Prof. Roger Chamberlain *Saint Louis, MO, USA*

University of Electronic Science and Technology of China **Sep 2015-Jul 2018**
MSc in Microelectronics and Solid-State Electronics, advised by Prof. YiWen Wang *Chengdu, China*

University of Electronic Science and Technology of China **Sep 2011- Jul 2015**
BEng in Integrated Circuit Design and Integrated Systems *Chengdu, China*

Research Interests

High-Performance Computing, High-Level Synthesis (HLS), FPGA, Hardware & Software Co-design, Graph Neural Networks (GNNs) Acceleration, Computer Architecture, Graph Processing, System-on-Chip

Projects

HLPerf: Efficient Dynamic Performance Estimation for HLS-based GNNs **Aug 2023 – Dec 2023**
Pioneered an novel simulation framework called HLPerf for dynamic performance estimation of dataflow GNN HLS kernels

- Devised an approximately-cycle-accurate simulator using Simpy to estimate the dynamic performance of GNN HLS kernels with a dataflow architecture.
- Developed a front-end compiler to automatically transform the HLS C-based source code into simulation components.
- Proposed a set of pragma-driven quantitative expressions to model the performance impact of optimization techniques.
- Conducted a comprehensive evaluation demonstrating the error rate of HLPerf is 7% on average and it is 13500× faster than RTL simulation and over 400× faster than leading tools.

GNNHLS: High-Level Synthesis for Graph Neural Network Acceleration **Feb 2022 – Aug 2023**
Built a High-Level Synthesis (HLS) benchmark suite for various Graph Neural Network (GNN) models

- Devised an software stack using PyTorch and DGL for data generation and baseline deployment.
- Developed 6 well-tuned GNN HLS kernels and deployed them on the Xilinx U280 FPGA Board.
- Conducted comprehensive evaluation on 4 graph datasets, demonstrating it achieves up to 51× speedup and 423× energy reduction over multicore CPU baselines, and up to 5× speedup and 75× energy reduction over the GPU baseline.

Software/Hardware Co-design for Efficient Near-Memory Graph Processing **Mar 2020 – Jun 2022**
Created a software/hardware co-design framework called SuperCut for near-memory graph processing acceleration

- Devised sevaral graph partitioning algorithms to mitigate the communication issue of near-memory graph processing.
- Introduced a three-phase programming model for general vertex programs to bridge software and hardware designs.
- Designed specialized accelerators via HLS and mapped them to FPGA resources inside 3D-stacked memory cubes.
- Built full-system bare-metal simulation platform by extending Gem5 for the multiple 3D memory cubes system.
- Conducted comprehensive evaluation, demonstrating SuperCut achieves up to 1.8× total energy reduction and 2.6× speedup with 48% lower extra memory footprint relative to SOTA.

Near-Memory Processing for Data Integration **July 2019 – Mar 2020**
Applied Near-Memory technique to accelerate data-integration applications

- Extended cycle-accurate simulation system (Gem5) for Near-Data Processing Based on 3D-stacked memory.
- Implemented various characterization methodologies for data integration applications.
- Proposed a Near-Memory Processing system that significantly enhanced application performance by an average of 3.5× and reduced energy consumption by an average of 4.2× (76%) compared to conventional systems.

Module-Supported SOC Chip Designing (taped out) **Sep 2016 – Apr 2018**
Designed an ARM Cortex-M3 processor-based SoC, including peripherals such as CAN, GMAC, SPI, ADC, SMC, and an FPGA configuration module. Corresponding functions completed through software collaboration

- Completed SoC architecture design, simulation and prototyping, including IP interconnection with Perl script, CPU customization, memory, reset, debug, and interrupt systems.
- Designed Selectmap IP core using Verilog HDL to configure multiple Xilinx 7 Series FPGAs at speeds $8-32\times$ higher than traditional SCI configuration modules. Verification undertaken on the Kintex-7 FPGA prototyping platform using C, Keil and Vivado.
- Designed the clock domain crossing module, making CPU and AHB system peripherals work at different clock frequencies, greatly reducing SoC power consumption.
- Programmed Micron PC28F00BM29EWHA flash algorithms using C, and verified it on the prototype platform, enabling hex files to be downloadable to external Flash via Keil and Ulink.
- Designed code bus matrix to realize memory address remap, allowing the system to boot from different memories selected by the internal address remapping register and external boot pins.

- Wrote scatter files to realize scatter loading function to greatly improve SoC performance by making the CPU automatically transport read-only data from embedded flash and external flash to high-speed SRAM.

Hardware and Software Co-Design Based on PCI Interface **Jun 2016 - Jul 2016**

Through PCI bus and PLX9054, completed large-scale data transmission between PC and FPGA.

- Designed hardware system based on PCI interface protocol and PLX 9054 using Verilog HDL to realize large-scale data transmission.
- Programmed host computer software using C++, according to PCI protocol, PCI 9054 technical reference manual and SDK library functions.
- Verified software and hardware systems on Altera's CycloneII FPGA platform & host computer, which realized PCI target single and burst transfer mode for large-scale data transmission.

Teaching Experience

Washington University in St. Louis **Jan 2024**
Teaching Assistant - CSE 566S High Performance Computer Systems

Washington University in St. Louis **Aug 2020 - Jan 2021**
Teaching Assistant - ESE 461 Design Automation for Integrated Circuit Systems

Washington University in St. Louis **Aug 2019 - Dec 2019 & Aug 2020 - Dec 2020**
Teaching Assistant - CSE 560 Computer Architecture

niversity of Electronic Science and Technology of China **Mar 2017 - Apr 2017**
Teaching Assistant - Comprehensive FPGA Course Design

University of Electronic Science and Technology of China **Jun 2016 - Jul 2016**
Teaching Assistant - Electronic Design Automation Technology

Awards

Honors Designation for PhD Progress Review (Top 15-20% of students) *2021-2022, 2022-2023*
Postgraduate Student Union Department Star *2015-2016*
Outstanding Postgraduate Student *2015-2016*
*3 * The First-Class People's Scholarship* *2012-2013,2013-2014,2015-2016*
*2 * The Second-Class People's Scholarship* *2011-2012, 2016-2017*

Technical Skills

Languages: Python, C/C++, HLS C, Shell, Verilog HDL, VHDL, Makefile, ARM Assembly, OpenCL, TCL
Developer Tools: Linux, Docker, Git, VS Code, Pytorch, GCC/G++, Vitis, GEM5, Verdi, VCS, ISE/Vivado, Quartus

Selected Publication

1. **Chenfeng Zhao**, Faber J, Clayton, Roger D. Chamberlain, Xuan Zhang, "HLPerf: Demystifying the Performance of HLS-based GNNs with Dataflow Architectures", Submitted to Transactions on Reconfigurable Technology and Systems, 2023.
2. **Chenfeng Zhao**, Zehao Dong, YiXin Chen, Xuan Zhang, Roger D. Chamberlain, "GNNHLS: Evaluating Graph Neural Network Inference via High-Level Synthesis", IEEE International Conference on Computer Design (ICCD), 2023.
3. **Chenfeng Zhao**, Roger D. Chamberlain, Xuan Zhang, "SuperCut: Communication-Aware Partitioning for Near-Memory Graph Processing", Computing Frontiers (CF), 2023.
4. **Chenfeng Zhao**, Xuan Zhang, and Roger D. Chamberlain. "Executing Data Integration Effectively and Efficiently Near the Memory." IEEE Design & Test (2021).
5. Darko Ivanovich, **Chenfeng Zhao**, Xuan Zhang, Roger D. Chamberlain, Amit Deliwala, Viktor Gruev, "Chip-to-chip optical data communications using polarization division multiplexing", IEEE High Performance Extreme Computing Conference (HPEC), 2020.