Cheng Fu

7655 Palmilla Drive., San Diego, CA - 92122 | cfu@ucsd.edu | +1 (734) 747-3638

Objective

Seeking for internship opportunities in summer 2019 in machine learning, computer hardware and RTL design.

Education

Ph.D Computer Science & Engineering *Sep 2018 - Present*
The University of California, San Diego, San Diego, CA
M.S. Electrical & Computer Engineering, VLSI track — GPA 4.0/4.0 *Sep 2016 - Apr 2018*
The University of Michigan, Ann arbor, MI
B.S. Information Engineering — GPA 90/100 (3.8/4.0) *Sep 2012 - Jul 2016*
Beijing Institute of Technology, Beijing, China

Internship

Iluvatar CoreX, San Jose — HLS Designer *May 2018 - Sep 2018*

- Designed a binarized neural network accelerator on Zynq board. The prototype is implemented by using high-level synthesize programming and Xilinx SdSoC tool. Exploited weight and input similarity to reduce energy and achieved speedup. The paper about this topic has been submitted to FPGA2019.

Projects

DESIGN & IMPLEMENT N-WAY SUPERSCALAR MIPS R10K PROCESSOR *Sep 2016 - Dec 2016*

- The processor is based on MIPS R10K architecture. A series of additional features, including parameterized superscalar width, stride instruction prefetching, multi-banked associative D-cache, Branch Target Buffer, and LSQ supporting store-load forwarding is implemented.

SPARSE-LUT: AN AREA-EFFICIENT ARCHITECTURE FOR FPGAs *Aug 2015 - Oct 2015*

- Designed new architecture of LUT (Sparse-LUT) by replacing SRAM cells with static logic values 0 or 1
- Introduced new technology mapping algorithm to accommodate the new architecture to the design flow; Benchmark demonstrated an average of 12 % improvement in logic area

DESIGN & TEST LOGICORE IP CIC & FIR COMPILER CORE *Aug 2015 - Oct 2015*

- Designed the circuit architecture of CIC and FIR filter based on their function. Implemented testing circuits of different IP cores under parameters.

DESIGN A PROGRAMMABLE GALOIS FIELD PROCESSOR *Sep 2016 - Nov 2016*
Electrical and Computer Engineering, The University of Michigan

- Simulated different methods to perform finite-field arithmetic in MATLAB and implemented the demo applications for algorithms in performing ECC, AES and CRC. The processor can serve the needs of both error coding and cryptographic processing. Paper about this research has been accepted by *ISCA2017*.

DNN FOR PULSE SHAPE DISCRIMINATION ON FPGA *Jan 2017 - Dec 2017*

- Designed recurrent and feedforward neural network algorithm to discriminate pulse shape, which achieves a fraction of misclassified neutron and piled-up pulses of approximately 1.4% and 0.6%, respectively. Implemented the new algorithm on labview FPGA for fast real-time detection, which runs at 250MHz sample rate. Paper about this research has been accepted by *Annals of Nuclear Energy journal*.

DESIGN & IMPLEMENT A SPARSE DNN ACCELERATOR *Jan 2018 - Present*

- Implementing a novel DNN inference accelerator that can stitch together sparse data from both weight and input activations for parallel execution.

Skills

Programming: Verilog, C/C++, Python, Java, Matlab, Bash Script, Javascript, Assembly
Tools/Simulators: VCS, Cadence, Quartus, Vivado, Labview, pthread, Gem5, LLVM
Machine Learning Library: Tensorflow, Pytorch, Matlab NN toolbox