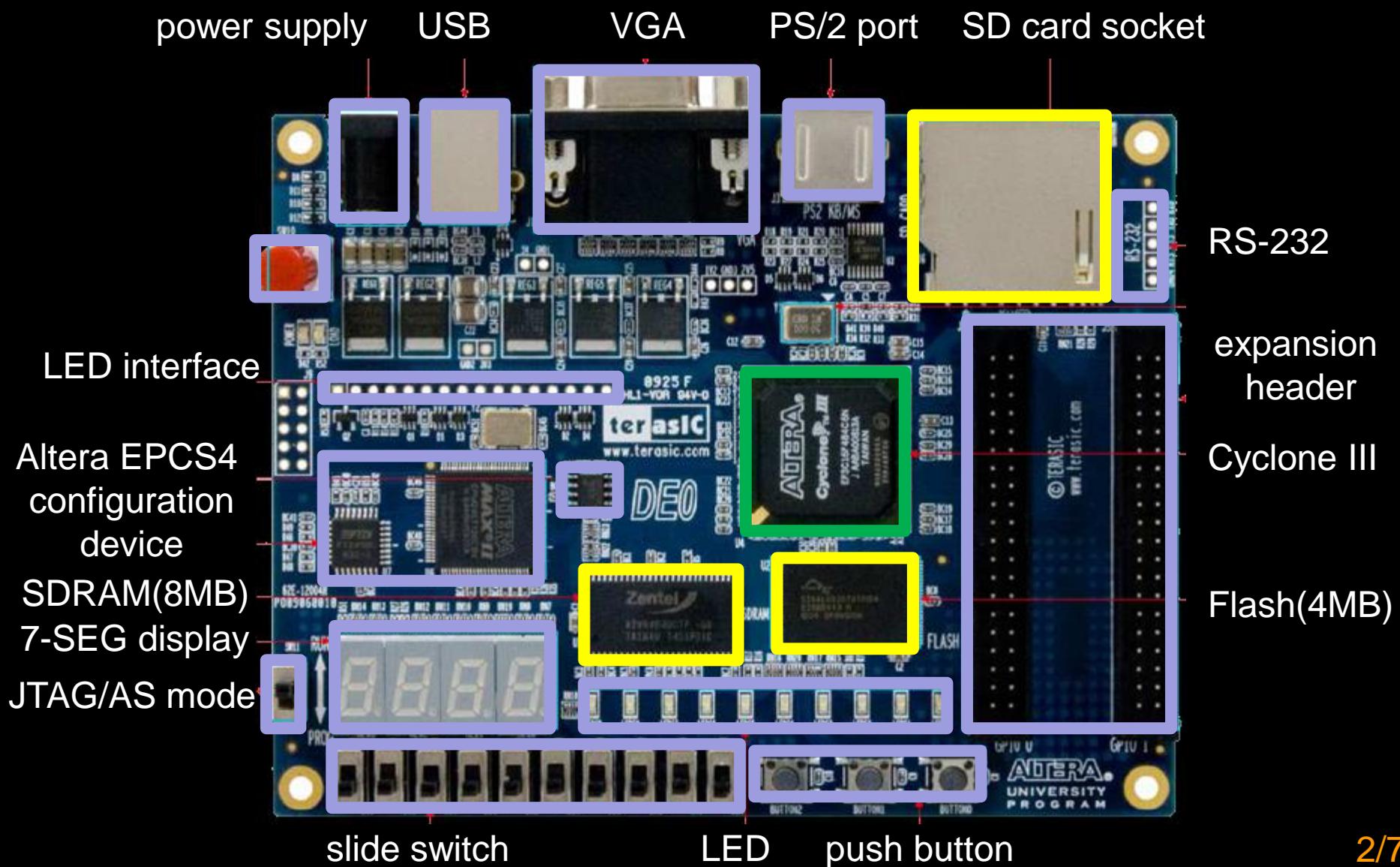


# FPGA Design Tutorial

# Outline

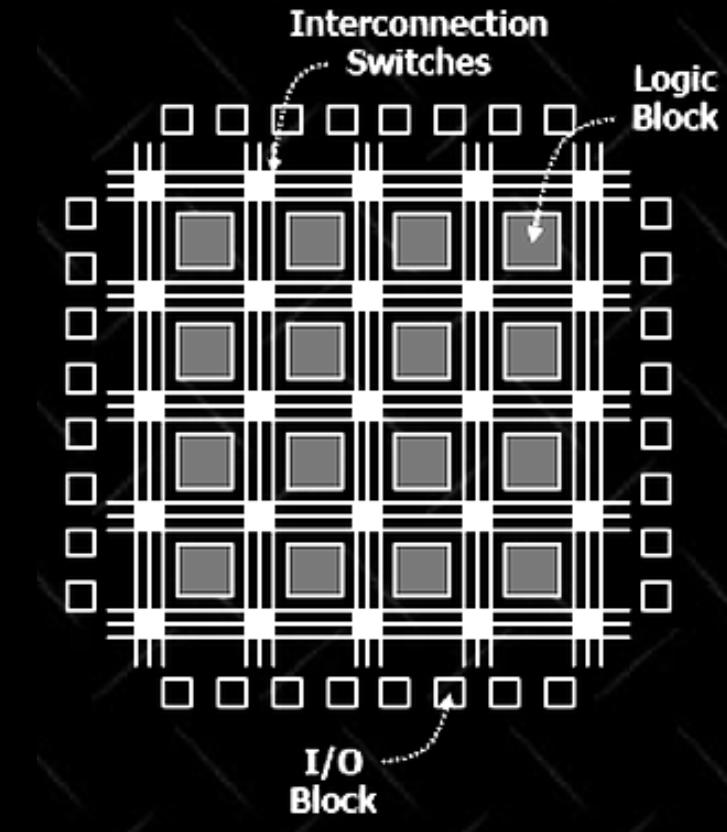
- **Introduction - Altera DE0 FPGA Board**
- **FPGA Design with Quartus II**
  - Lab1: Schematic Design Flow
  - Lab2: Dip switch to LED
  - Lab3: Binary to Decimal
  - Lab4: Lightning LED

# Layout and Component of DE0 Board

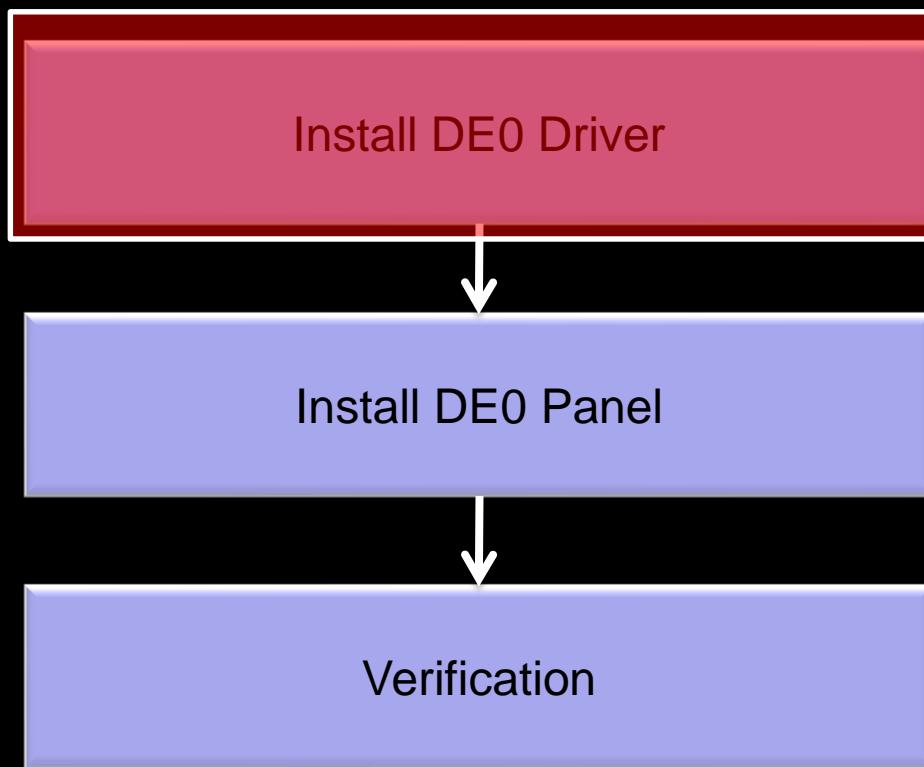


# Field-programmable Gate Array (FPGA)

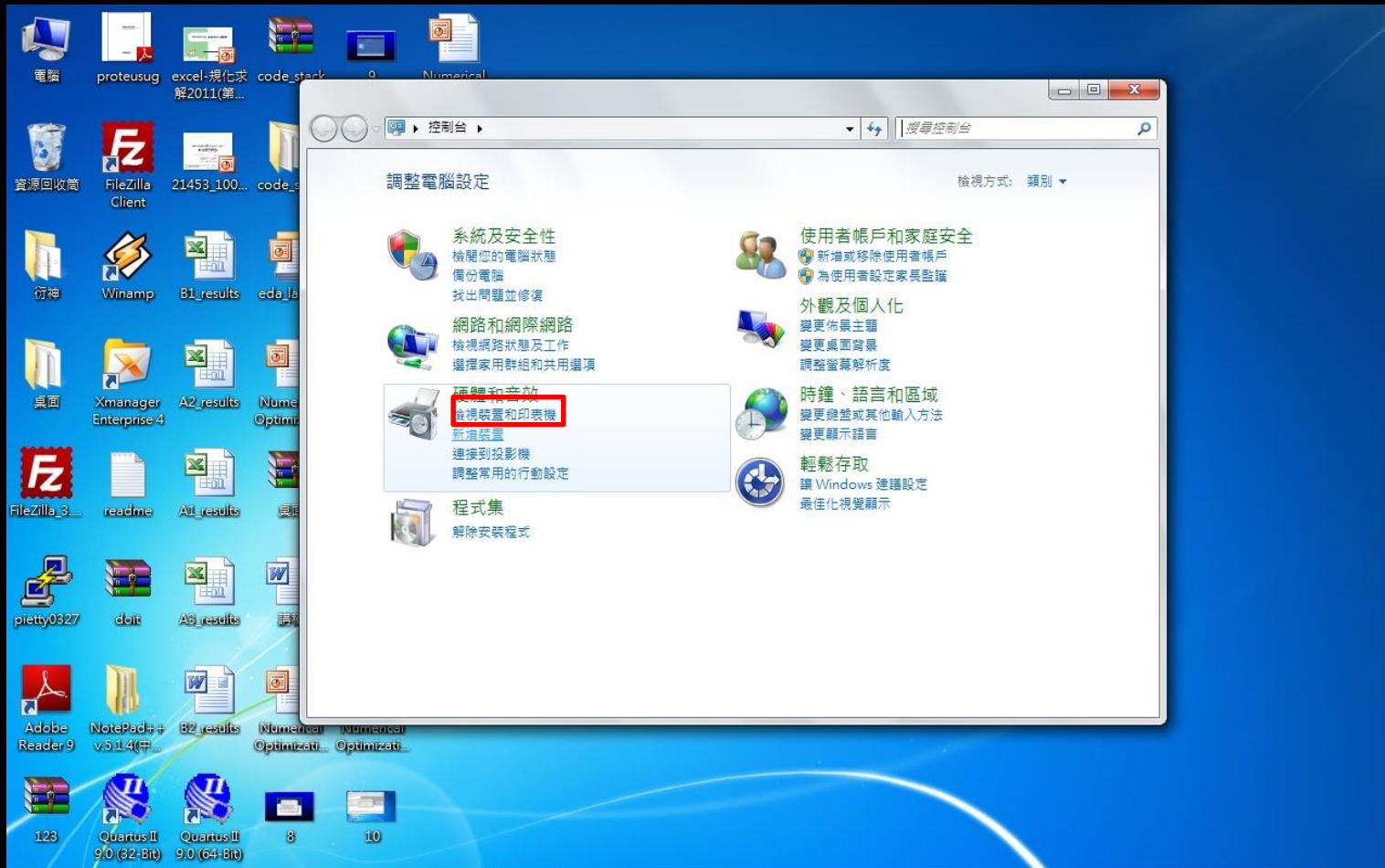
- **Advantage:**
  - Programmability
  - Short turnaround time
  - Low manufacturing cost
- **Disadvantage:**
  - Low performance
  - High power consumption
  - High unit cost
- **Why do we use FPGA for this course?**



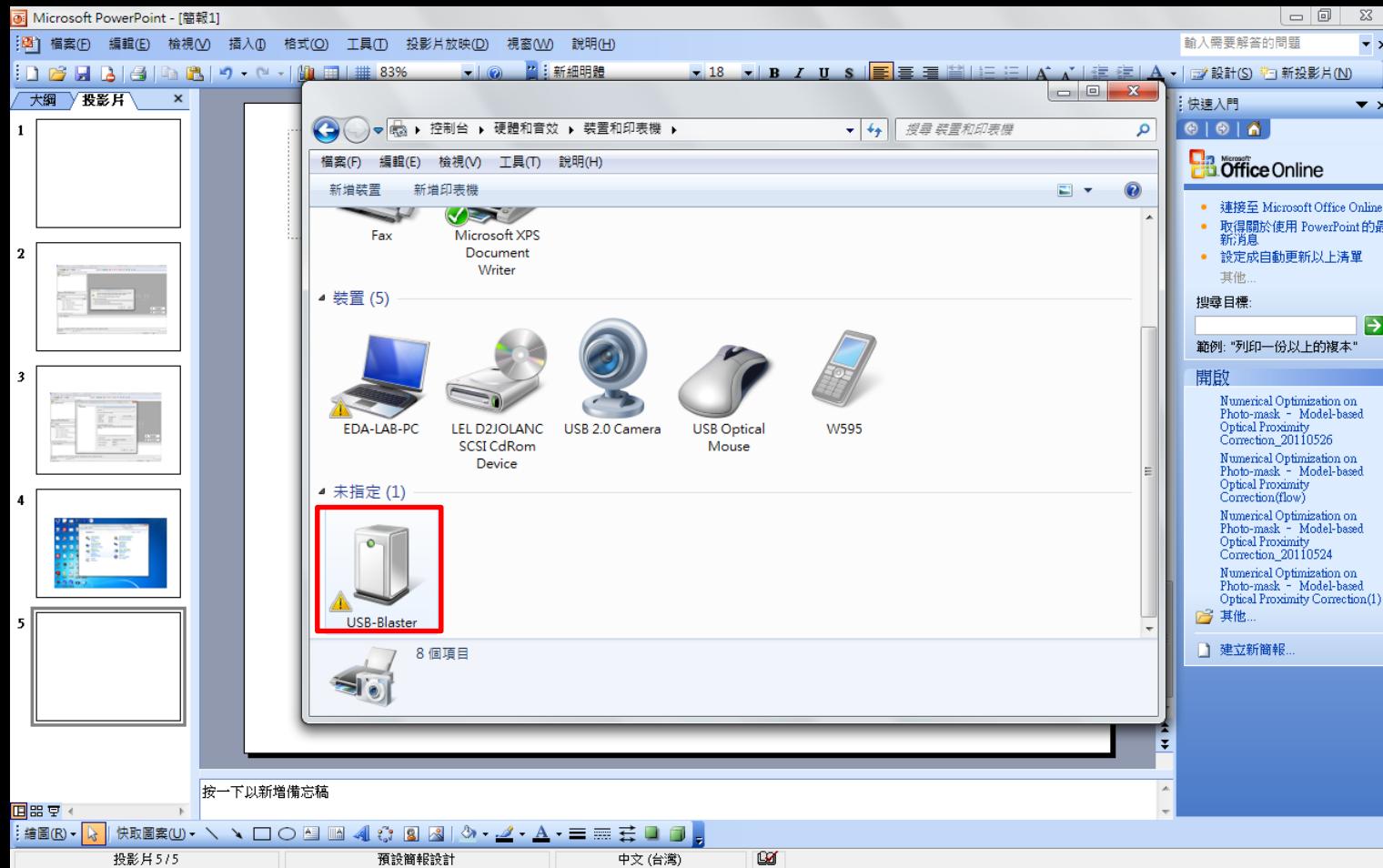
# Getting Started with Altera DE0 Board



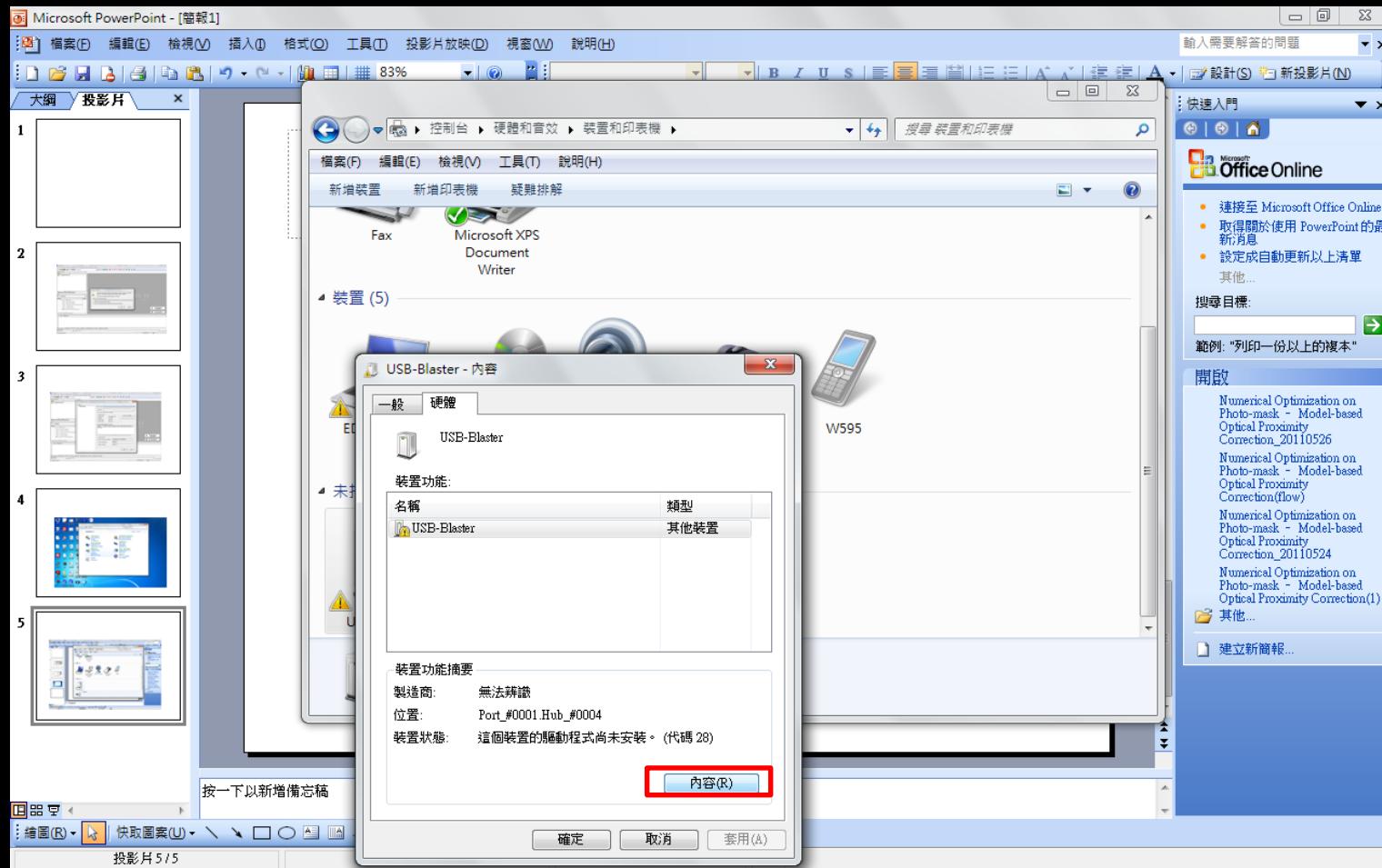
# DE0 Driver Installation (1/7)



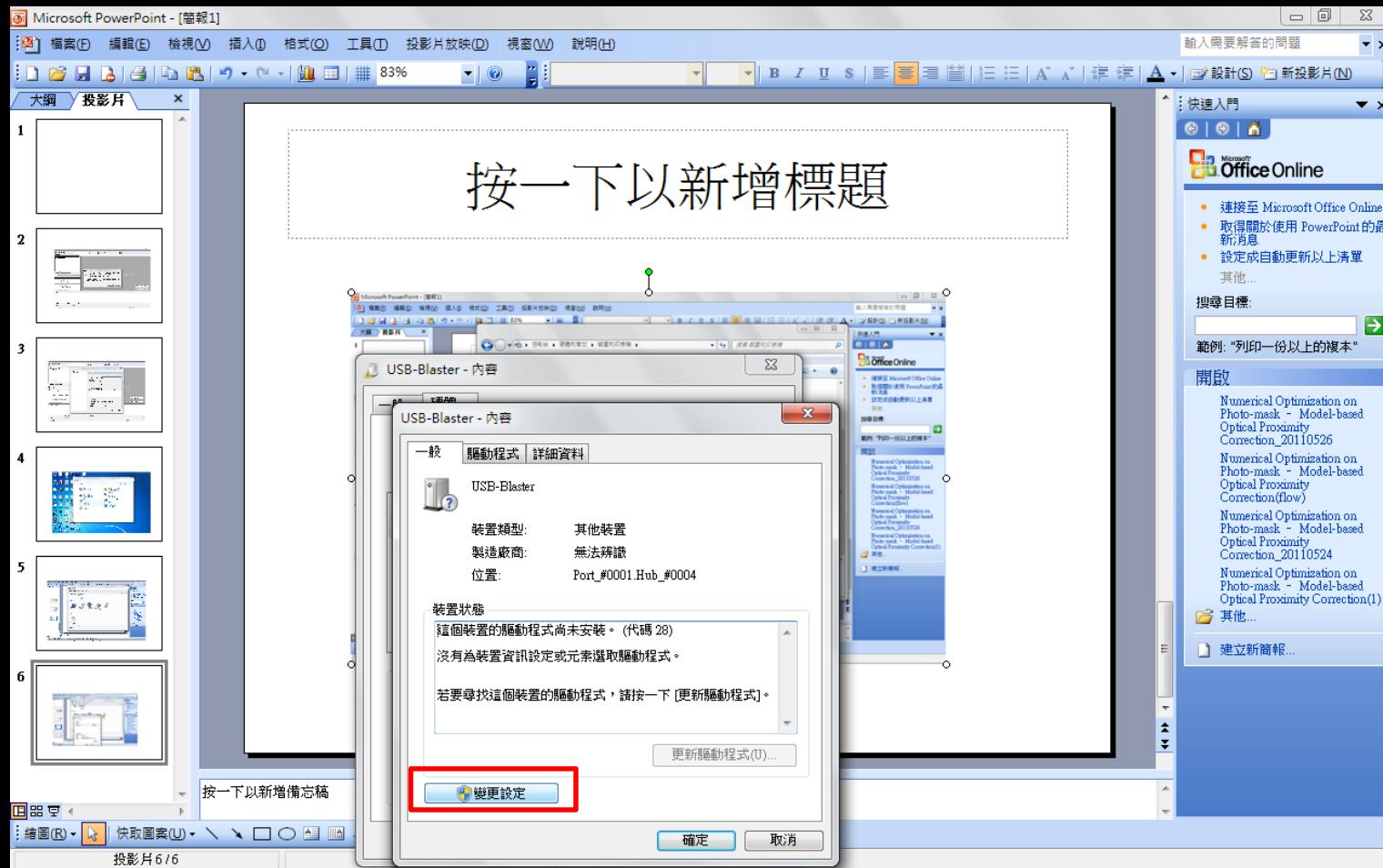
# DE0 Driver Installation (2/7)



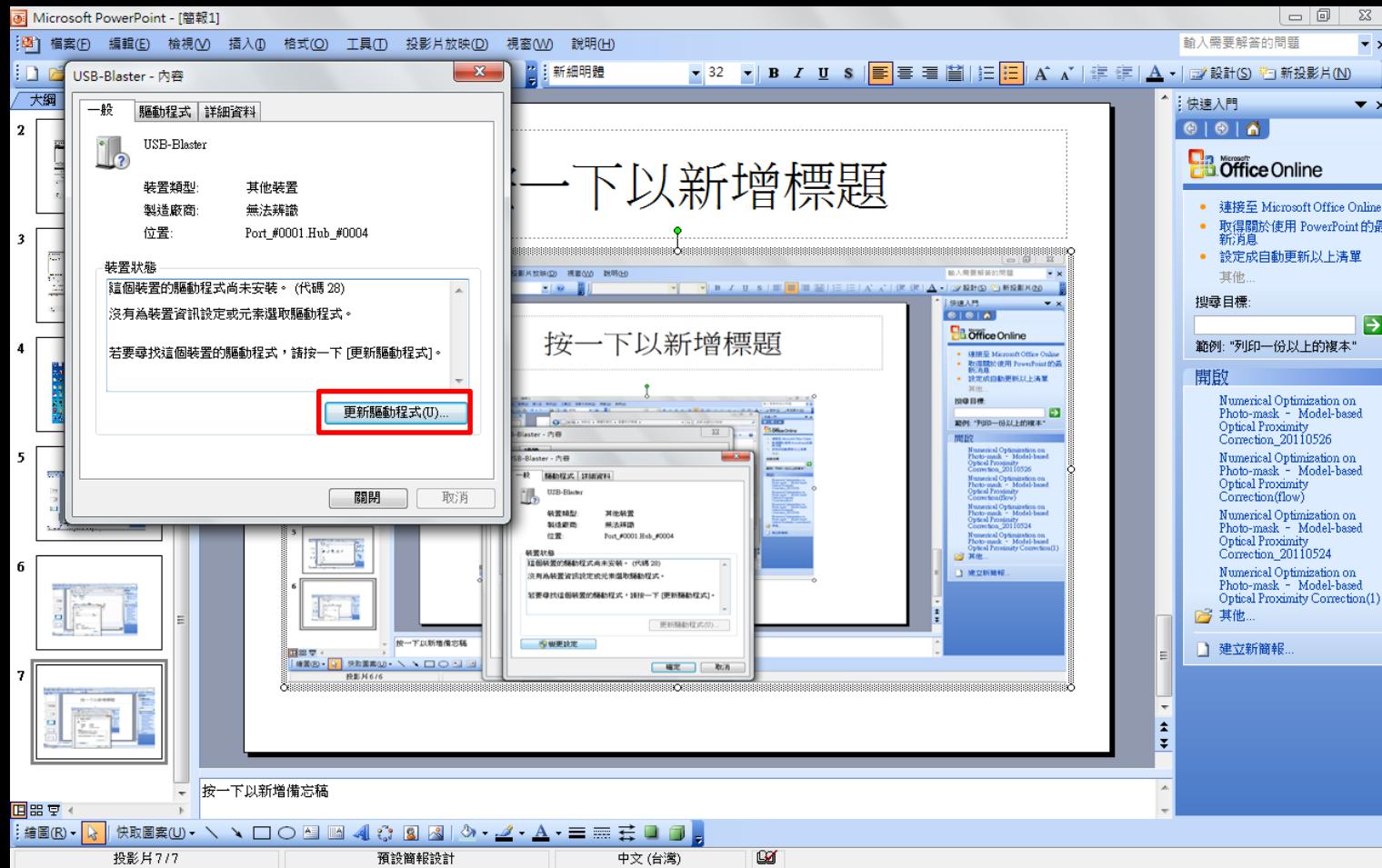
# DE0 Driver Installation (3/7)



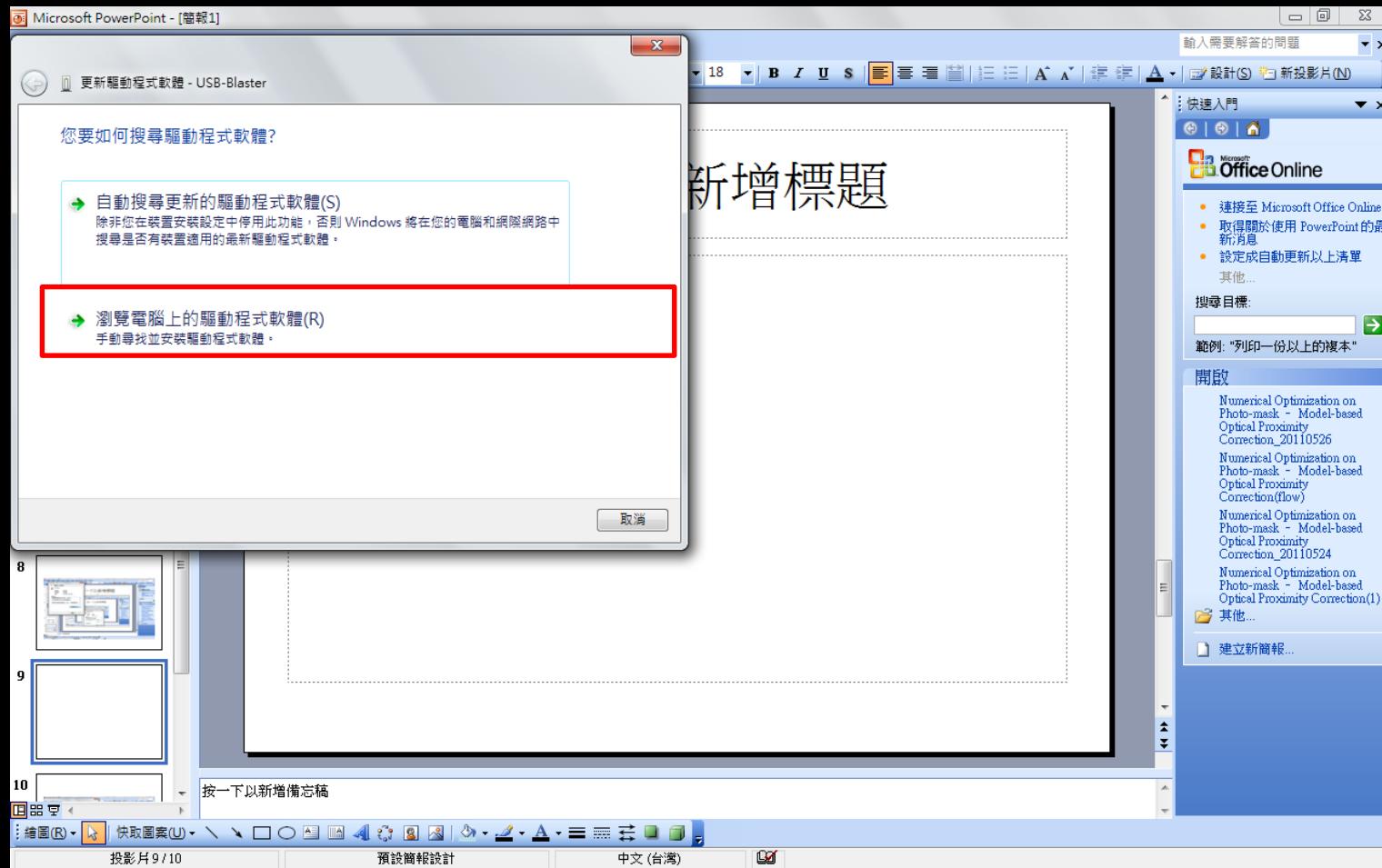
# DE0 Driver Installation (4/7)



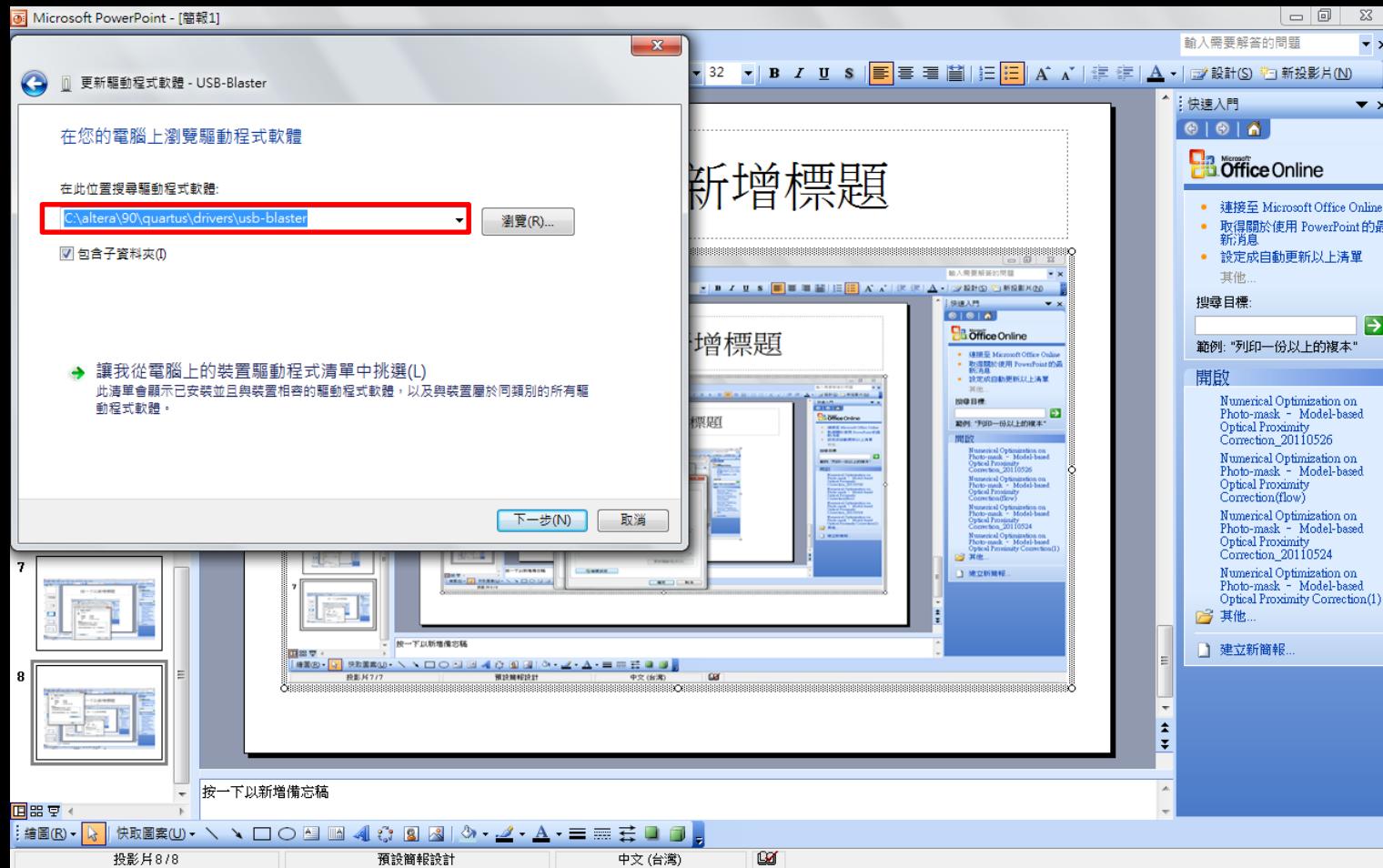
# DE0 Driver Installation (5/7)



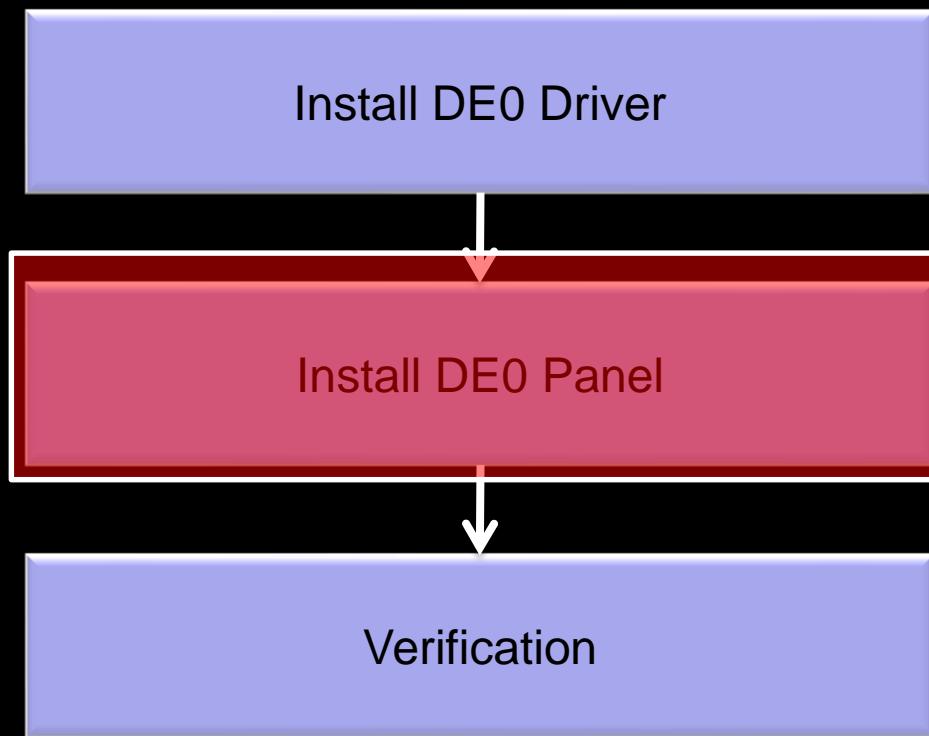
# DE0 Driver Installation (6/7)



# DE0 Driver Installation (7/7)



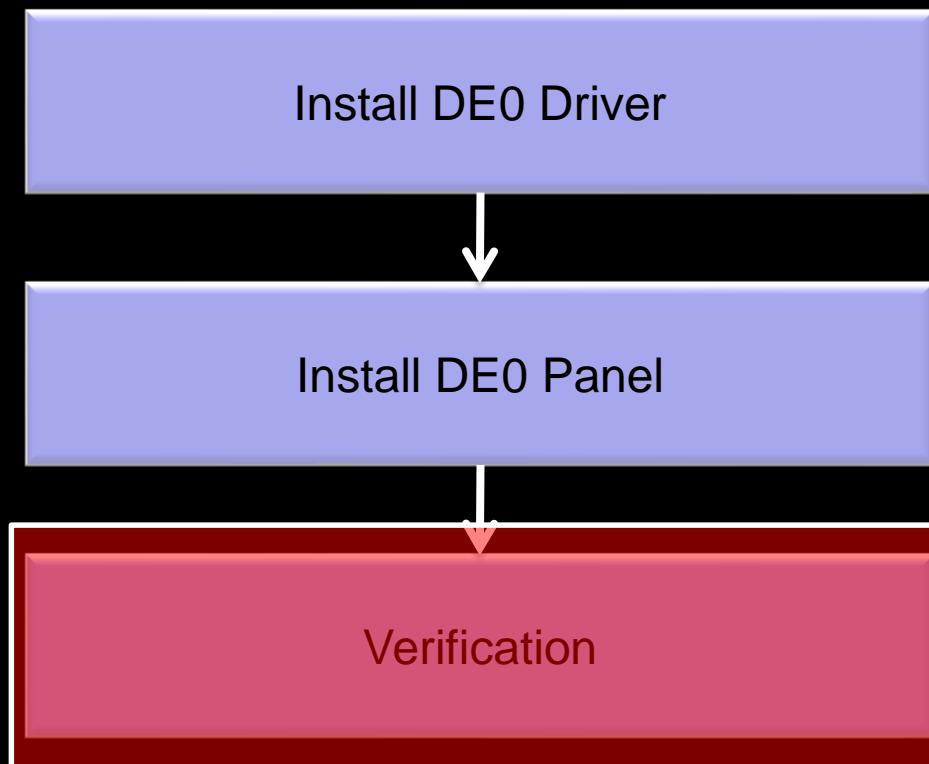
# Getting Started with Altera DE0 Board



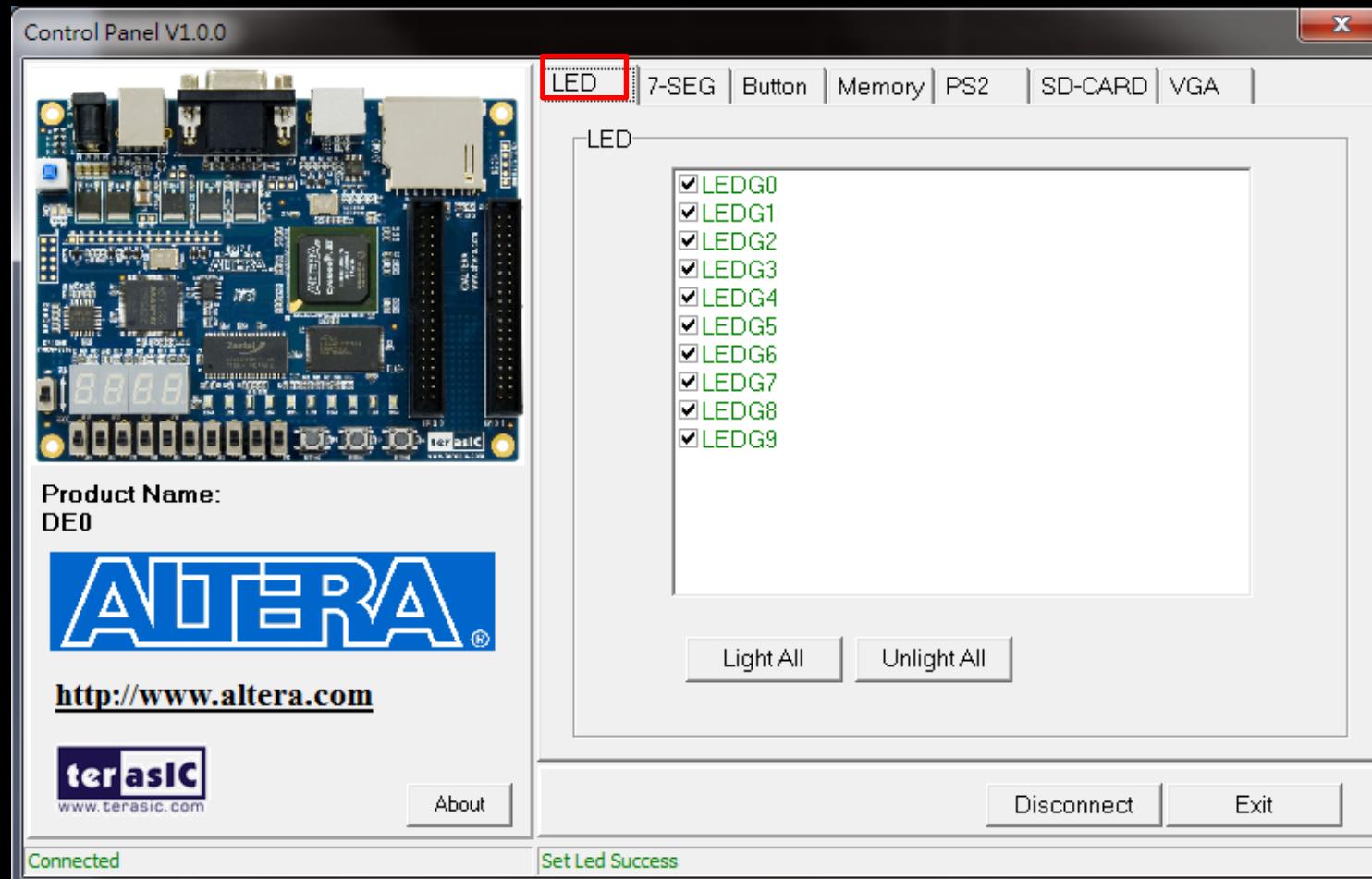
# DE0 Control Panel

- Copy the “Control\_panel” from “DE0 CD\_ROM” to C:\altera\13.1\quartus
- Copy the “jtag\_client.dll” and “dinkum\_alt.dll” from C:\altera\13.1\quartus\bin to C:\altera\13.1\quartus\Control\_panel
- Click “DE0\_ControlPanel.exe”
- Click “Connect”

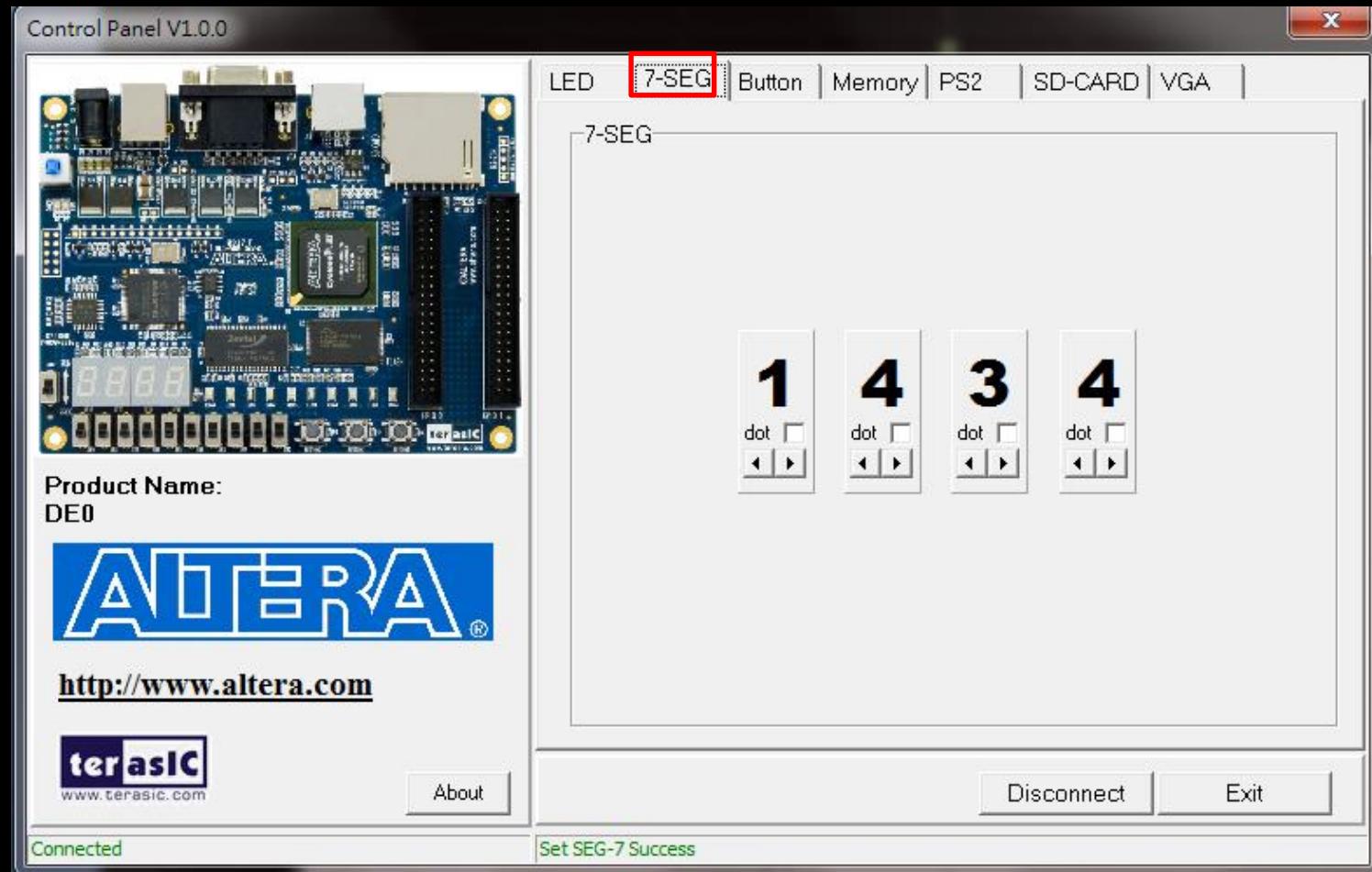
# Getting Started with Altera DE0 Board



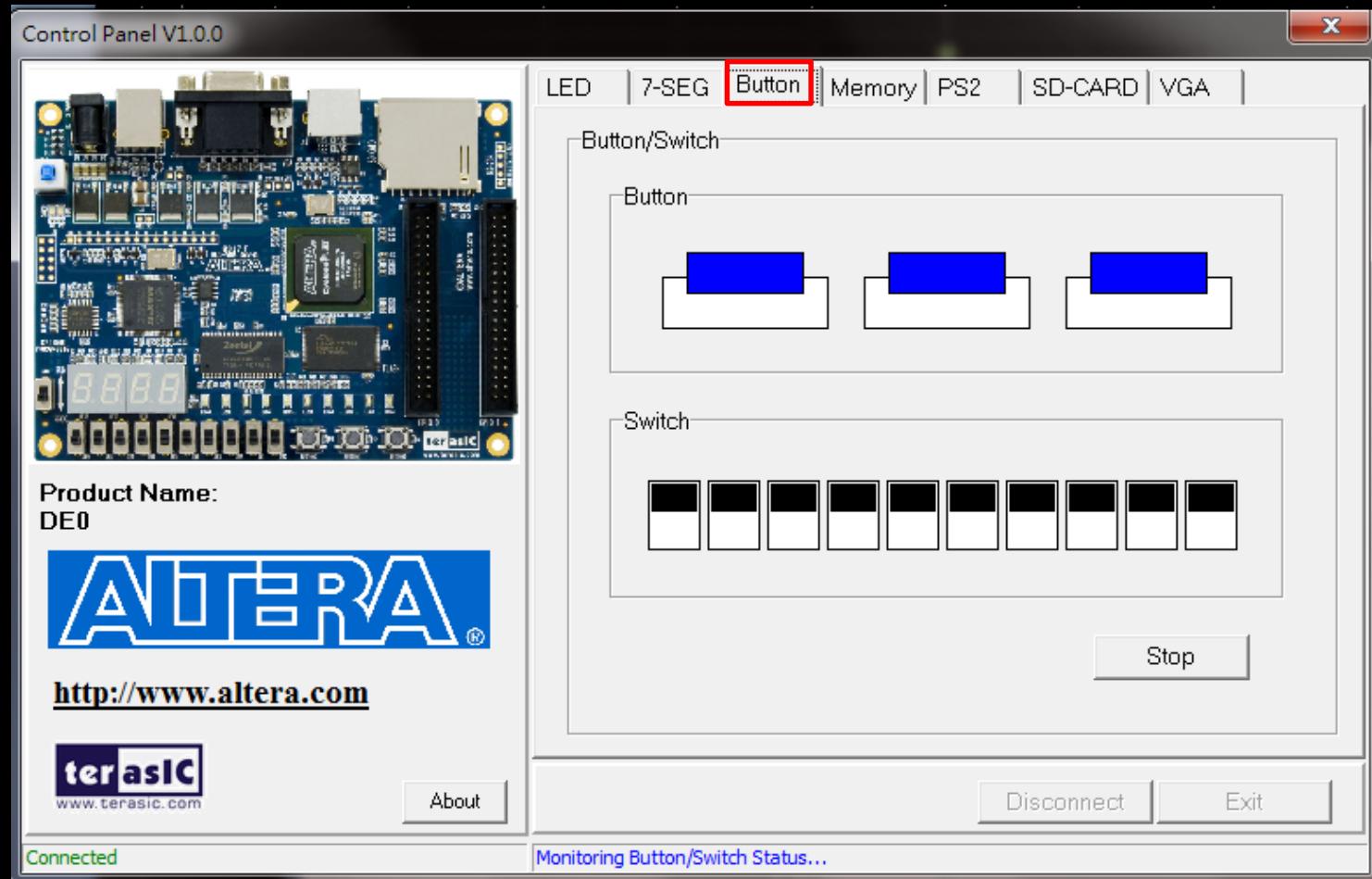
# Verification of LED



# Verification of 7-SEG



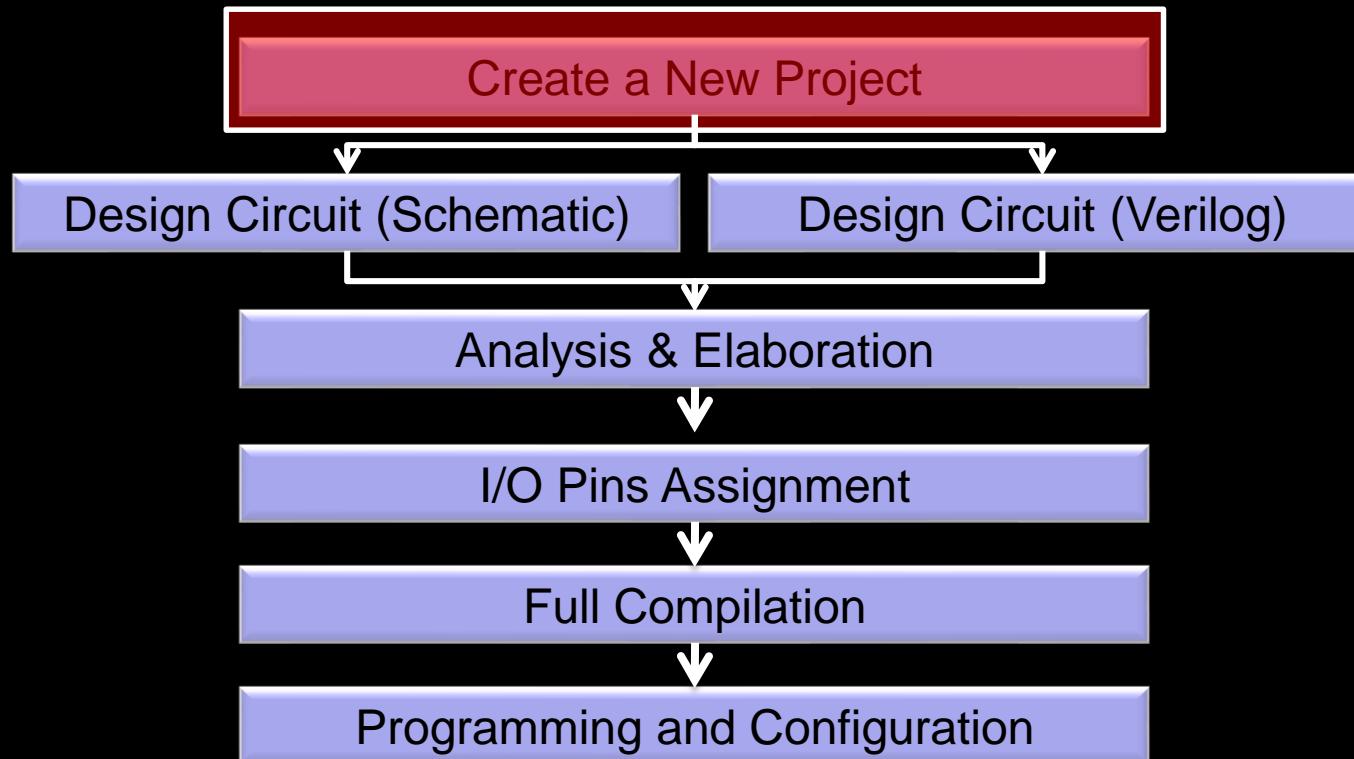
# Verification of Button



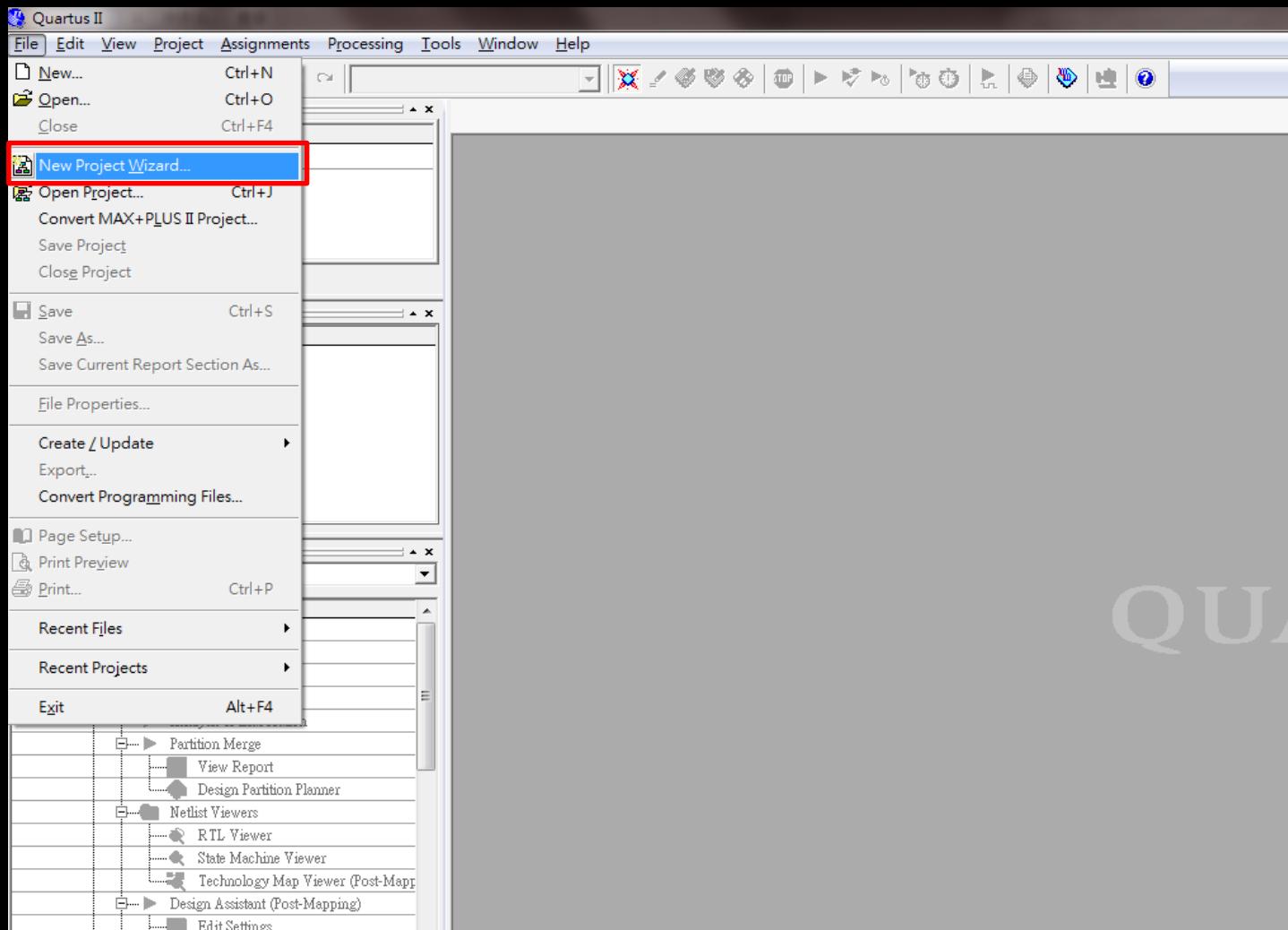
# Outline

- **Introduction - Altera DE0 FPGA Board**
- **FPGA Design with Quartus II**
  - Lab1: Schematic Design Flow
  - Lab2: Dip switch to LED
  - Lab3: Binary to Decimal
  - Lab4: Lightning LED

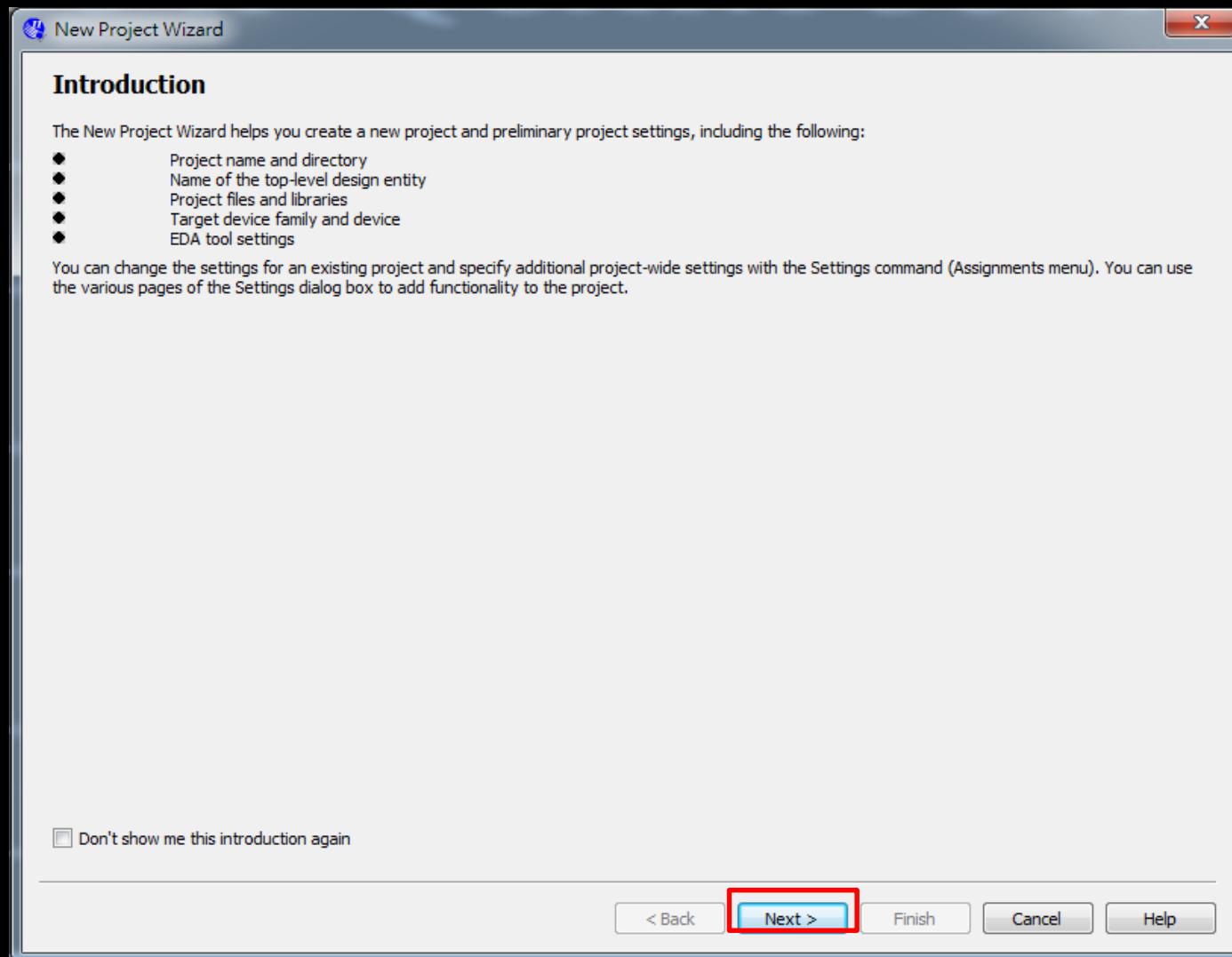
# Flow of FPGA Design with Quartus II



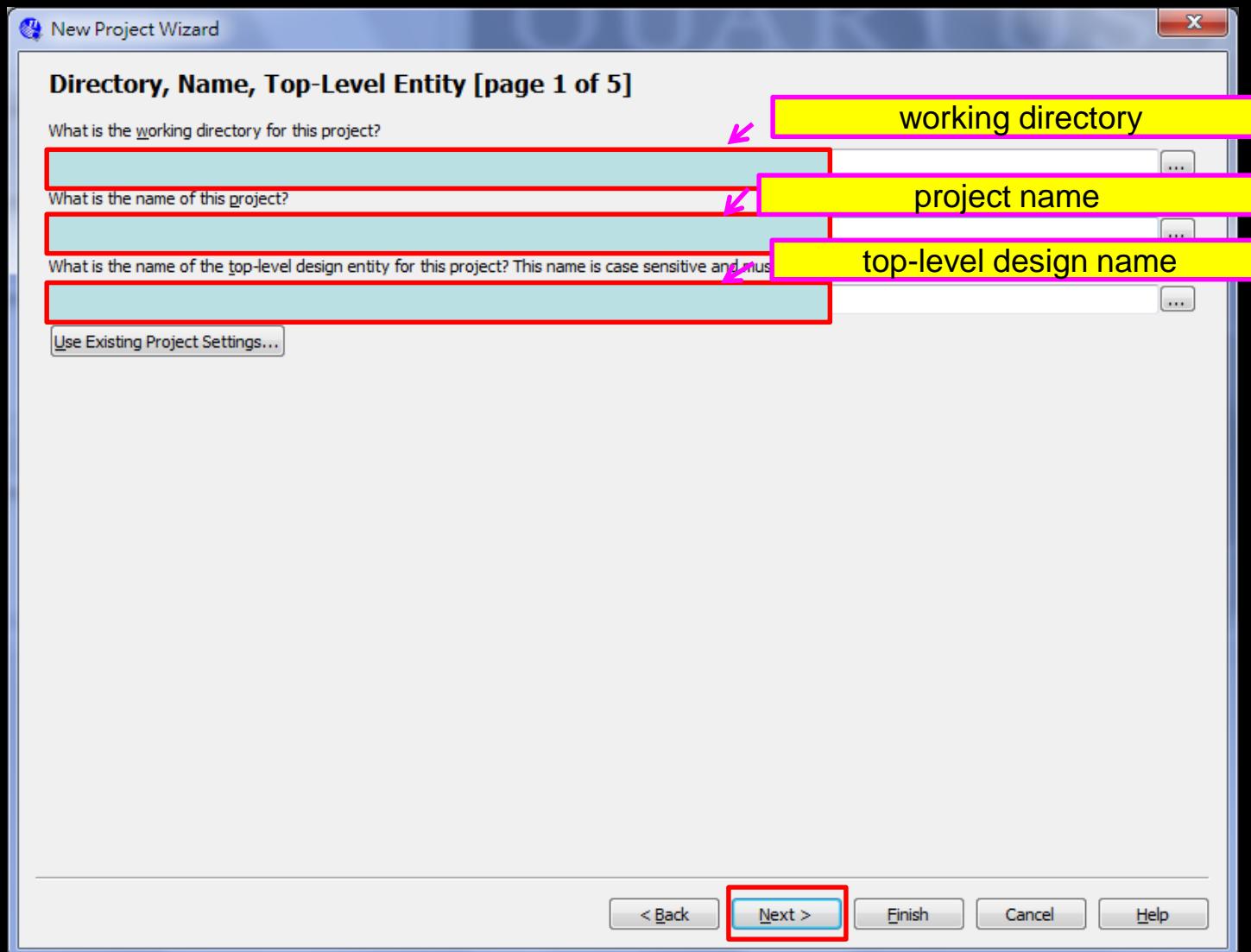
# Creating a New Project



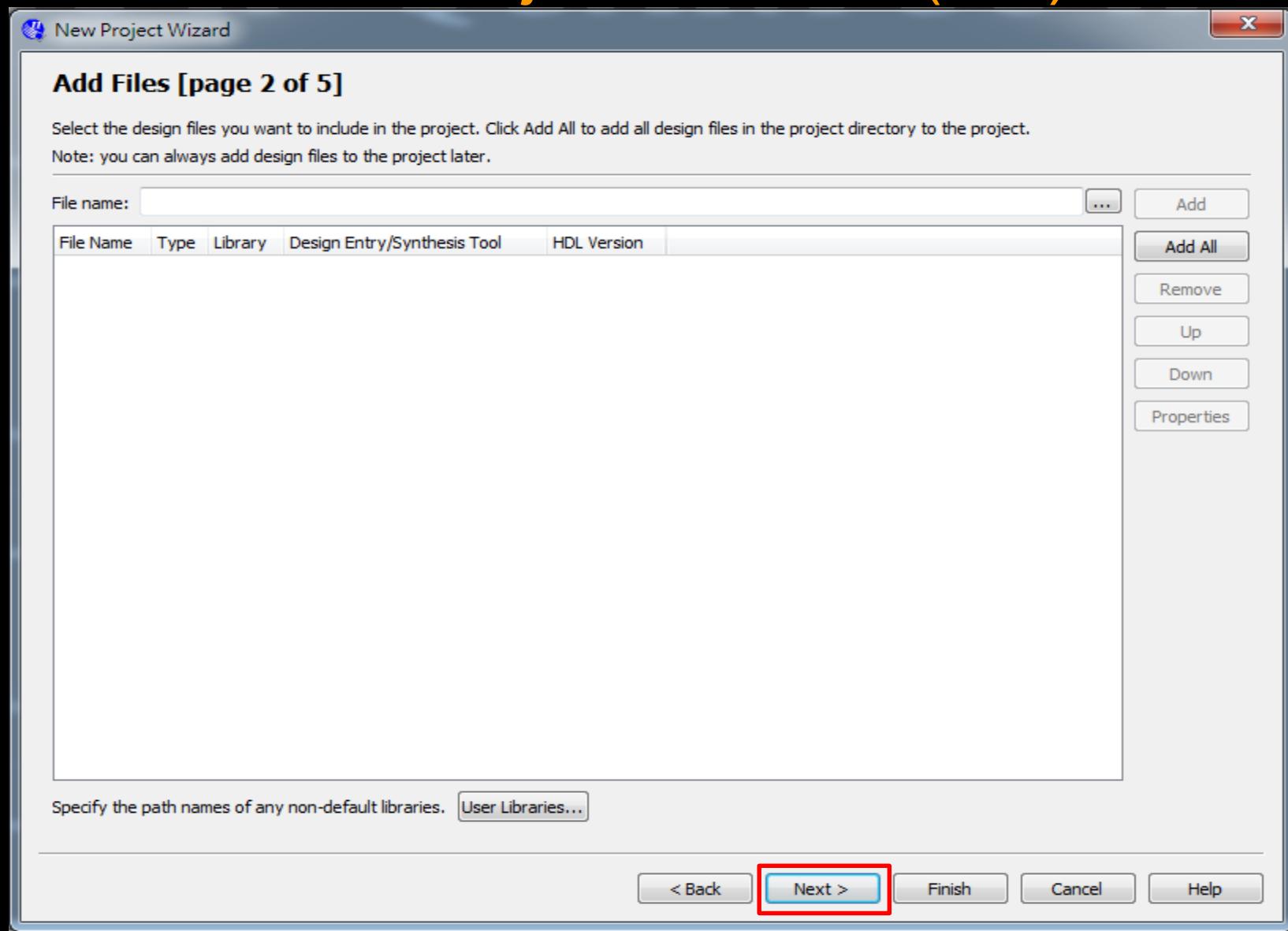
# New Project Wizard: Introduction



# New Project Wizard (1/5)



# New Project Wizard (2/5)



# New Project Wizard (3/5)

New Project Wizard

## Family & Device Settings [page 3 of 5]

Select the family and device you want to target for compilation.

Device family

Family: Cyclone III

Devices: All

Target device

Auto device selected by the Fitter

Specific device selected in 'Available devices' list

Other: n/a

Show in 'Available devices' list

Package: FBGA

Pin count: 484

Speed grade: 6

Show advanced devices

HardCopy compatible only

Available devices:

Name	Core Voltage	LCs	User I/Os	Memory Bits	Embedded multiplier 9-bit elements	PLL	Glob
EP3C16F484C6	1.2V	15408	347	516096	112	4	20
EP3C40F484C6	1.2V	39600	332	1161216	252	4	20
EP3C55F484C6	1.2V	55856	328	2396160	312	4	20
EP3C80F484C6	1.2V	81264	296	2810880	488	4	20

Companion device

HardCopy:

Limit DSP & RAM to HardCopy device resources

< Back

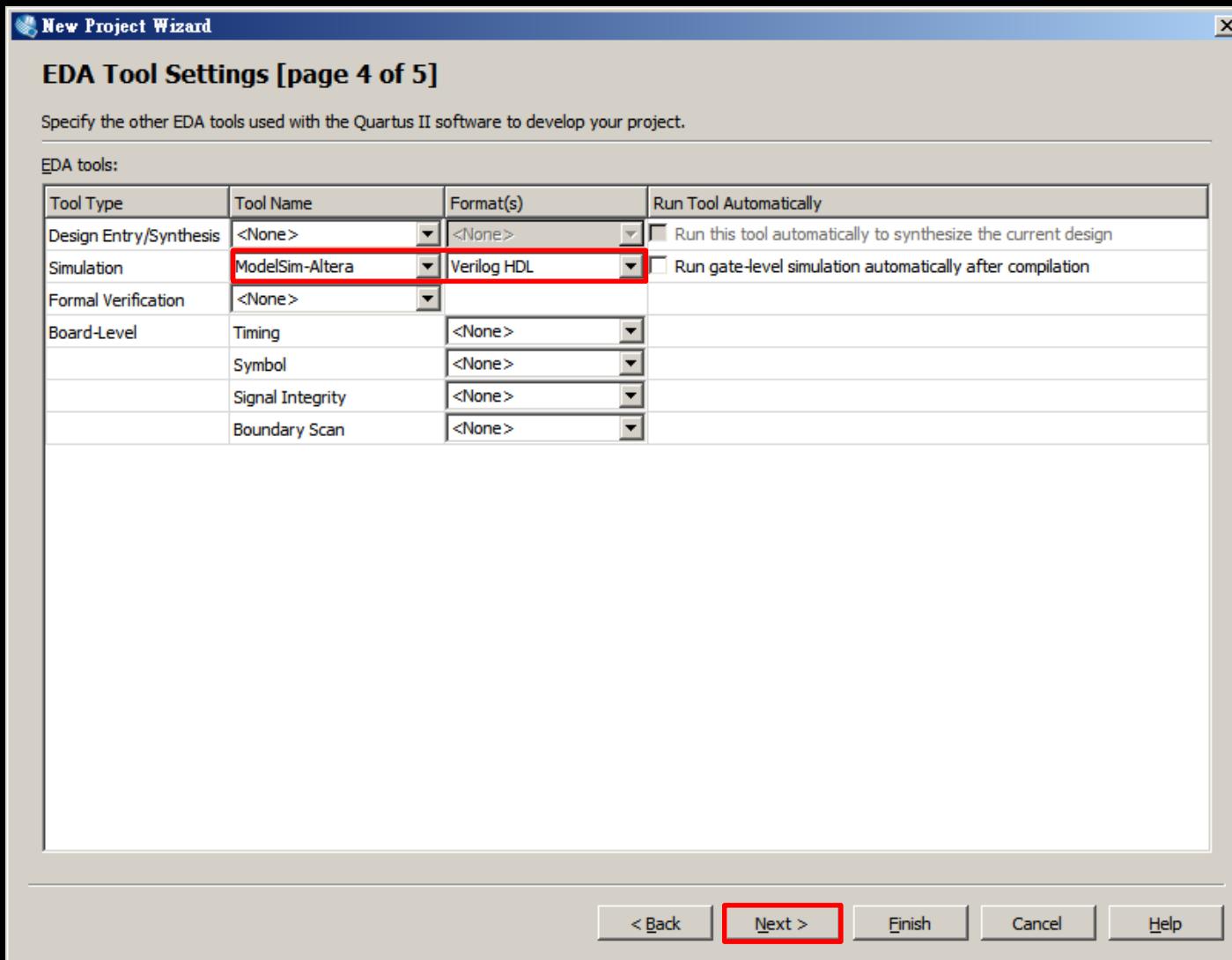
Next >

Finish

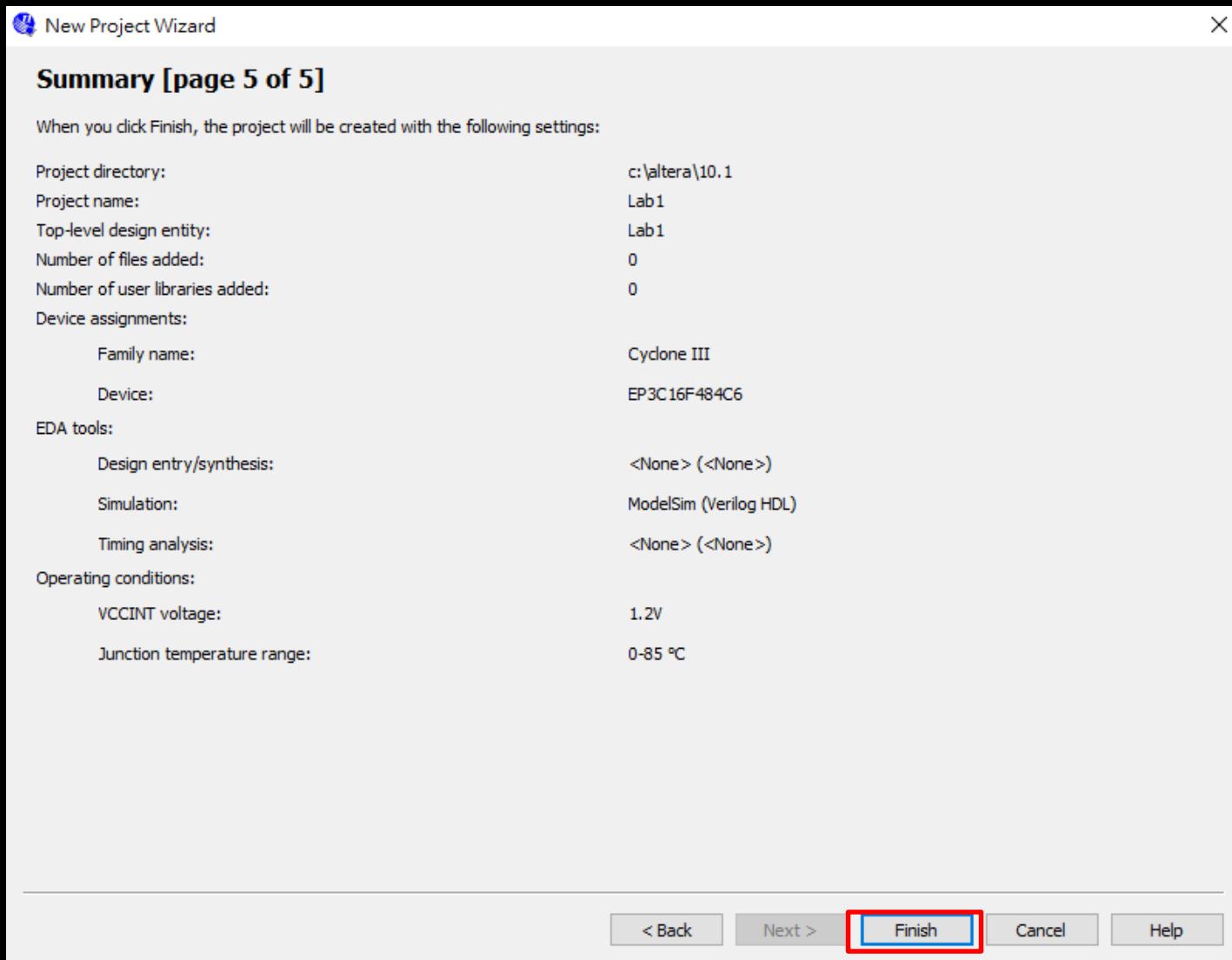
Cancel

Help

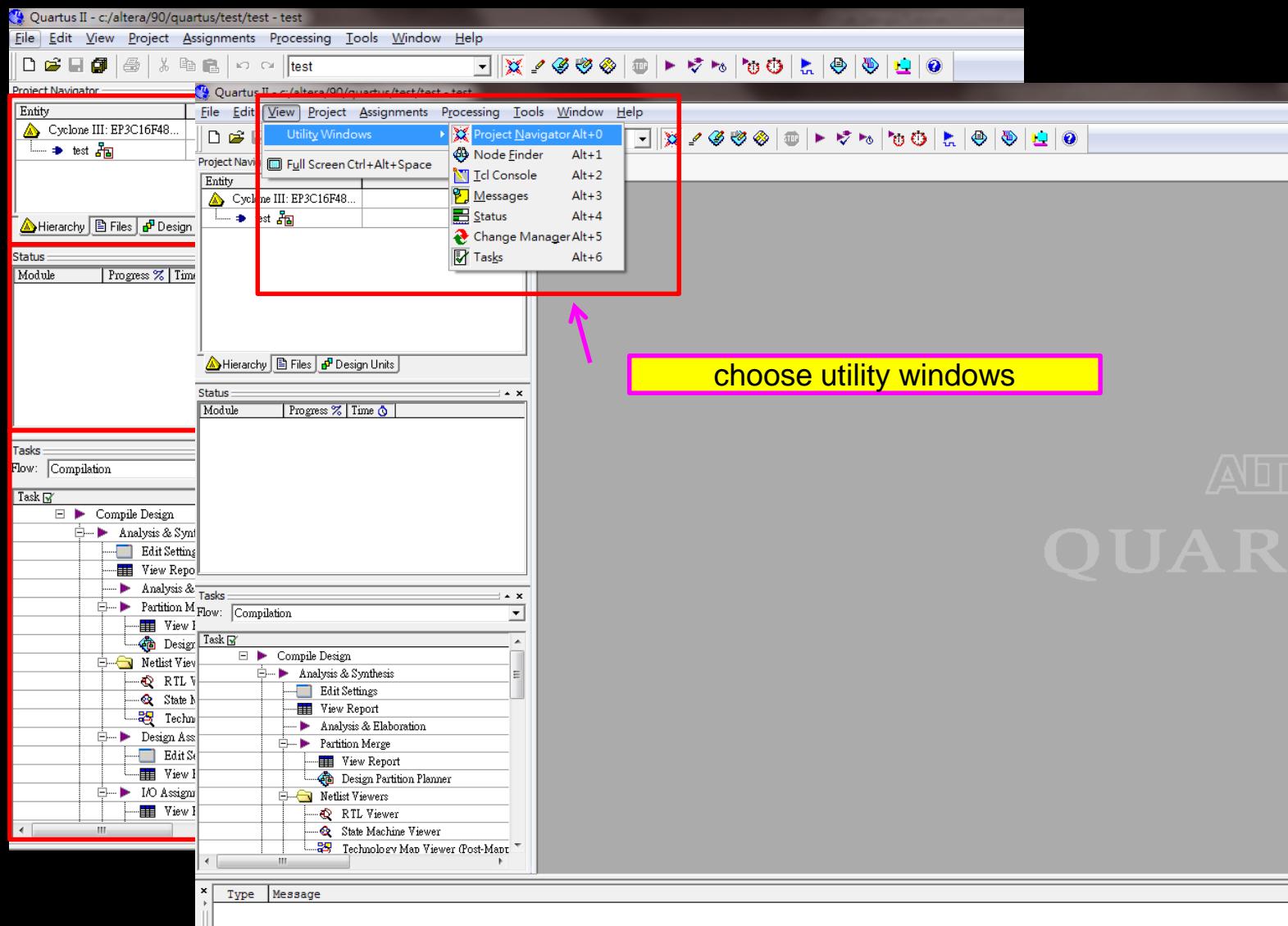
# New Project Wizard (4/5)



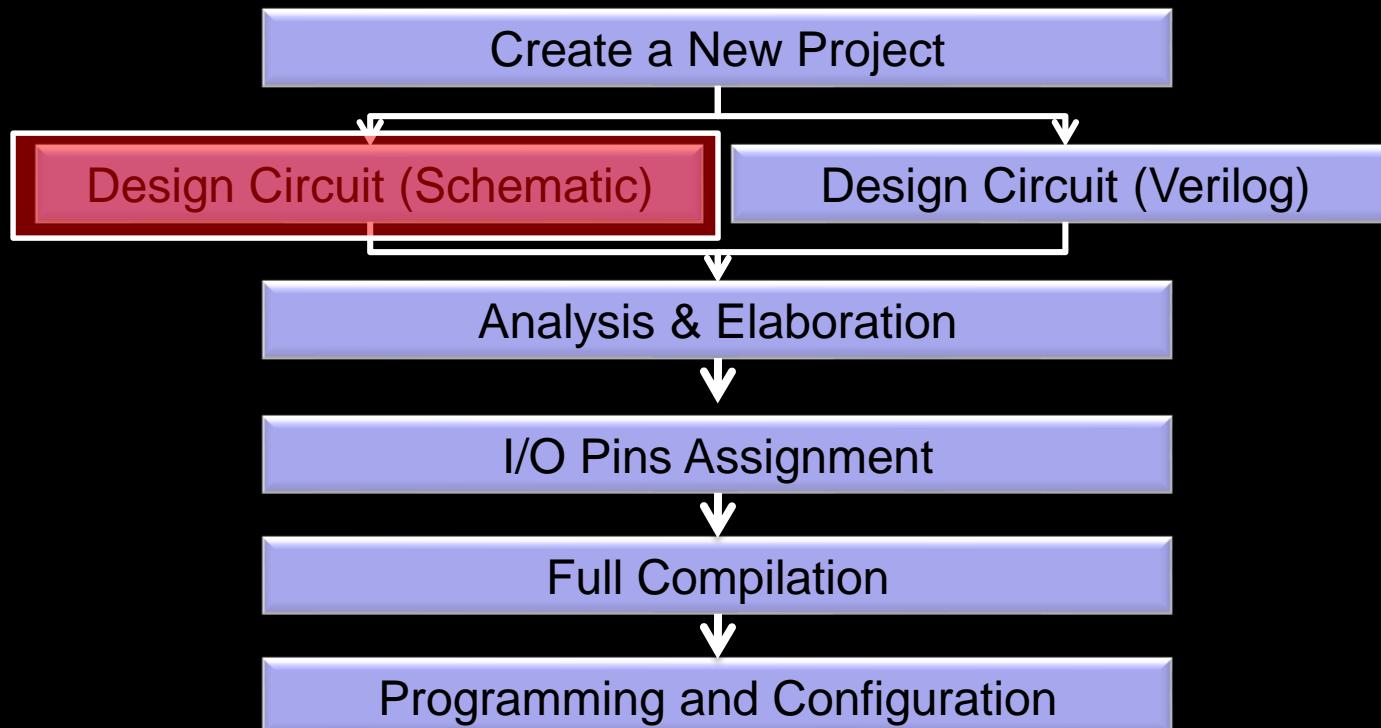
# New Project Wizard (5/5)



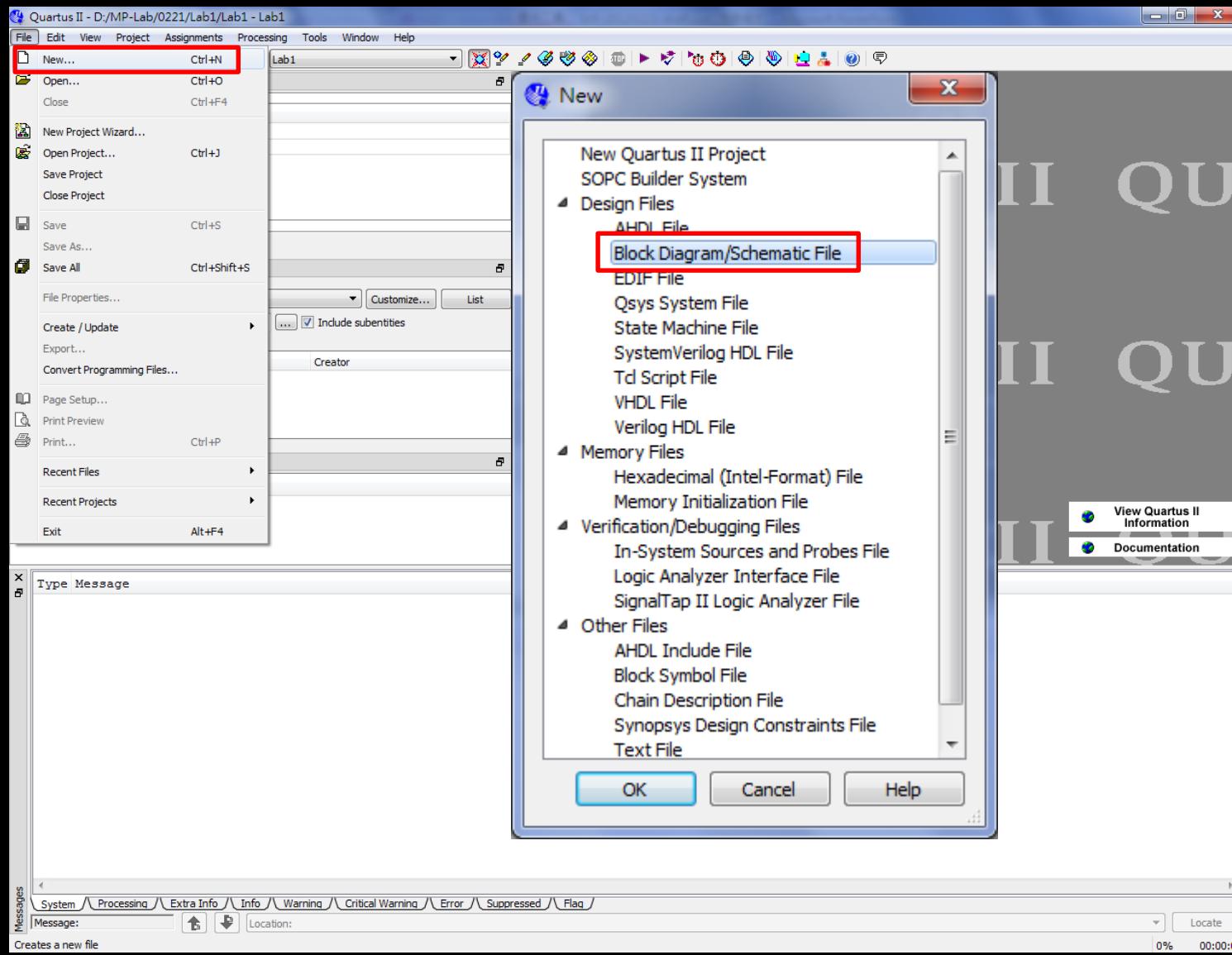
# View Utility



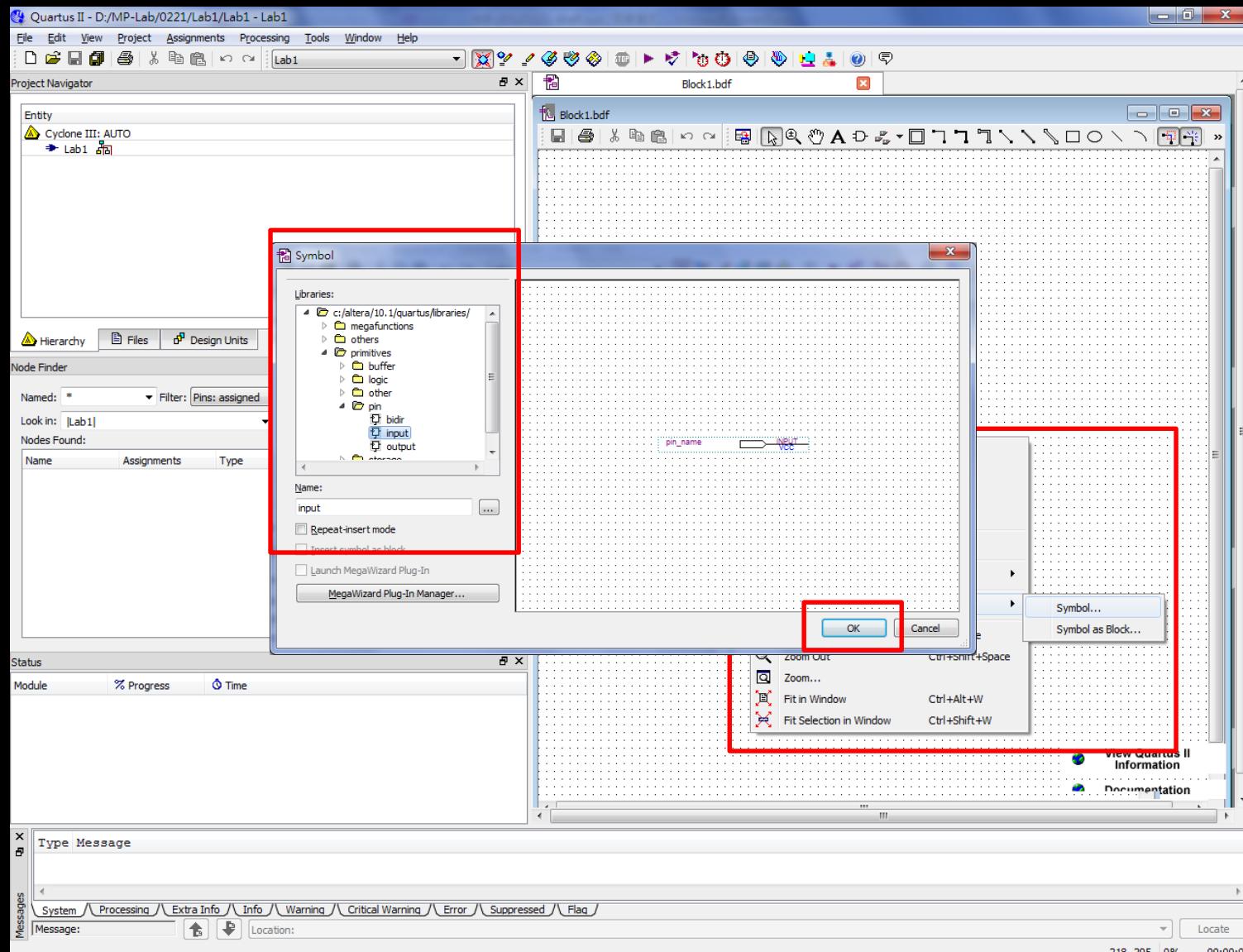
# Flow of FPGA Design with Quartus II



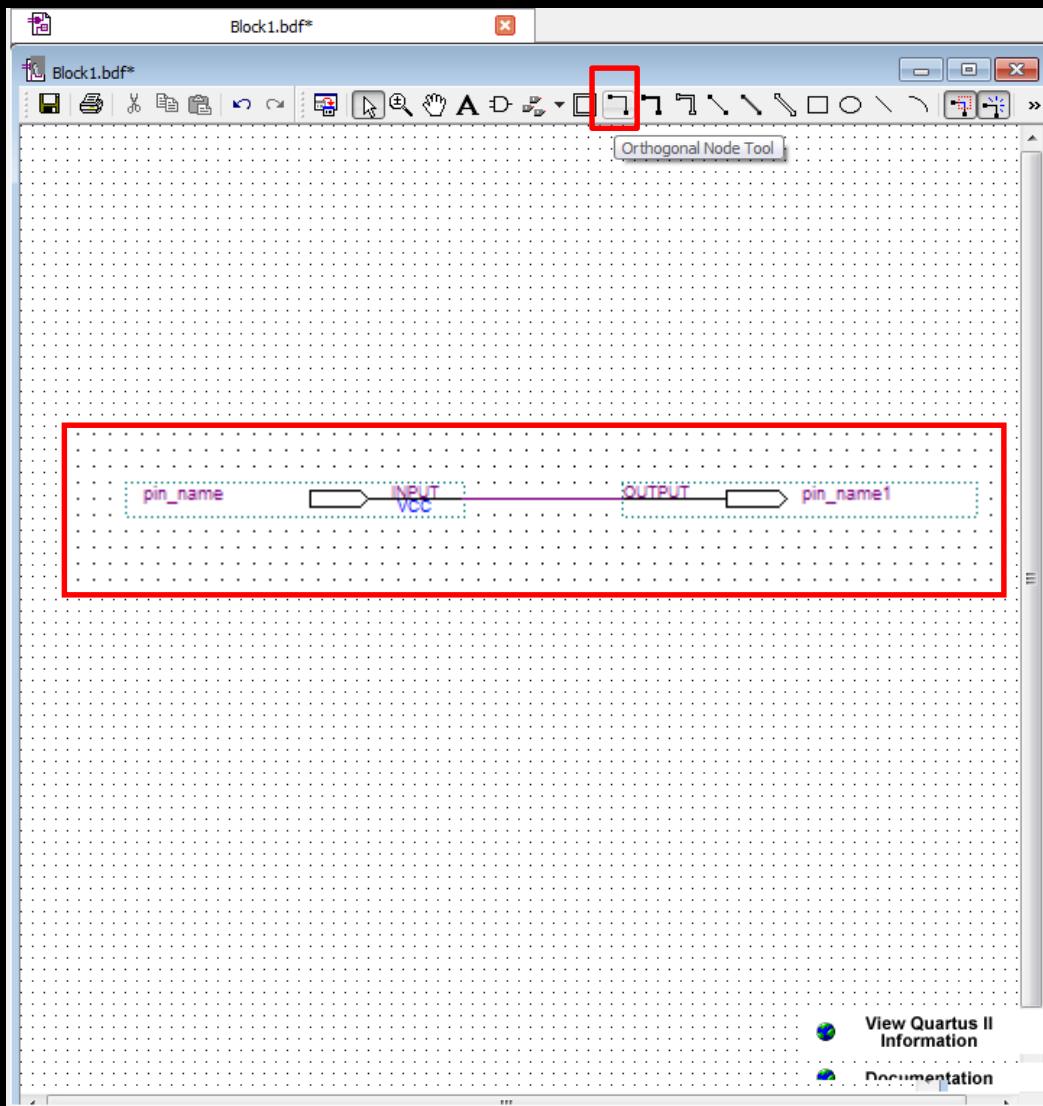
# Lab1: Create a Schematic File



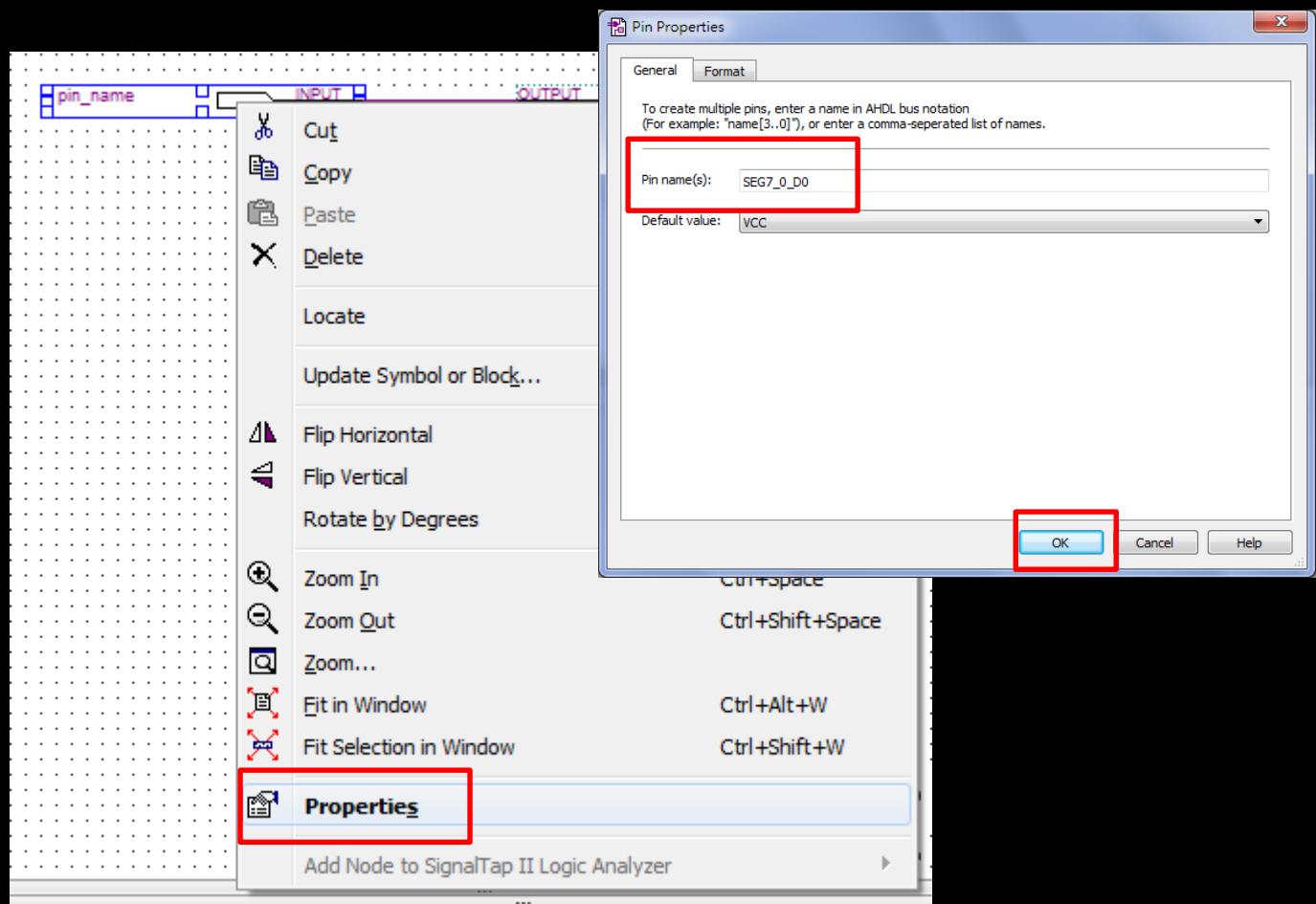
# Insert Symbols



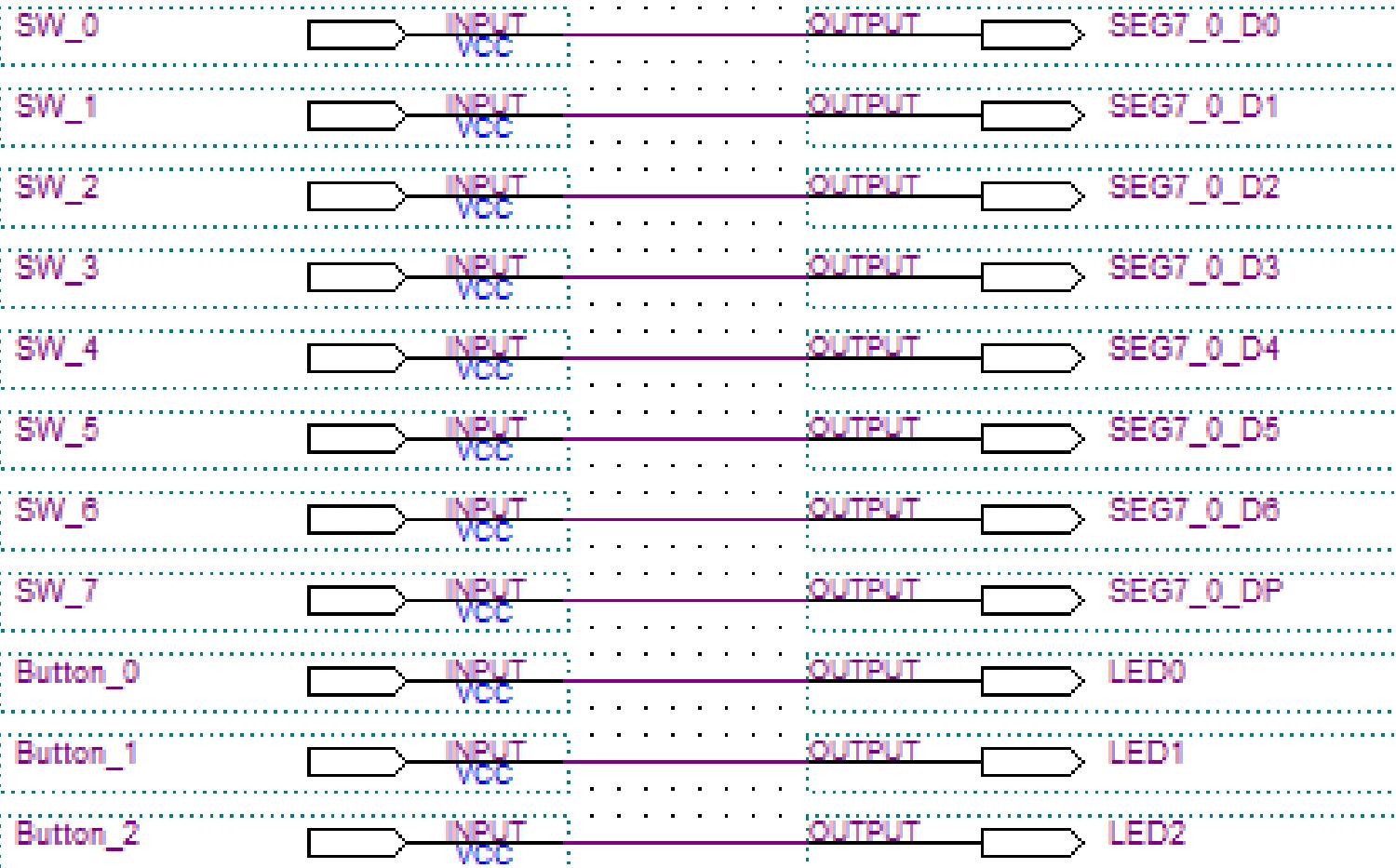
# Add Wires



# Modify Pin Names



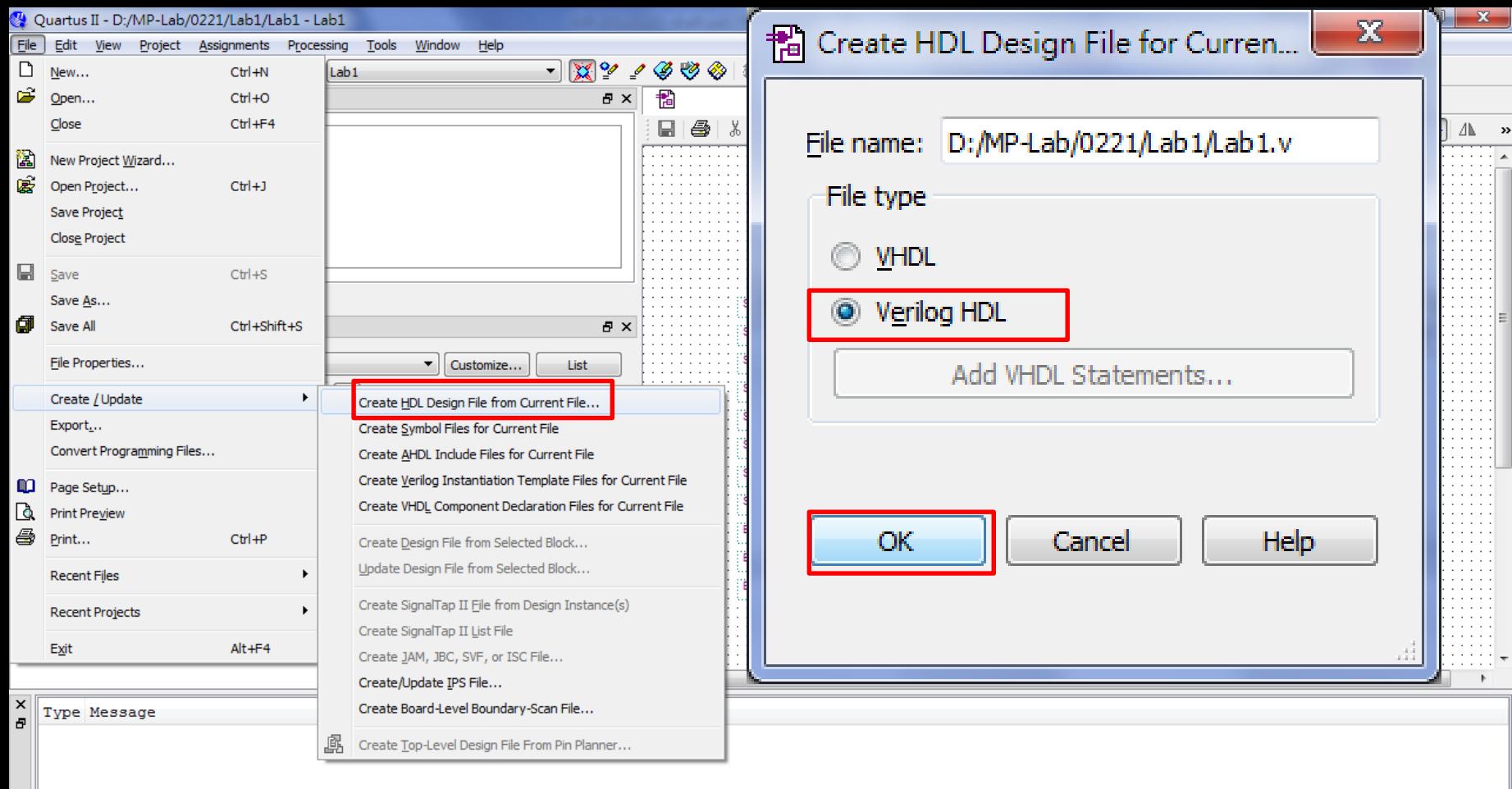
# Schematic Design Result



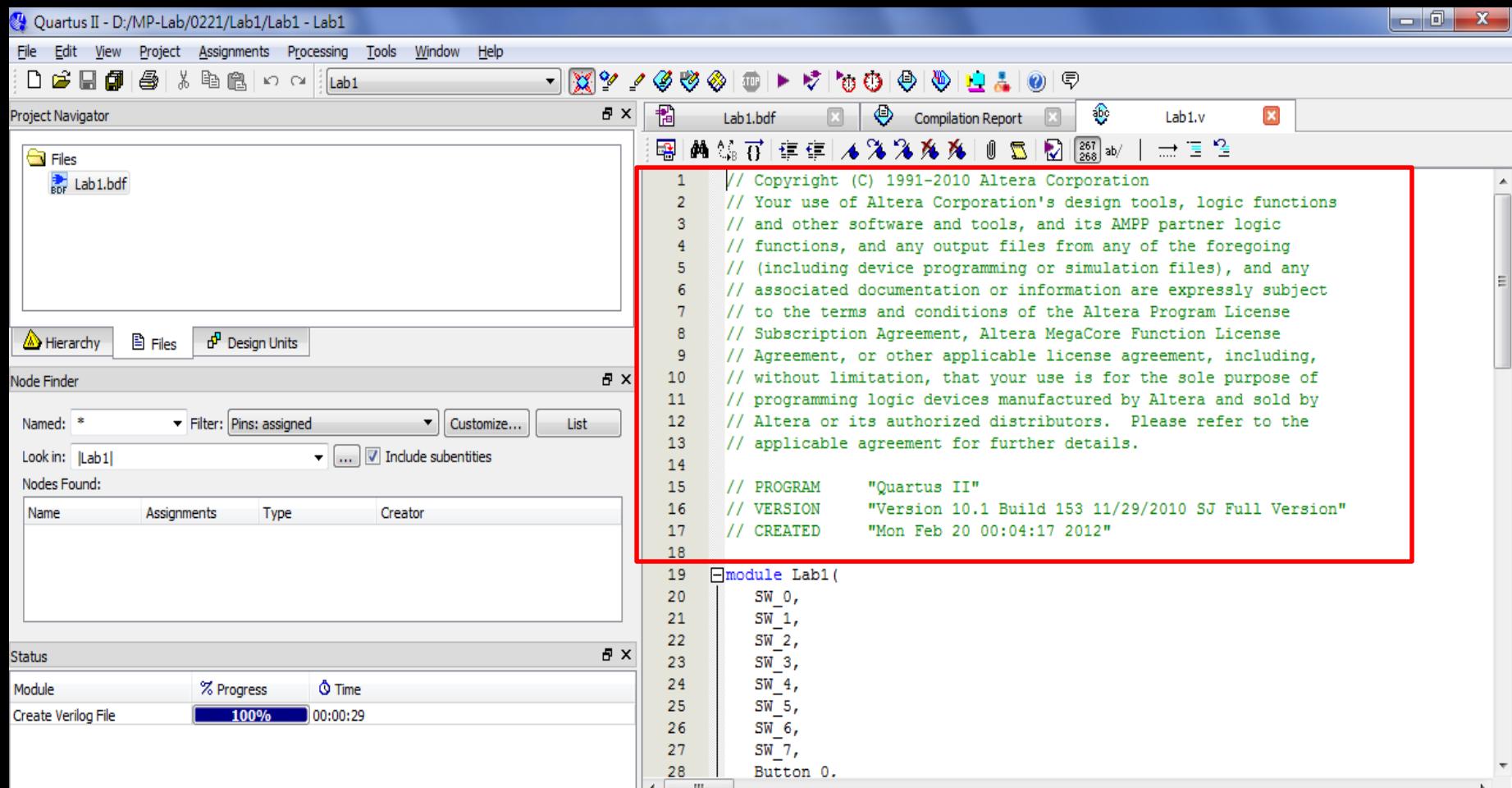
# Schematic Design Result (cont.)



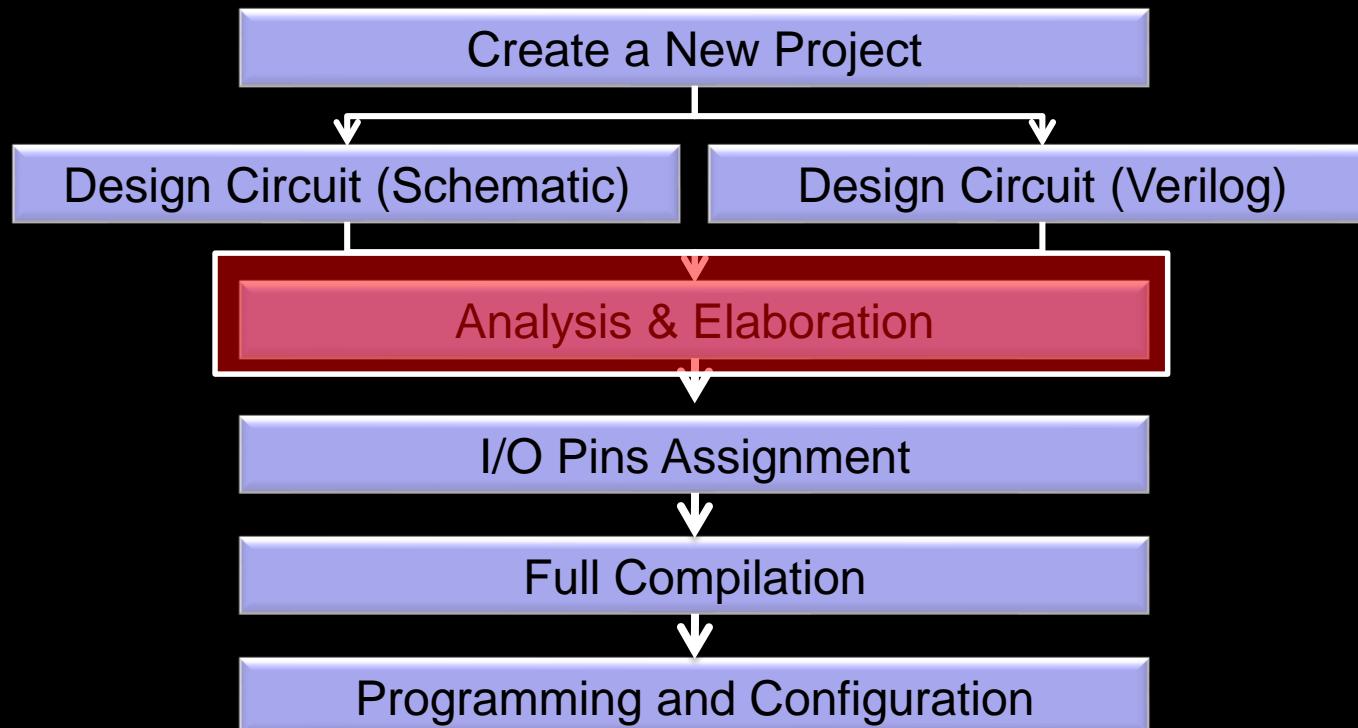
# TIP: Transfereing Schematic to Verilog Code



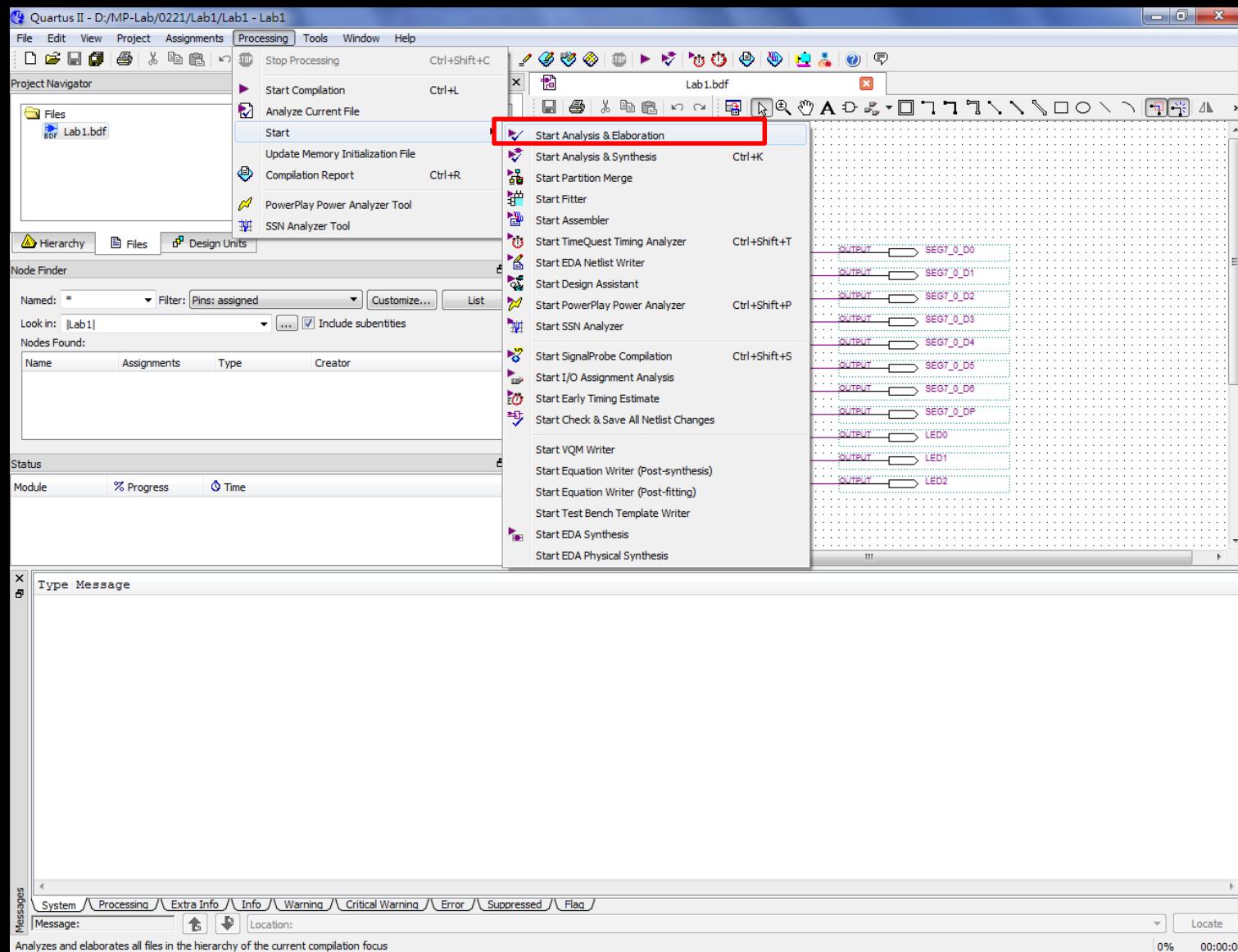
# TIP: Transfereing Schematic to Verilog Code (cont.)



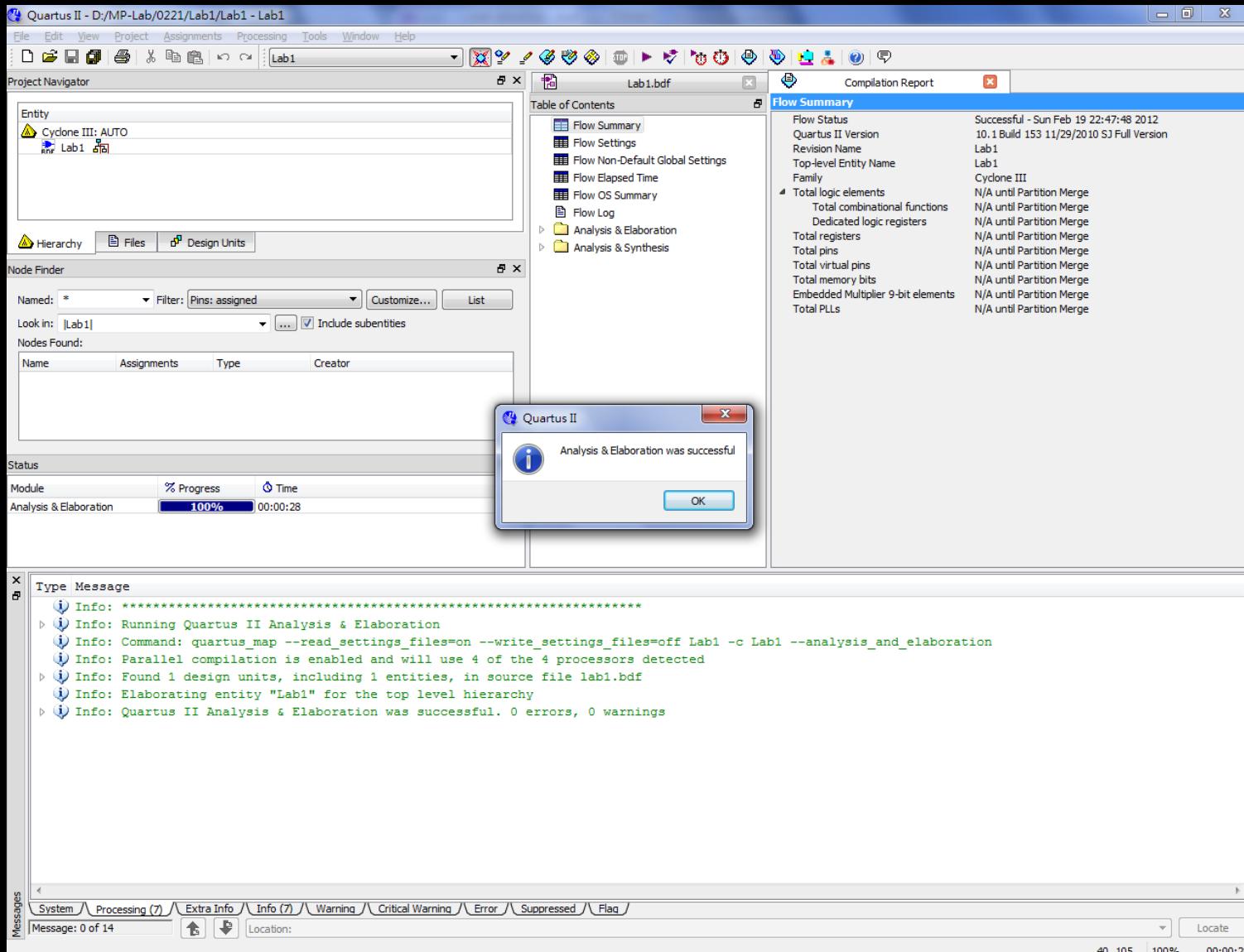
# Flow of FPGA Design with Quartus II



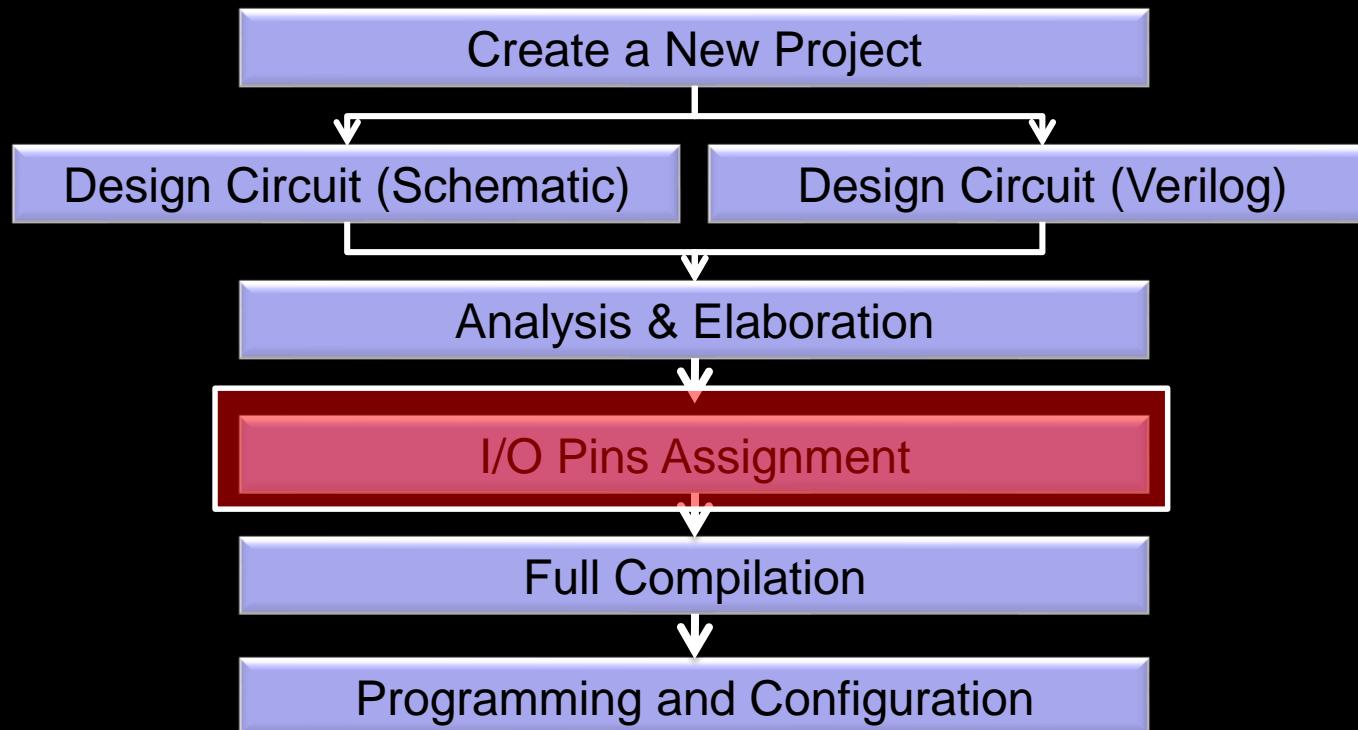
# Analysis & Elaboration



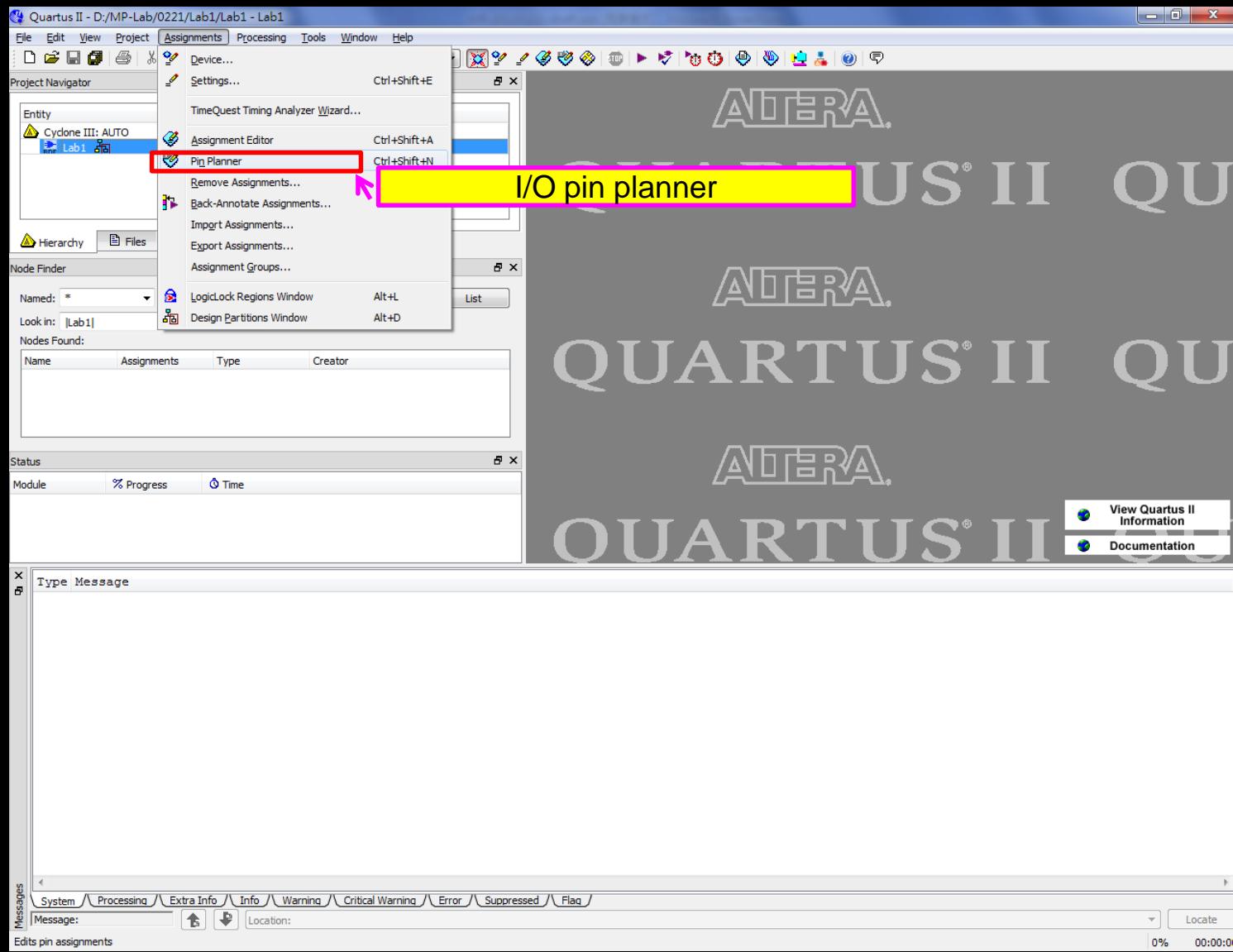
# Success of Analysis & Elaboration



# Flow of FPGA Design with Quartus II



# Pin Planner



# Assign I/O Pins

Pin Planner - D:/MP-Lab/0221/Lab1/Lab1 - Lab1

File Edit View Processing Tools Window

Groups  
Named: \* <<new group>>

Node Name Direction Location

Top View - Wire Bond  
Cyclone III - EP3C16F484C6

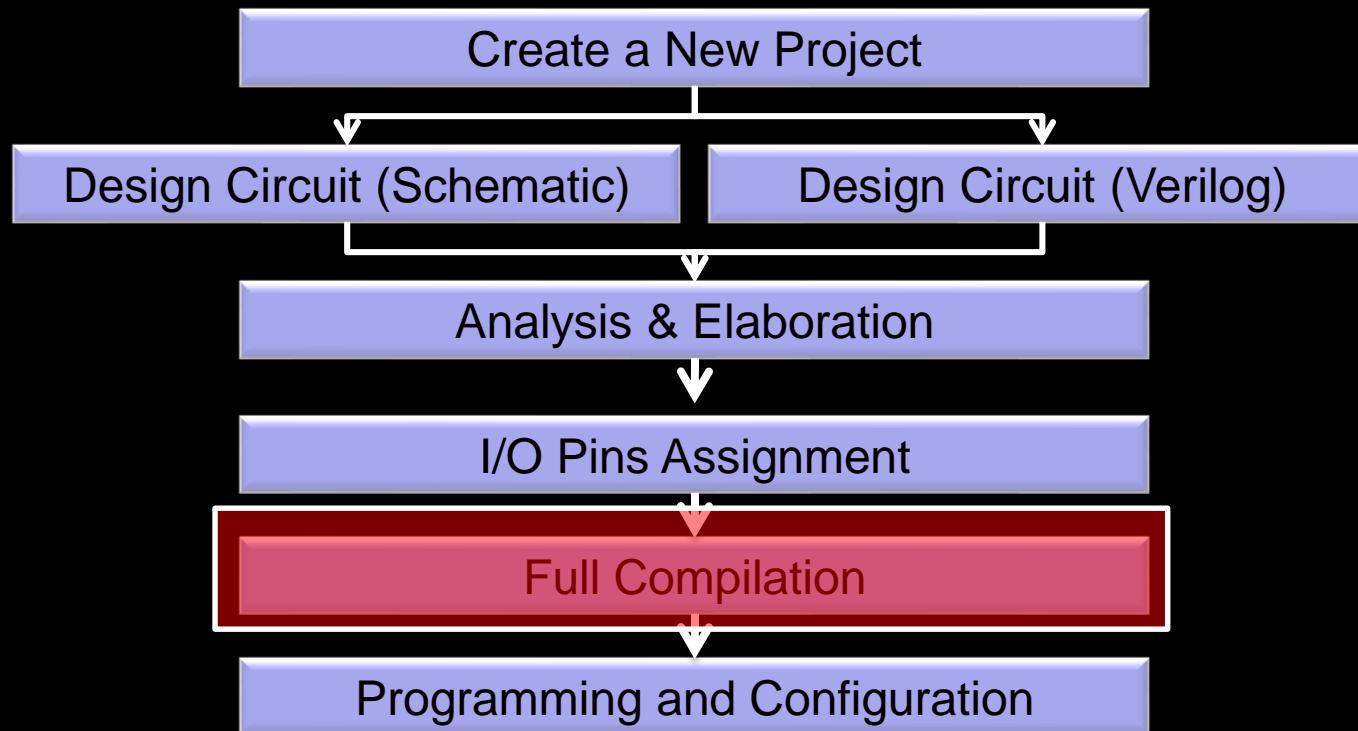
See user manual for pin assignment

Node Name	Direction	Location	I/O Standard	Reserved
Button_0	Input		2.5 V (default)	
Button_1	Input		2.5 V (default)	
Button_2	Input		2.5 V (default)	
LED0	Output		2.5 V (default)	
LED1	Output		2.5 V (default)	
LED2	Output		2.5 V (default)	
SEG7_0_D0	Output		2.5 V (default)	
SEG7_0_D1	Output		2.5 V (default)	
SEG7_0_D2	Output		2.5 V (default)	
SEG7_0_D3	Output		2.5 V (default)	
SEG7_0_D4	Output		2.5 V (default)	
SEG7_0_D5	Output		2.5 V (default)	
SEG7_0_D6	Output		2.5 V (default)	
SEG7_0_DP	Output		2.5 V (default)	
SW_0	Input		2.5 V (default)	
SW_1	Input		2.5 V (default)	
SW_2	Input		2.5 V (default)	
SW_3	Input		2.5 V (default)	
SW_4	Input		2.5 V (default)	
SW_5	Input		2.5 V (default)	

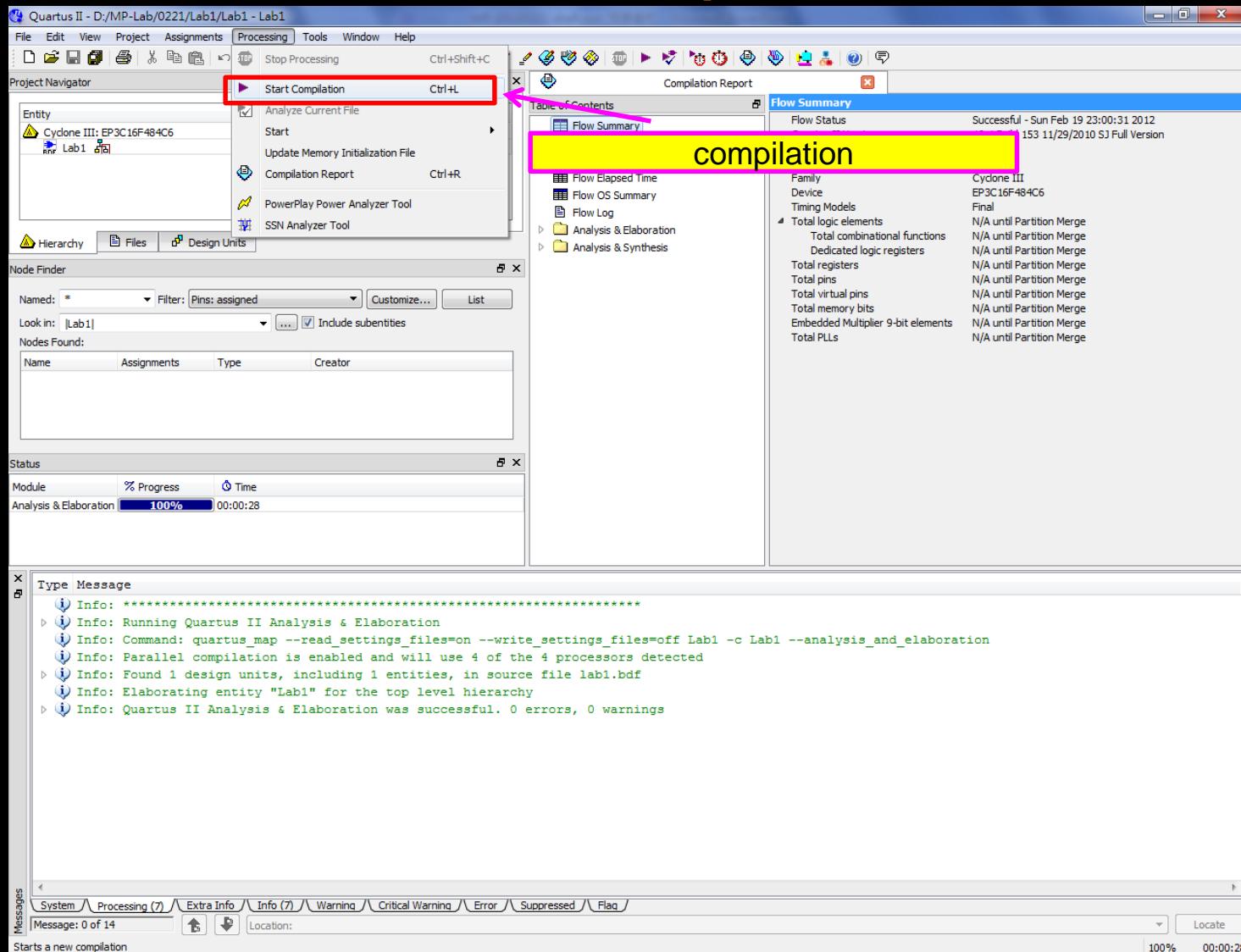
0% 00:00:00

42/75

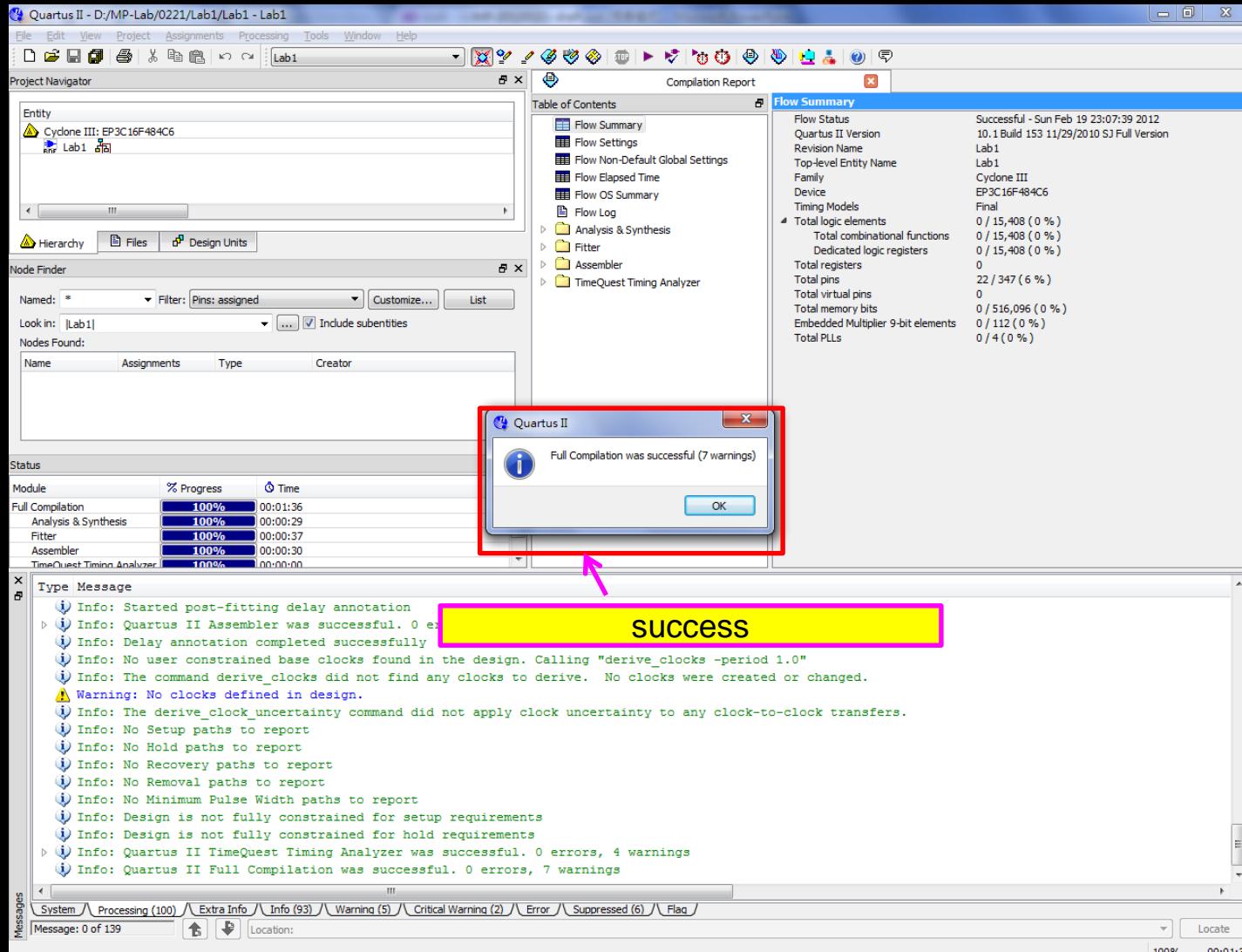
# Flow of FPGA Design with Quartus II



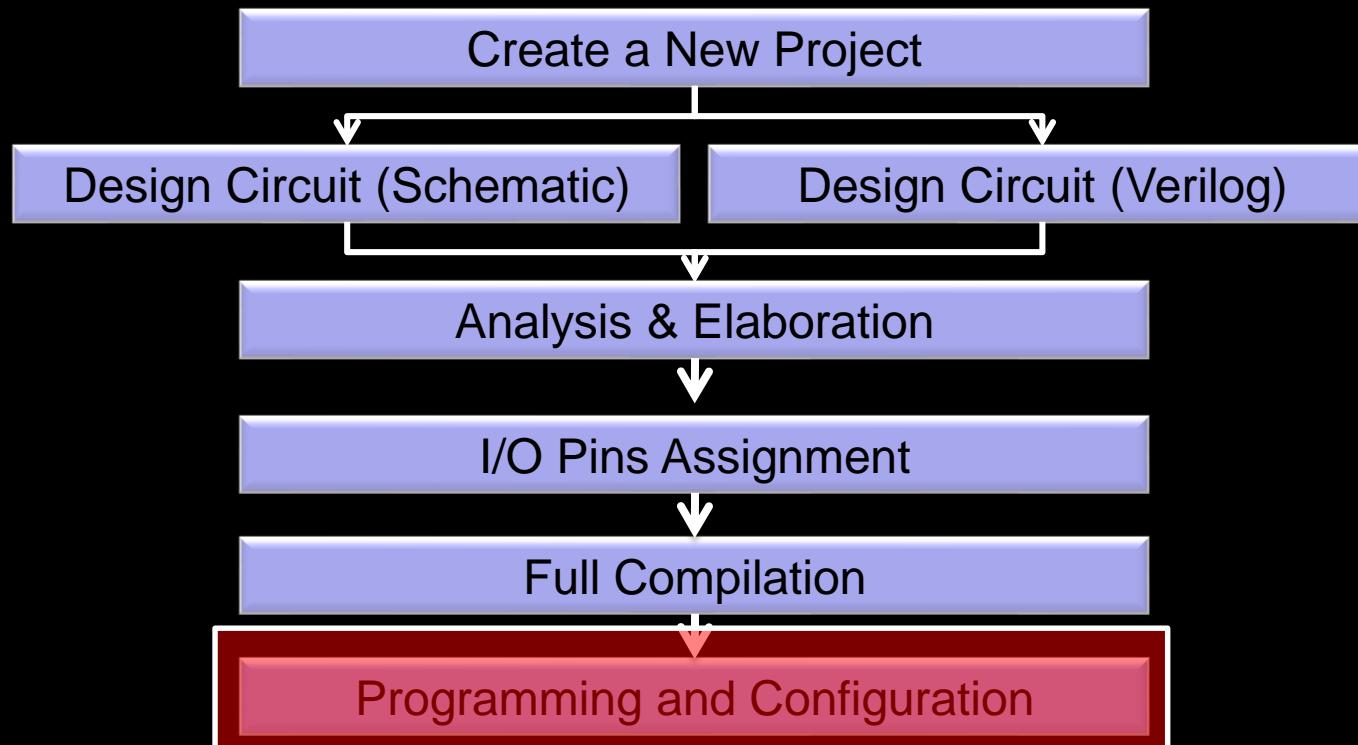
# Start Compilation



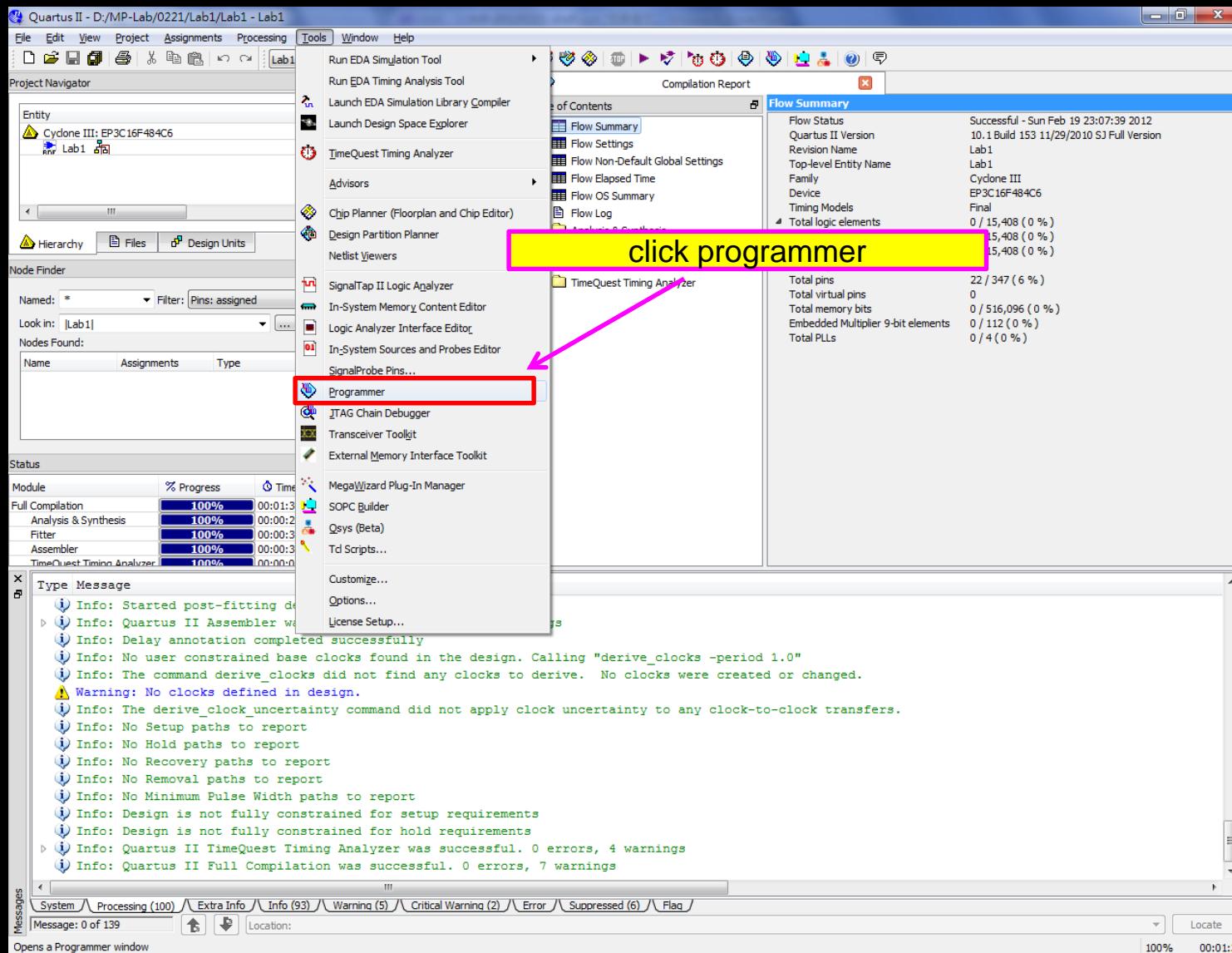
# Success of Compilation



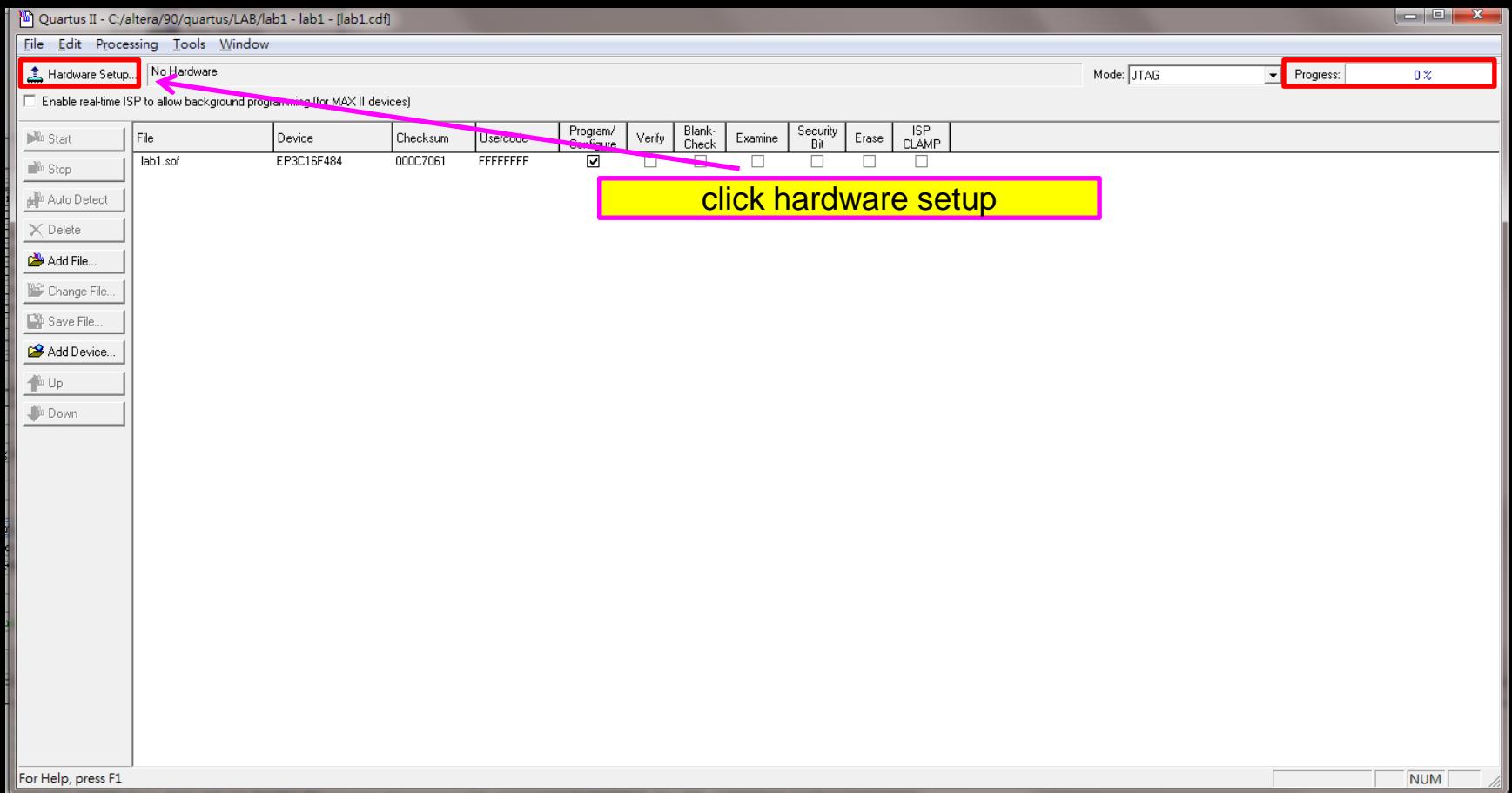
# Flow of FPGA Design with Quartus II



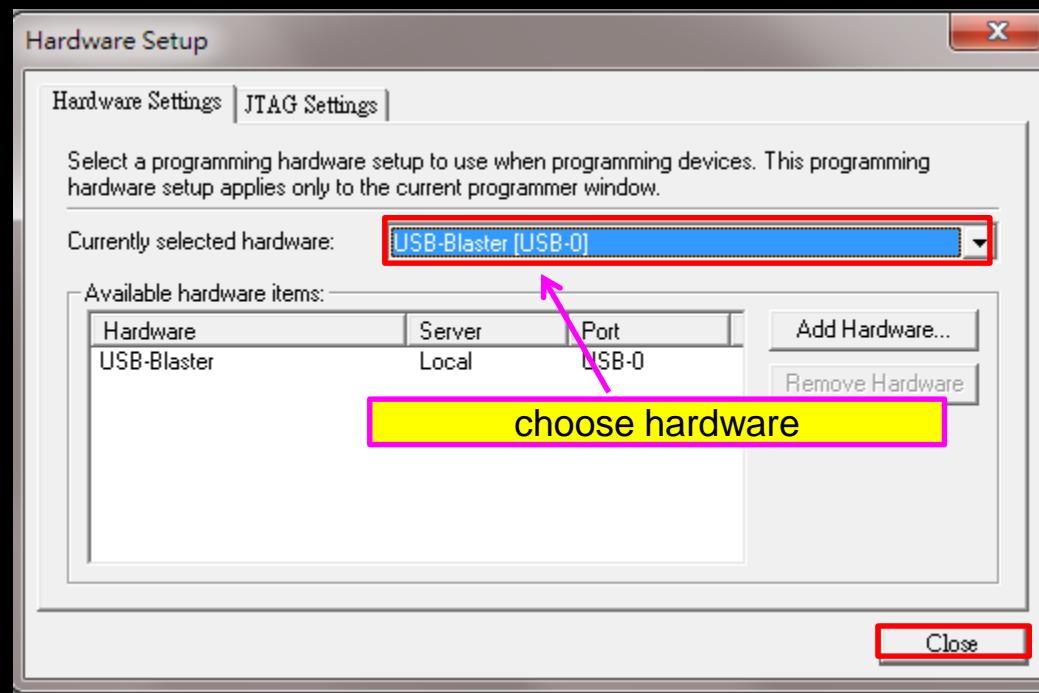
# Programmer



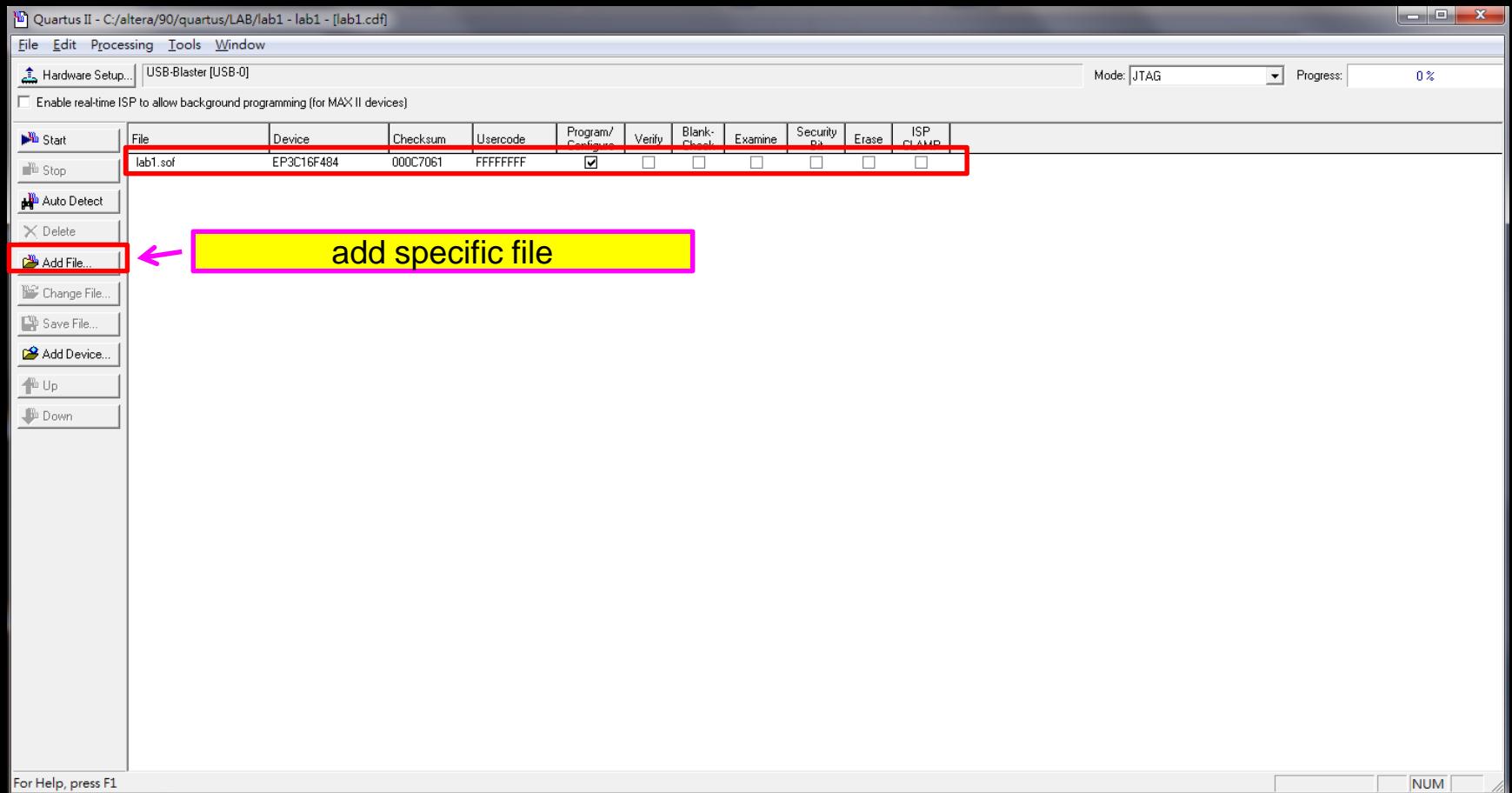
# Hardware Setup



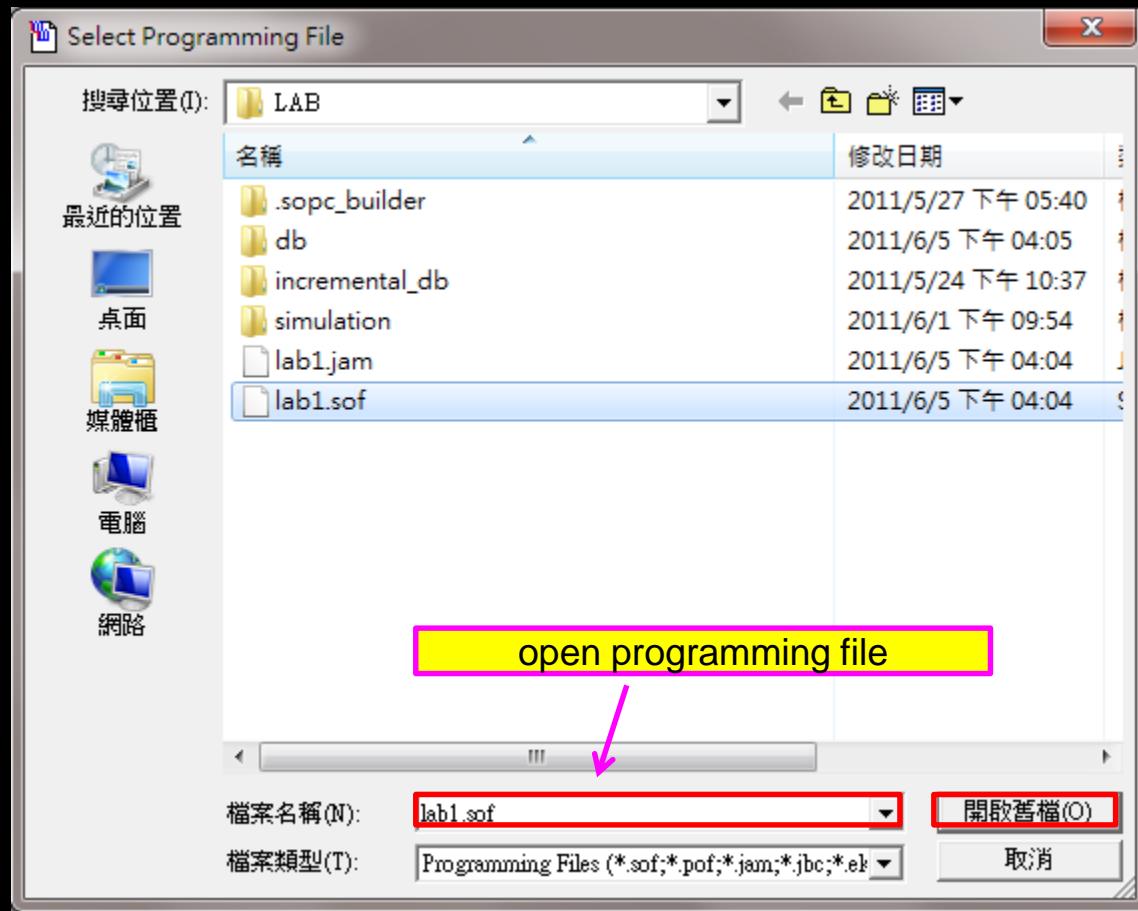
# Add Hardware



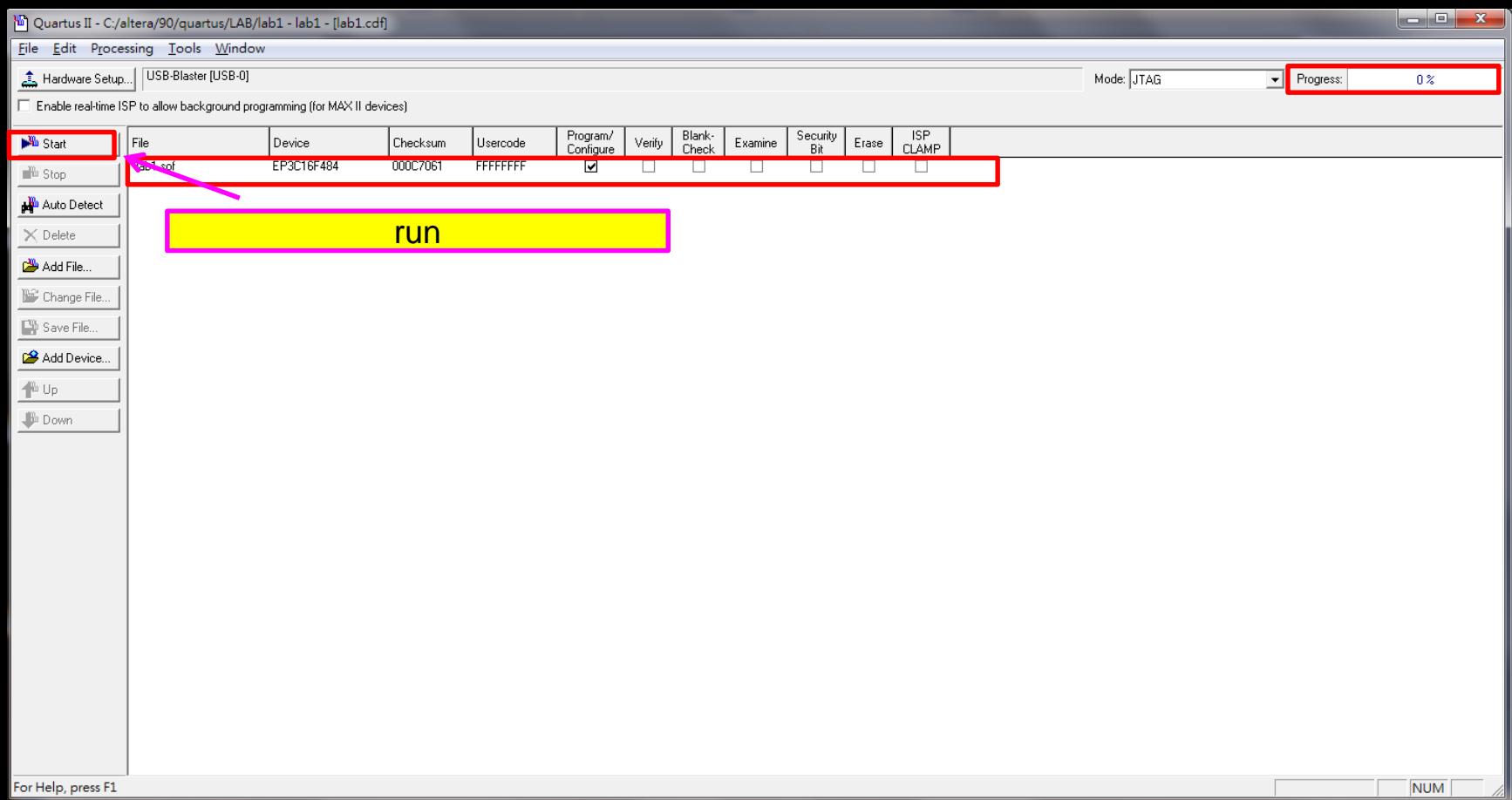
# Design Window



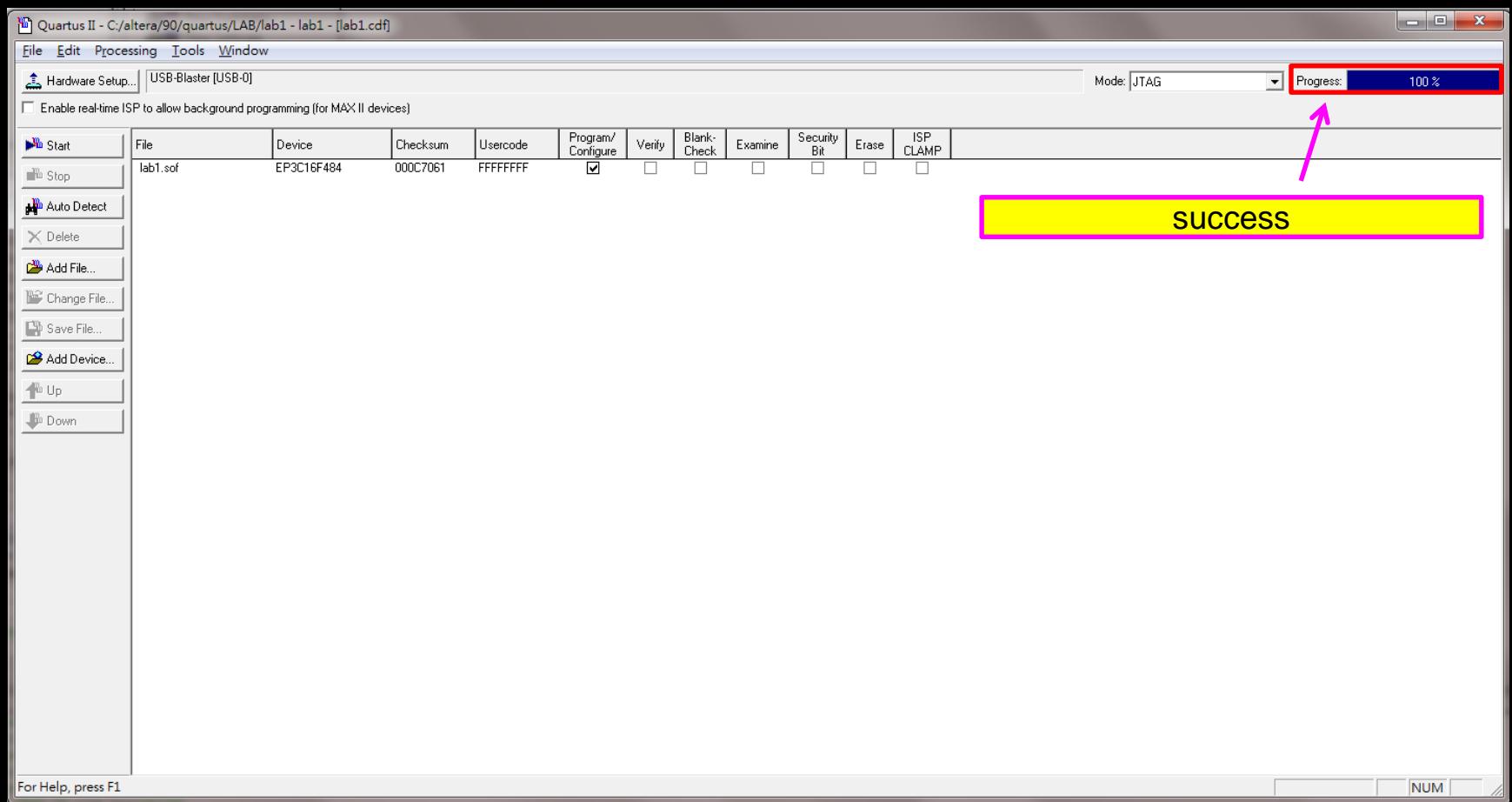
# Read Programming File



# Run Programming File



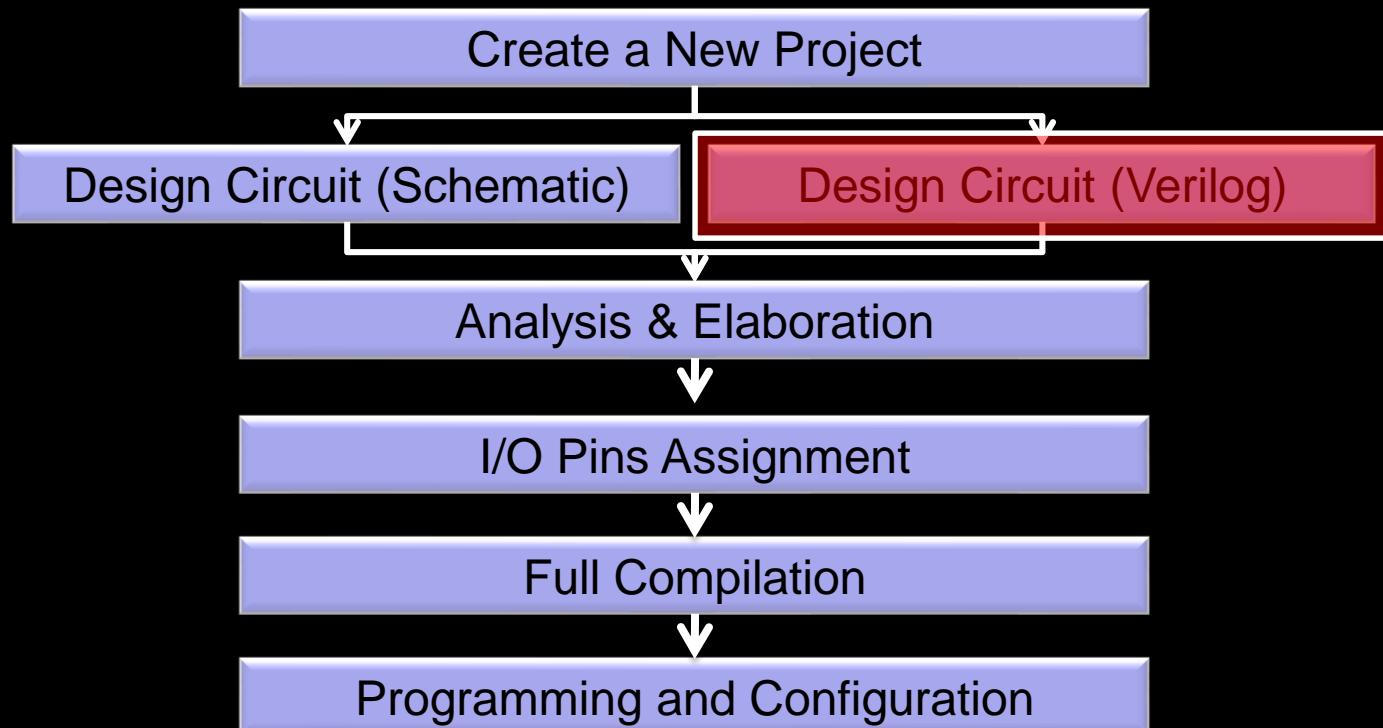
# Success of Configuration



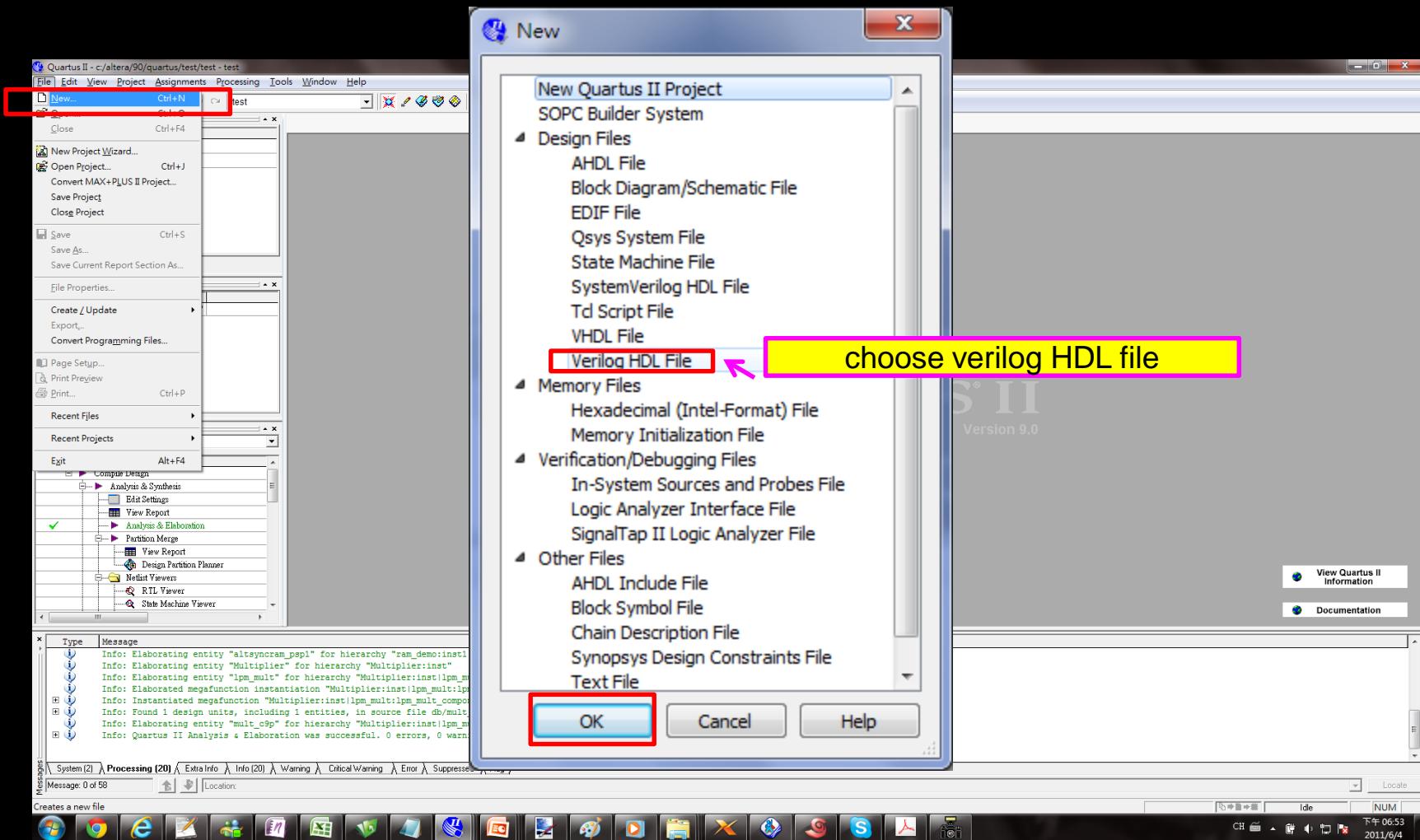
# Outline

- **Introduction - Altera DE0 FPGA Board**
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  - Lab4: Lightning LED

# Flow of FPGA Design with Quartus II



# HDL Design (Verilog File)



# Top-level Module (Lab 2.v)

The screenshot shows the Quartus II software interface with the following components:

- Project Navigator**: Shows the project entity "Lab2" under "Cyclone III: EP3C16F484C6".
- Code Editor (Lab2.v\*)**: Displays the Verilog code:

```
1 module Lab2(Sw, Led);
2   input [9:0] Sw;
3   output [9:0] Led;
4   Switch2Led s2l_inst(Sw, Led);
5 endmodule
```

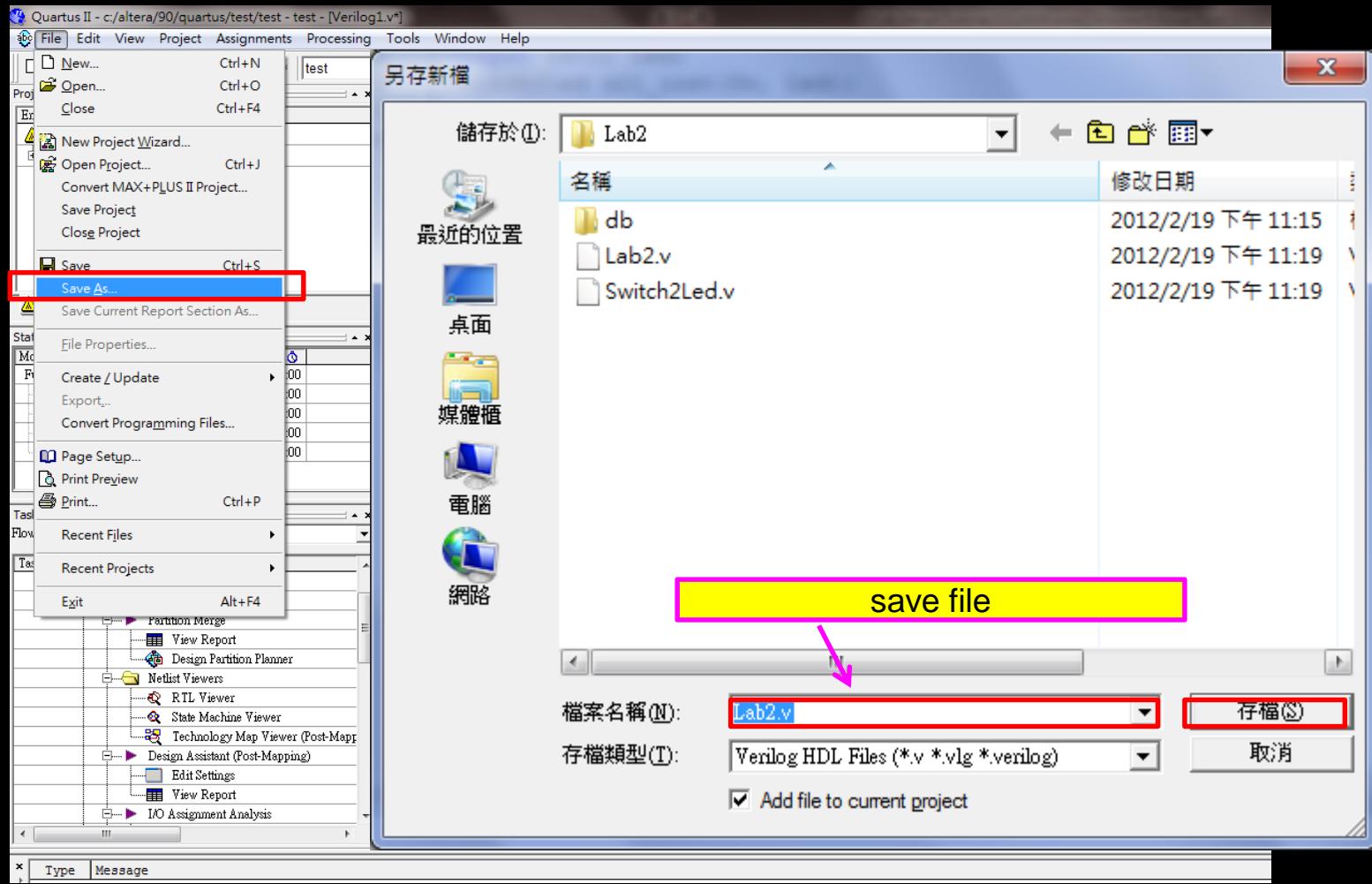
Annotations with red arrows point from the text "Module" to the word "endmodule" and from "Module instance" to the line "Switch2Led s2l\_inst(Sw, Led);".
- Hierarchy**, **Files**, and **Design Units** tabs are visible in the bottom-left.
- Tasks**: Shows a tree view of compilation steps: Compile Design, Analysis & Synthesis, Edit Settings, View Report, Analysis & Elaboration, Partition Merge, Netlist Viewers, Design Assistant (Post-Mapping), I/O Assignment Analysis, Early Timing Estimate, and Fitter (Place & Route).

# Lab2: Switch2Led.v

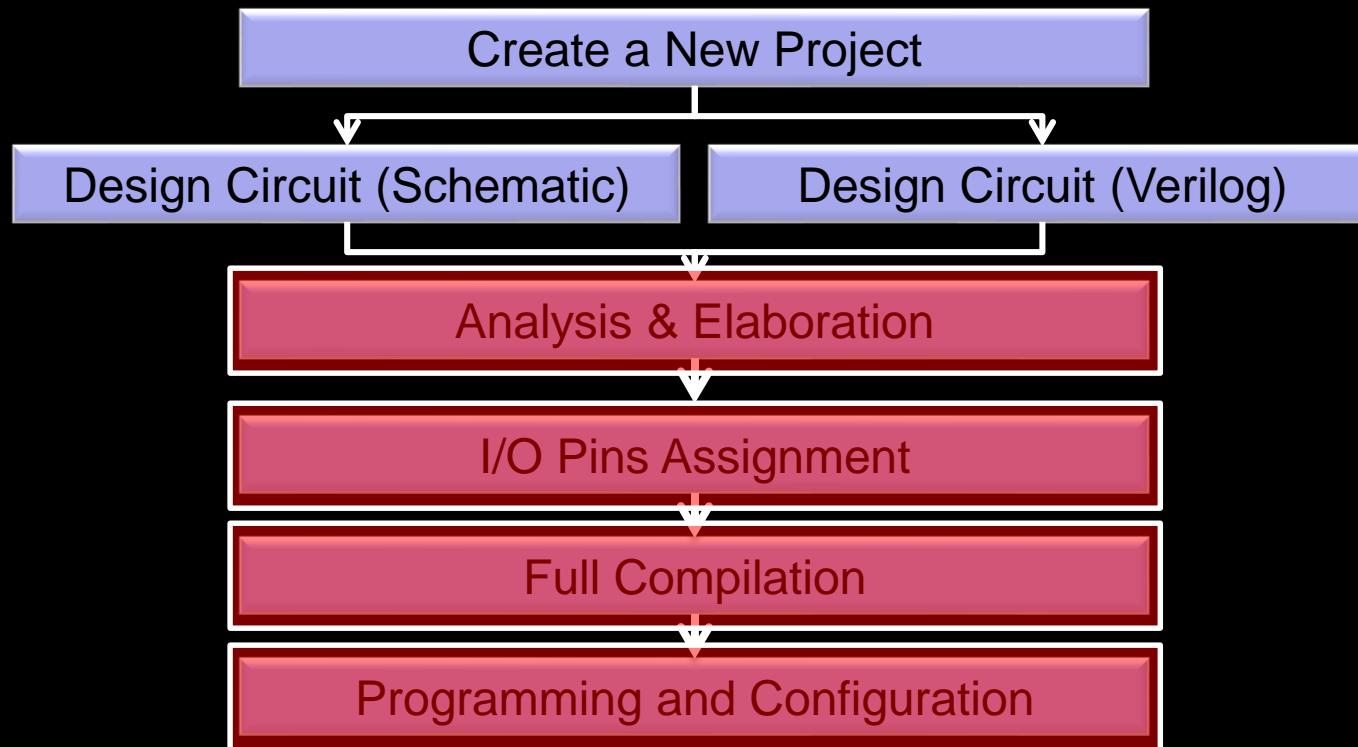
The screenshot shows the Quartus II software interface with the project 'Lab2' open. The 'Switch2Led.v' file is selected in the Project Navigator. A red box highlights the Verilog code in the main editor window.

```
1 module Switch2Led(Sw,Led);
2   input [9:0] Sw;
3   output [9:0] Led;
4   reg [9:0] Led;
5   always@ (Sw)
6     begin
7       Led[9:0] = Sw[9:0];
8     end
9   endmodule
10
```

# Save As Verilog File



# Flow of FPGA Design with Quartus II



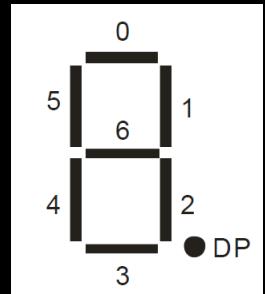
# Outline

- **Introduction - Altera DE0 FPGA Board**
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# Lab3: Binary to Decimal

```
1 module Lab3(Sw, Seg7);
2   input [9:0] Sw;
3   output [31:0] Seg7;
4   Bin2Dec b2d_inst(Sw, Seg7);
5 endmodule
```

Top module



```
1 module Bin2Dec(Sw, Seg7);
2   input [9:0] Sw;
3   output [31:0] Seg7;
4   wire [3:0] n0, n1, n2, n3;
5
6   assign n3 = Sw/1000;
7   assign n2 = (Sw%1000)/100;
8   assign n1 = (Sw%100)/10;
9   assign n0 = (Sw%10);
10
11 Seg7Decode s0(n0, Seg7[7:0]);
12 Seg7Decode s1(n1, Seg7[15:8]);
13 Seg7Decode s2(n2, Seg7[23:16]);
14 Seg7Decode s3(n3, Seg7[31:24]);
15 endmodule
```

```
1 module Seg7Decode(num, seg7Decode);
2   input [3:0] num;
3   output reg [7:0] seg7Decode;
4   always@(num)
5     begin
6       case(num)
7         0 : seg7Decode = 8'b11000000; // 0
8         1 : seg7Decode = 8'b11111001; // 1
9         2 : seg7Decode = 8'b10100100; // 2
10        3 : seg7Decode = 8'b10110000; // 3
11        4 : seg7Decode = 8'b10011001; // 4
12        5 : seg7Decode = 8'b10010010; // 5
13        6 : seg7Decode = 8'b10000010; // 6
14        7 : seg7Decode = 8'b11011000; // 7
15        8 : seg7Decode = 8'b10000000; // 8
16        9 : seg7Decode = 8'b10010000; // 9
17       default :
18         seg7Decode = 8'b11111111;
19     endcase
20   end
21 endmodule
```

Sub modules

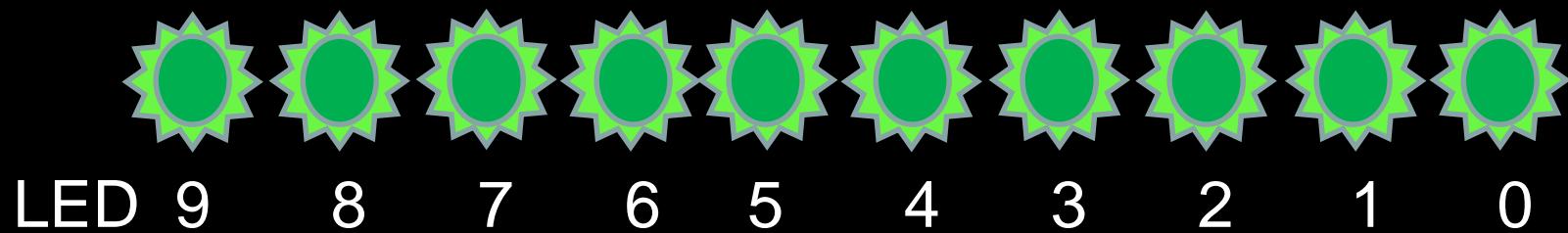
# Outline

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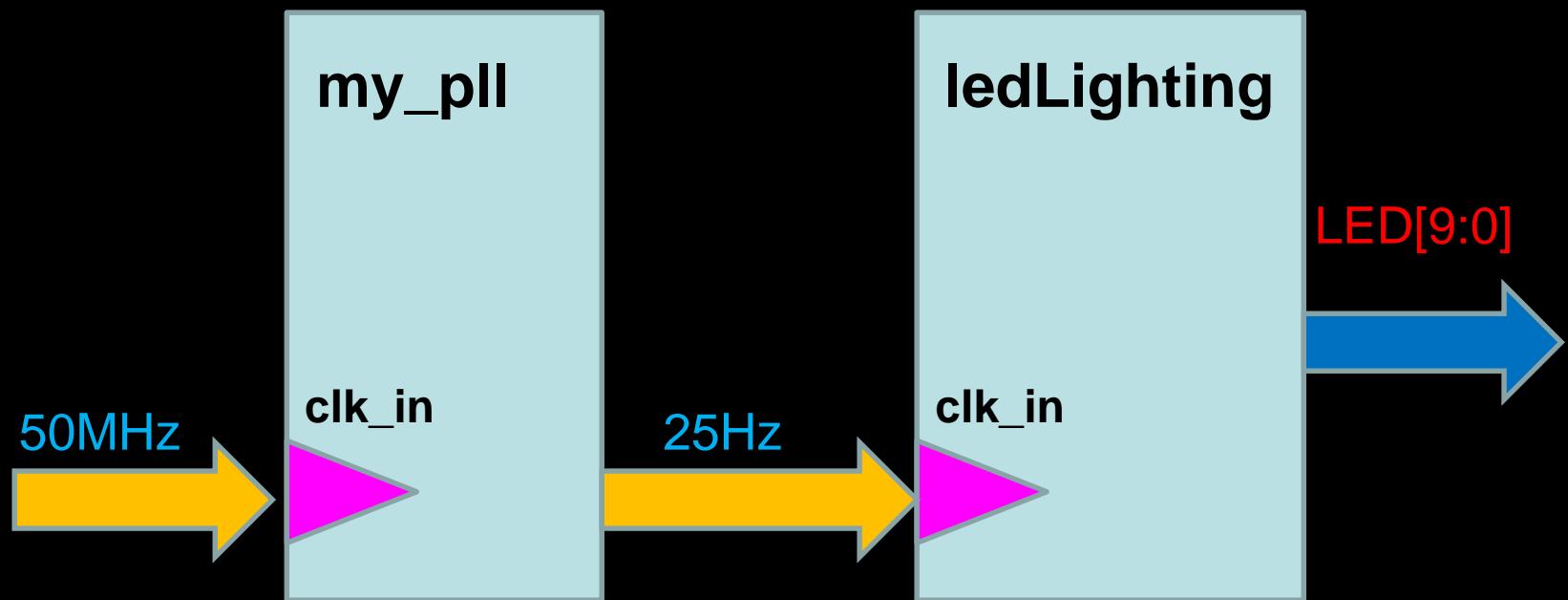
# Knight Rider



# Design: Lightning LED



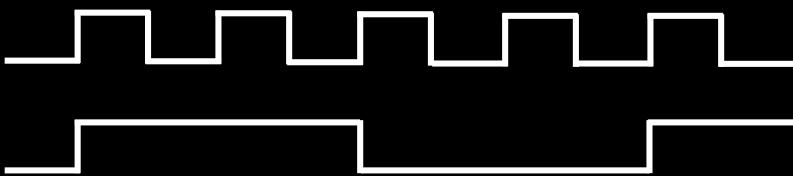
# Lab4: Lightning LED



# Lab4 Design Flow

- **Create a new project “Lab4”**
- **Create a new Verilog file “my\_pll.v”**
- **Create a new Verilog file “ledLightning.v”**
- **Create two new symbols for my\_pll.v and ledLightning.v**
- **Schematic Design**
- **Pin Assignment**
- **Full compilation**

# Module1 my\_pll



New\_clock = 1/2n \* Original\_clock

```
1 module my_pll(clk_in, clk_out);
2   input clk_in; //50MHz
3   output clk_out; //25Hz
4   reg clk_out;
5   parameter counter_max = 1_000_000;
6   reg [19:0] current;
7
8   initial
9   begin
10    clk_out <= 1'b0;
11    current <= counter_max;
12  end
13
14  always@ (posedge clk_in)
15  begin
16    if(current == 0)
17    begin
18      current <= counter_max;
19      clk_out <= !clk_out;
20    end
21    else
22      current <= current - 1;
23  end
24 endmodule
```

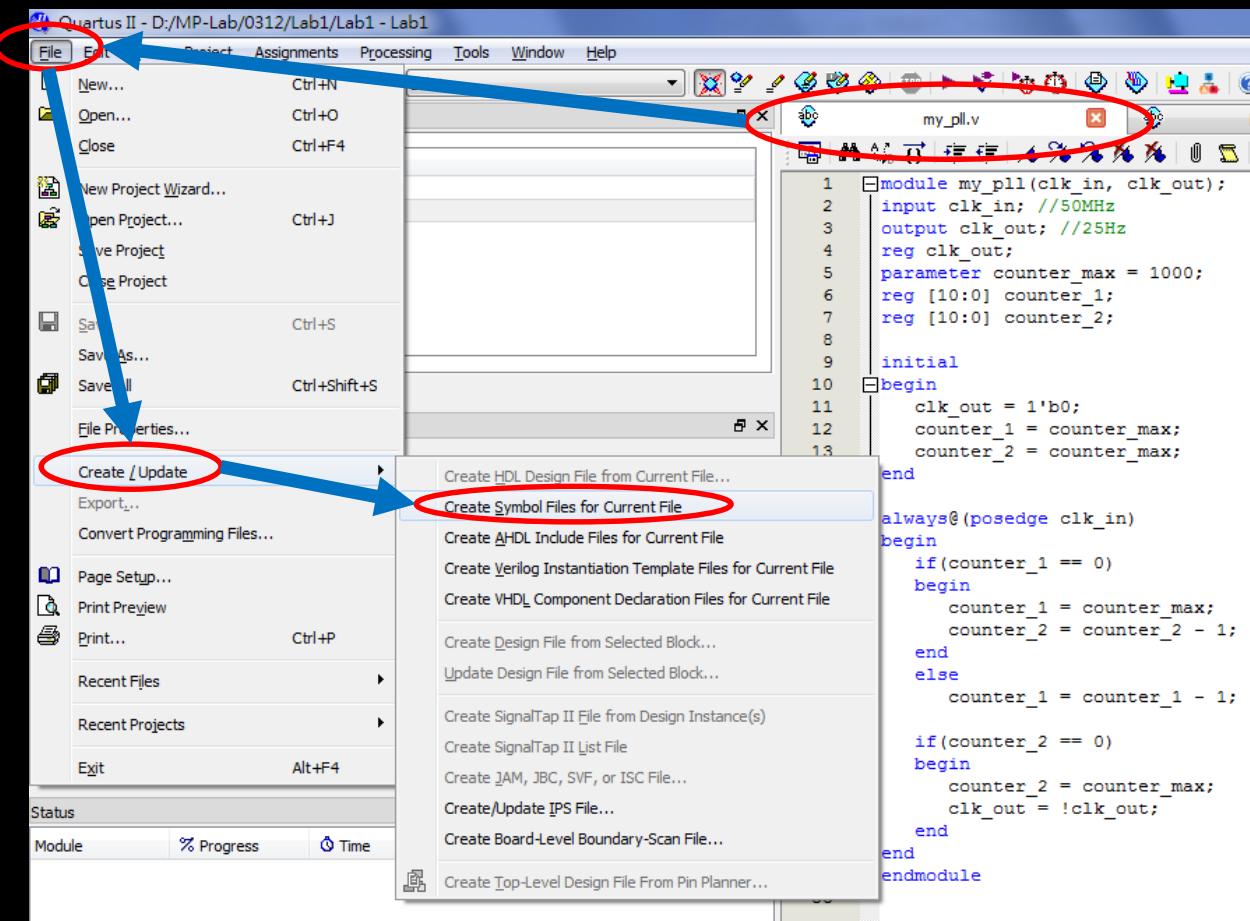
# Module2 ledLightning

```
1 module ledLightning(clk, Led);
2   input clk;
3   output [9:0] Led;
4   reg [9:0]Led;
5   reg direction;
6   initial
7   begin
8     Led[9:1]<=9'b0;
9     Led[0]<=1'b1;
10    direction<=1'b1;
11  end
12
13  always@ (posedge clk)
14  begin
15    if(Led[1] && !direction)
16      direction <= 1'b1;
17    if(Led[8] && direction)
18      direction <= 1'b0;
19  end
20
```

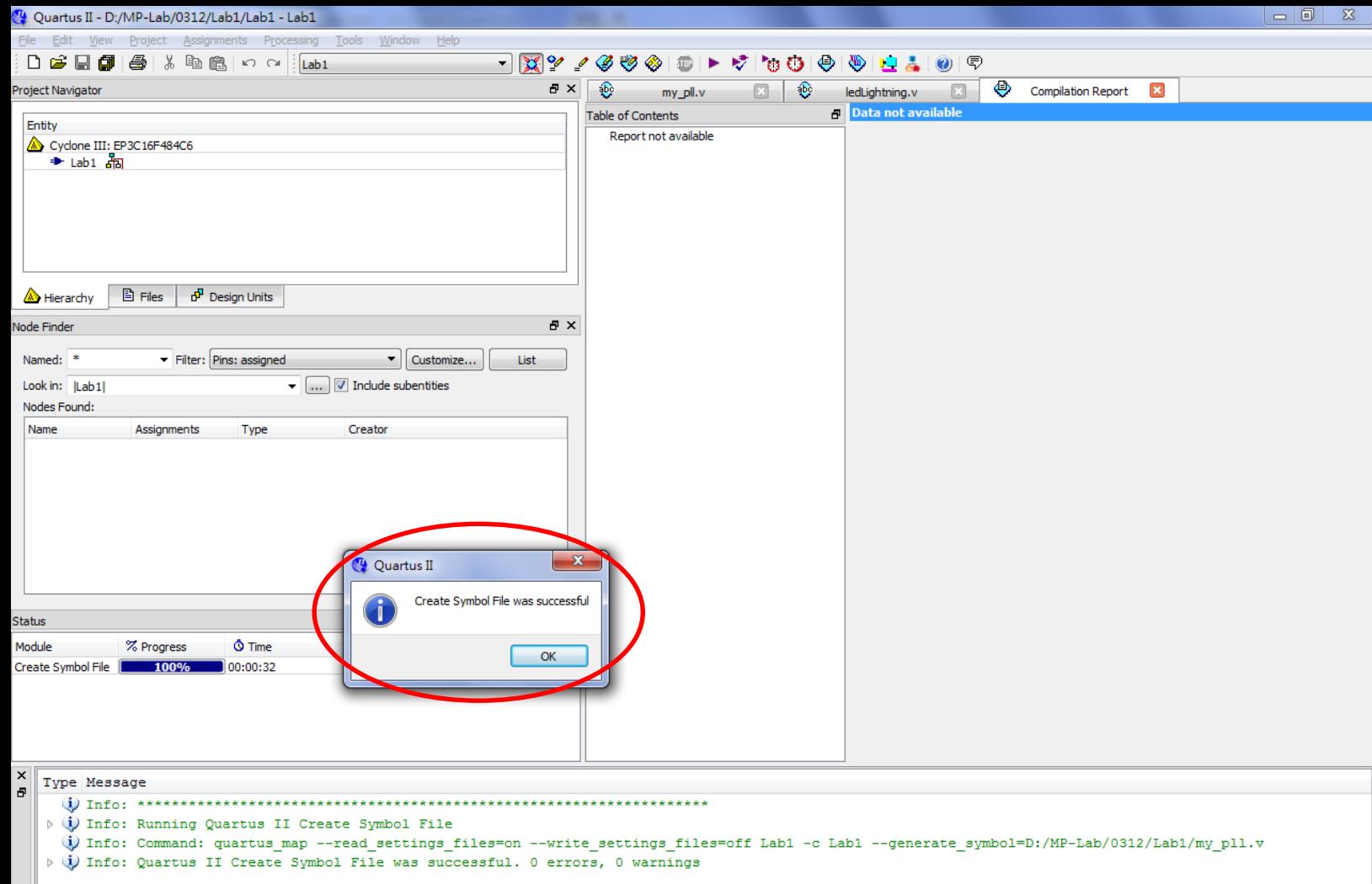
```
21  always@ (posedge clk)
22  begin
23    if(direction)
24    begin
25      Led[0]<=Led[9];
26      Led[1]<=Led[0];
27      Led[2]<=Led[1];
28      Led[3]<=Led[2];
29      Led[4]<=Led[3];
30      Led[5]<=Led[4];
31      Led[6]<=Led[5];
32      Led[7]<=Led[6];
33      Led[8]<=Led[7];
34      Led[9]<=Led[8];
35    end
36    else begin
37      Led[8]<=Led[9];
38      Led[7]<=Led[8];
39      Led[6]<=Led[7];
40      Led[5]<=Led[6];
41      Led[4]<=Led[5];
42      Led[3]<=Led[4];
43      Led[2]<=Led[3];
44      Led[1]<=Led[2];
45      Led[0]<=Led[1];
46      Led[9]<=Led[0];
47    end
48  end
49 endmodule
```

# Create a Symbol File for Verilog-1

- File -> Create / Update -> Create Symbol Files for Current File

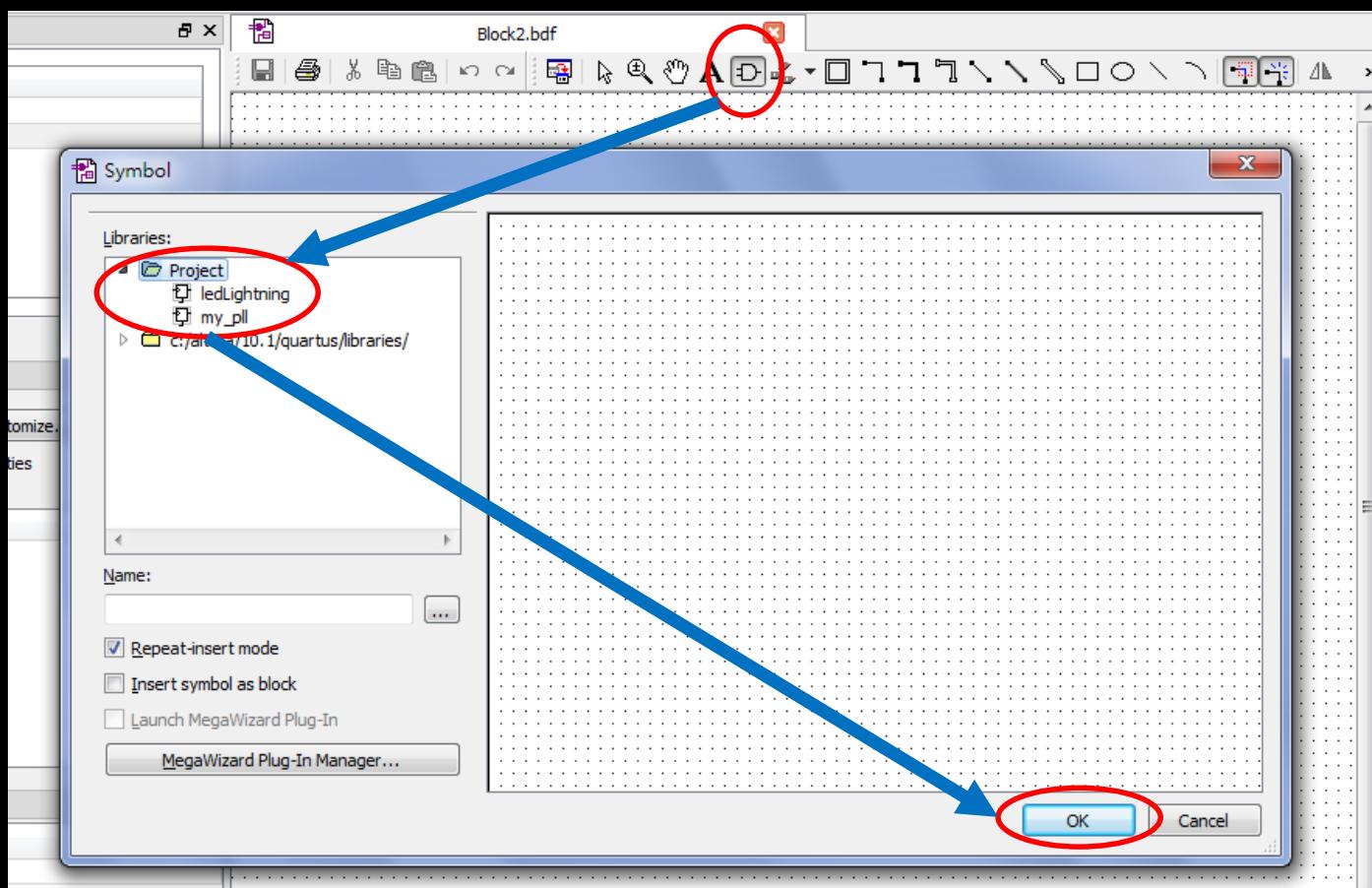


# Create a Symbol File for Verilog-2

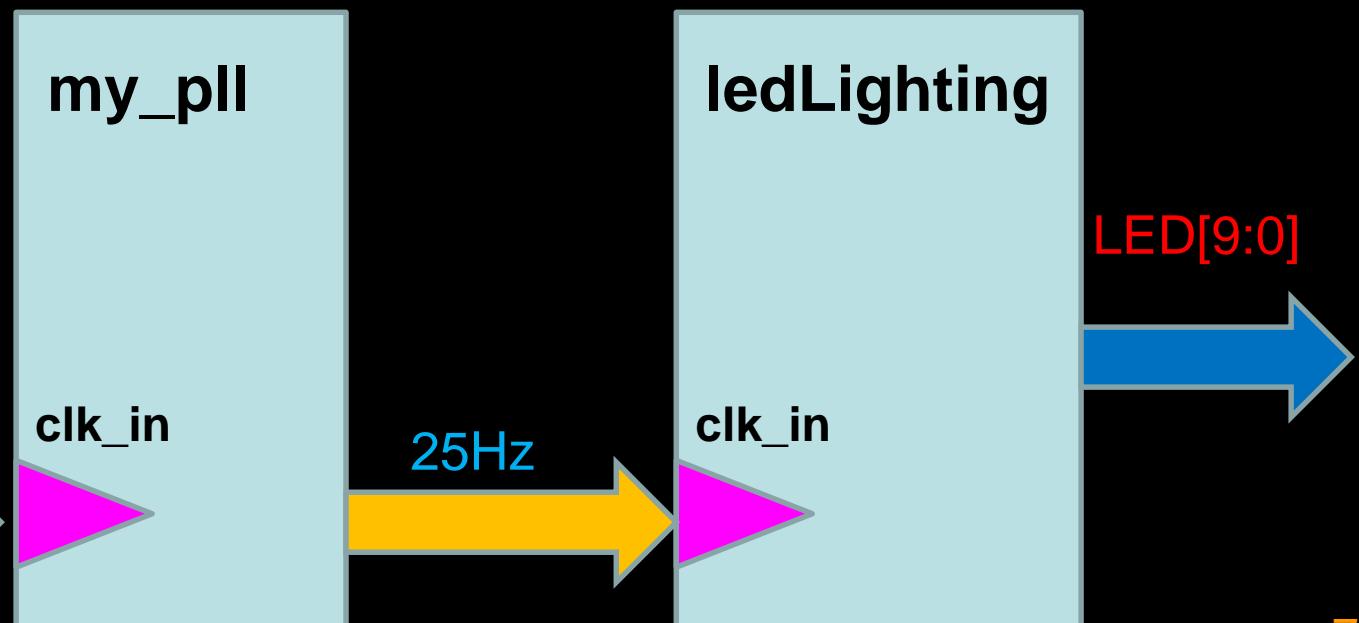
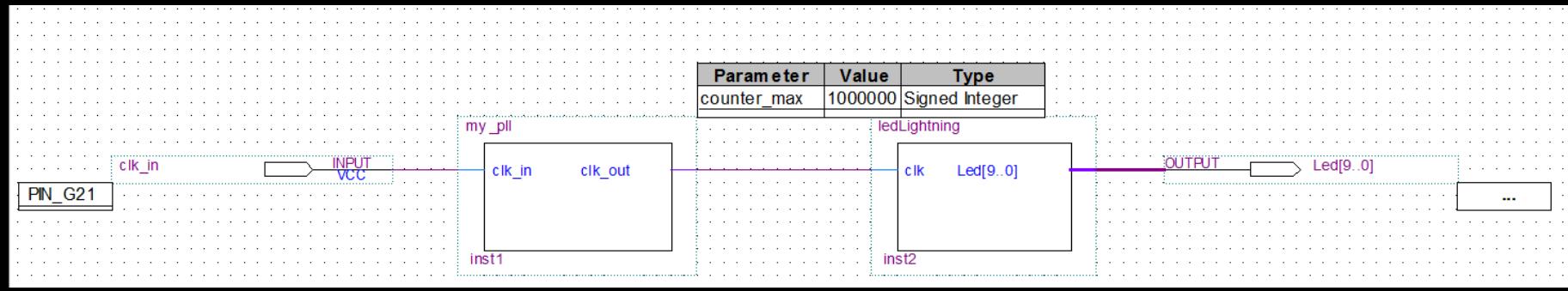


# Schematic Design-1

- File -> New -> Block Diagram / Schematic File



# Schematic Design-2



# Pin Assignment

Pin Planner - D:/MP-Lab/0312/Lab1/Lab1 - Lab1

File Edit View Processing Tools Window

Groups  
Named: \*

Node Name	Direction	Location	I/O Standard	Reserved
Led[9..0]	Output Group			
<<new group>>				

Top View - Wire Bond  
Cyclone III - EP3C16F484C6

The diagram shows the top view of a Cyclone III EP3C16F484C6 chip, specifically the wire bond layout. It features 22 pins along the bottom edge, labeled 1 through 22. The chip is organized into four main vertical columns of pads, each containing various standard symbols like triangles, circles, and squares. The columns are color-coded: yellow (leftmost), green, blue, and red (rightmost). The left side of the chip has labels A through AB corresponding to the pin numbers. The right side has labels A through AB. The top and bottom edges have labels A through AB. The center of the chip has labels J through T.

Node Name Direction Location I/O Standard Reserved

clk_in	Input	PIN_G21	2.5 V (default)	
Led[9]	Output	PIN_B1	2.5 V (default)	
Led[8]	Output	PIN_B2	2.5 V (default)	
Led[7]	Output	PIN_C2	2.5 V (default)	
Led[6]	Output	PIN_C1	2.5 V (default)	
Led[5]	Output	PIN_E1	2.5 V (default)	
Led[4]	Output	PIN_F2	2.5 V (default)	
Led[3]	Output	PIN_H1	2.5 V (default)	
Led[2]	Output	PIN_J3	2.5 V (default)	
Led[1]	Output	PIN_J2	2.5 V (default)	
Led[0]	Output	PIN_J1	2.5 V (default)	
<<new node>>				

# FPGA Project

- **Submit demonstration video clip(s)**
  - Demo your 4 labs including brief oral illustration
  - The PC system time
  - Put your student ID card on the FPGA
  - You may combine the four videos into one
  - There is no grace period for this project

