Lab 3

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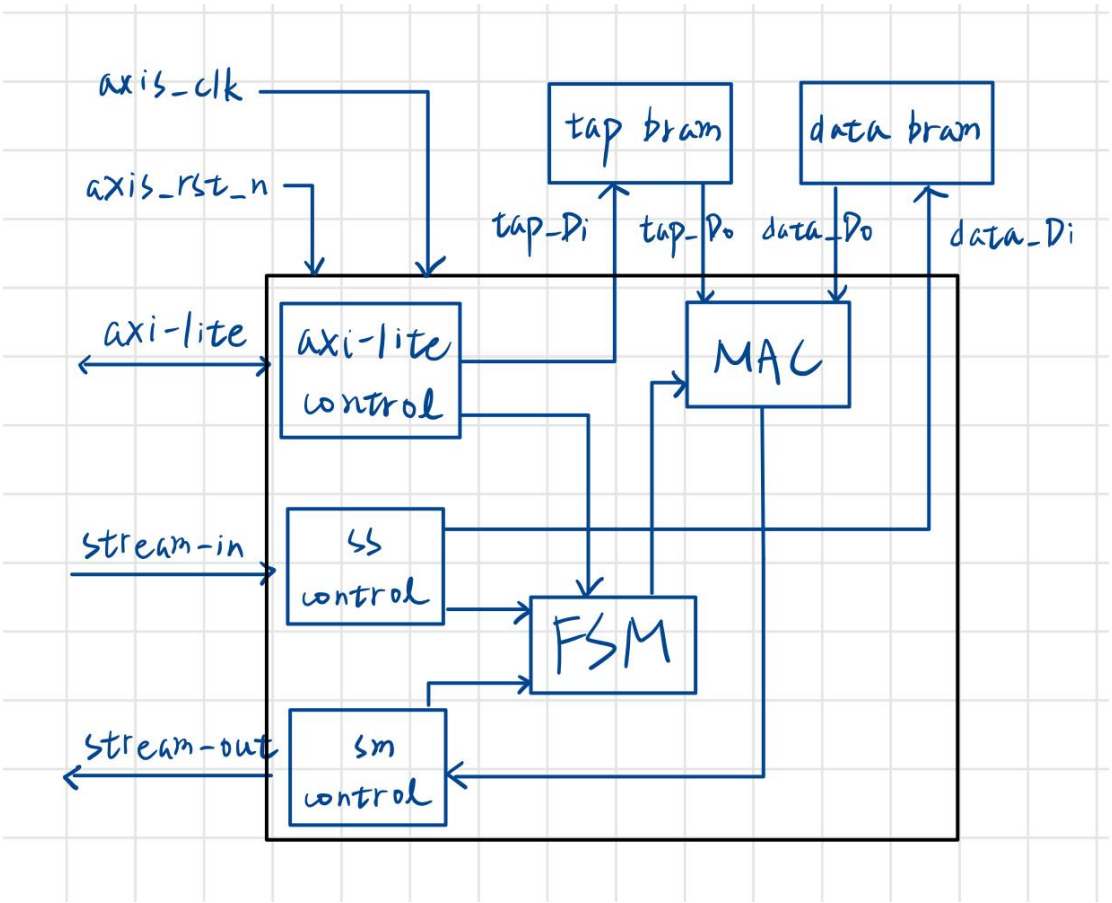
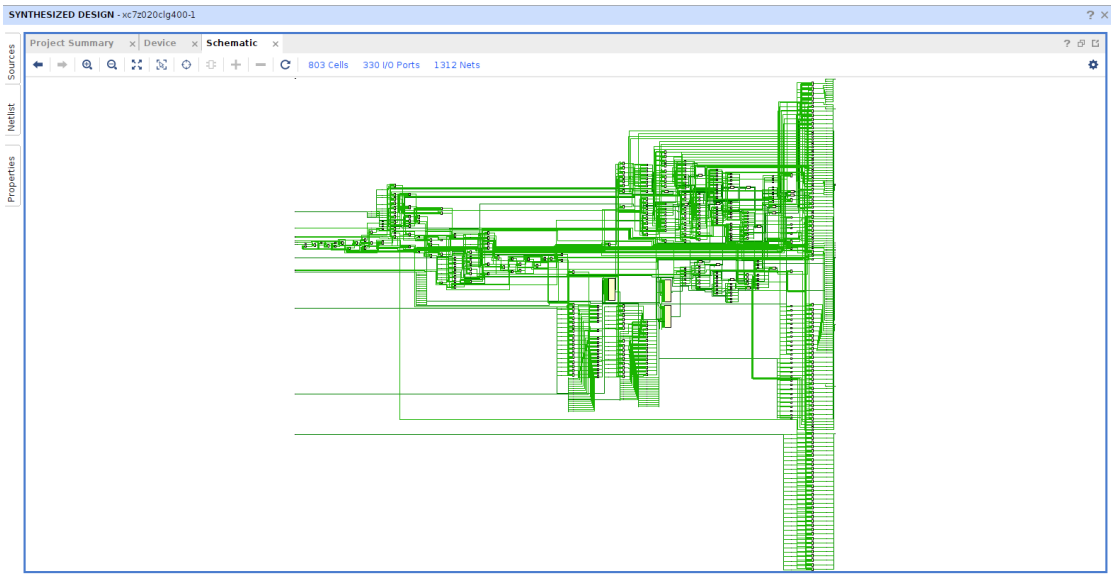
1. Block Diagram





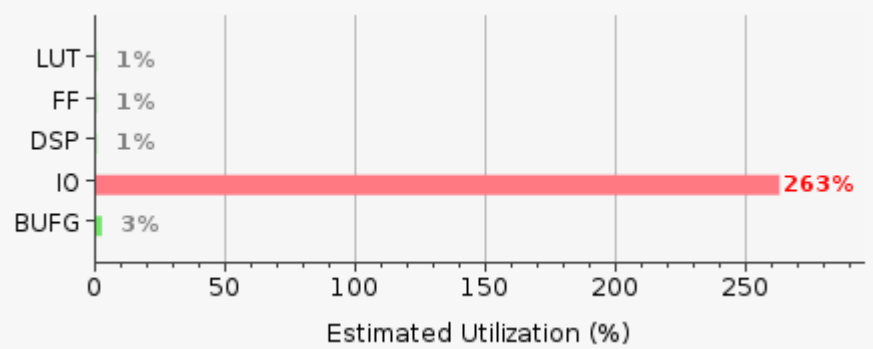
2. Operation

在這次的 Lab3，我們要透過 Verilog 實作 Lab2 中的 FIRN11Stream。其中，coef, len, ap signals 的部分使用 axi-lite protocal 來傳輸，而 input data (Xn)及 output data (Yn)則是使用 axi-stream protocal 來傳輸。

首先，我透過 axi-lite 來接收 host 端傳過來的 write 訊號，並將 write data (coef/tap)儲存到 tap bram 中。接著再次透過 axi-lite 接收 host 端的 read 訊號，將 read data (coef/tap)回傳給 host 端檢查。

完成 coef 的傳輸之後，host 會將 data input (Xn)透過 axi-stream 的方式，持續將 ss (stream slave)訊號傳進來，接著我除了會將以儲存於 tap bram 及 data bram 的資料讀出來進行 pipeline 運算外，也會一邊將新的 data input 存進 data bram 得以進行下一個 data output 運算。

3. Resource usage



Resource	Estimation	Available	Utilization %
LUT	181	53200	0.34
FF	189	106400	0.18
DSP	3	220	1.36
IO	329	125	263.20
BUFG	1	32	3.13

4. Timing Report

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.327 ns	Worst Hold Slack (WHS):	0.142 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	335	Total Number of Endpoints:	335	Total Number of Endpoints:	192

All user specified timing constraints are met.

Longest Path:

Summary

Name	Path 1
Slack	1.327ns
Source	addr_cnt_reg[3]/C (rising edge-triggered cell FDPE clocked by axis_clk {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	mult_out__1/PCIN[0] (rising edge-triggered cell DSP48E1 clocked by axis_clk {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	axis_clk
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (axis_clk rise@10.000ns - axis_clk rise@0.000ns)
Data Path Delay	7.093ns (logic 4.933ns (69.550%) route 2.160ns (30.450%))
Logic Levels	3 (DSP48E1=1 LUT4=2)
Clock Path Skew	-0.145ns
Clock Un...rtainty	0.035ns

Source Clock Path

Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)
(clock axis_clk rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000		axis_clk
net (fo=0)	0.000	0.000		axis_clk
				axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.972	0.972		axis_clk_IBUF_inst/O
net (fo=1, unplaced)	0.800	1.771		axis_clk_IBUF
				axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.101	1.872		axis_clk_IBUF_BUFG_inst/O
net (fo=191, unplaced)	0.584	2.456		axis_clk_IBUF_BUFG
FDPE				addr_cnt_reg[3]/C

Data Path

Delay Type	Incr (ns)	Path ...	Loca...	Netlist Resource(s)
FDPE (Prop_fdpe_C_Q)	(r) 0.478	2.934		addr_cnt_reg[3]/Q
net (fo=10, unplaced)	0.784	3.718		addr_cnt[3]
				data_Di_OBUF[31]_inst_i_2/I1
LUT4 (Prop_lut4_I1_O)	(r) 0.295	4.013		data_Di_OBUF[31]_inst_i_2/O
net (fo=33, unplaced)	0.521	4.534		data_Di_OBUF[31]_inst_i_2_n_0
				data_Di_OBUF[16]_inst_i_1/I2
LUT4 (Prop_lut4_I2_O)	(r) 0.124	4.658		data_Di_OBUF[16]_inst_i_1/O
net (fo=3, unplaced)	0.800	5.458		data_Di_OBUF[16]
				mult_out__0/A[16]
DSP48E1 (Prop_dsp..._A[16]_PCOUT[0])	(r) 4.036	9.494		mult_out__0/PCOUT[0]
net (fo=1, unplaced)	0.055	9.549		mult_out__0_n_153
DSP48E1				mult_out__1/PCIN[0]
Arrival Time		9.549		

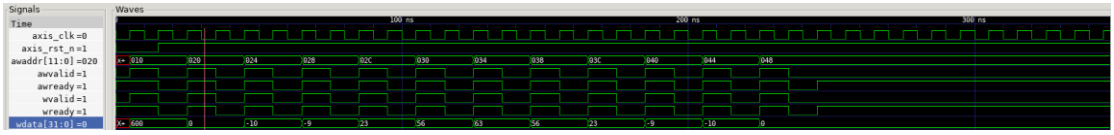
Destination Clock Path

Delay Type	Incr (ns)	Path (...	Loca...	Netlist Resource(s)
(clock axis_clk rise edge)	(r) 10.000	10.000		
	(r) 0.000	10.000		axis_clk
net (fo=0)	0.000	10.000		axis_clk
				axis_clk_IBUF_inst/I
IBUF (Prop_ibuf_I_O)	(r) 0.838	10.838		axis_clk_IBUF_inst/O
net (fo=1, unplaced)	0.760	11.598		axis_clk_IBUF
				axis_clk_IBUF_BUFG_inst/I
BUFG (Prop_bufg_I_O)	(r) 0.091	11.689		axis_clk_IBUF_BUFG_inst/O
net (fo=191, unplaced)	0.439	12.128		axis_clk_IBUF_BUFG
DSP48E1				mult_out__1/CLK
clock pessimism	0.184	12.311		
clock uncertainty	-0.035	12.276		
DSP48E1 (Setup_dsp48e1_CLK_PCIN[0])	-1.400	10.876		mult_out__1
Required Time		10.876		

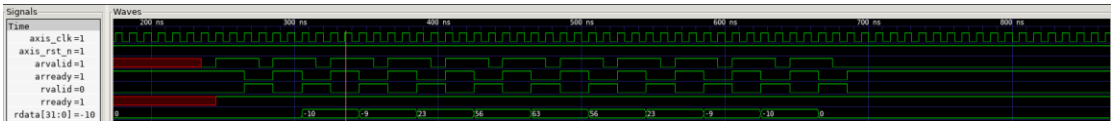
5. Simulation Waveform

- Coefficient program, and read back

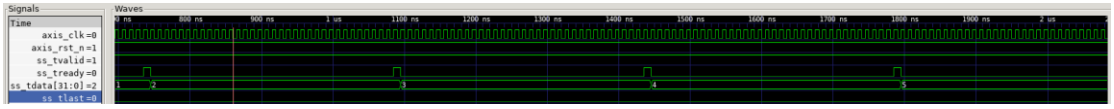
  AXI4-Lite Write:



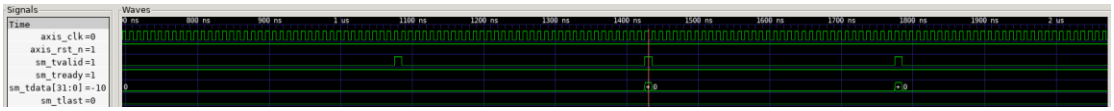
  AXI4-Lite Read:



- Data-in stream-in

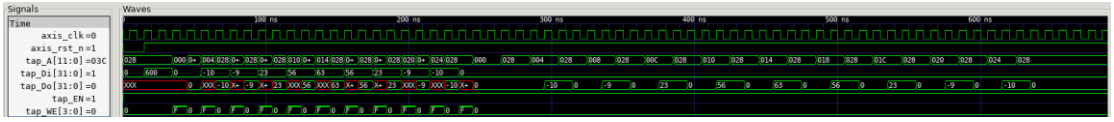


- Data-out stream-out

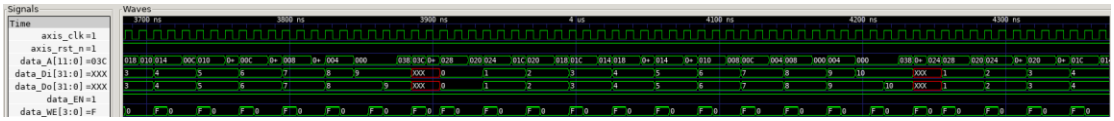


- Bram access control

  Tap Bram:

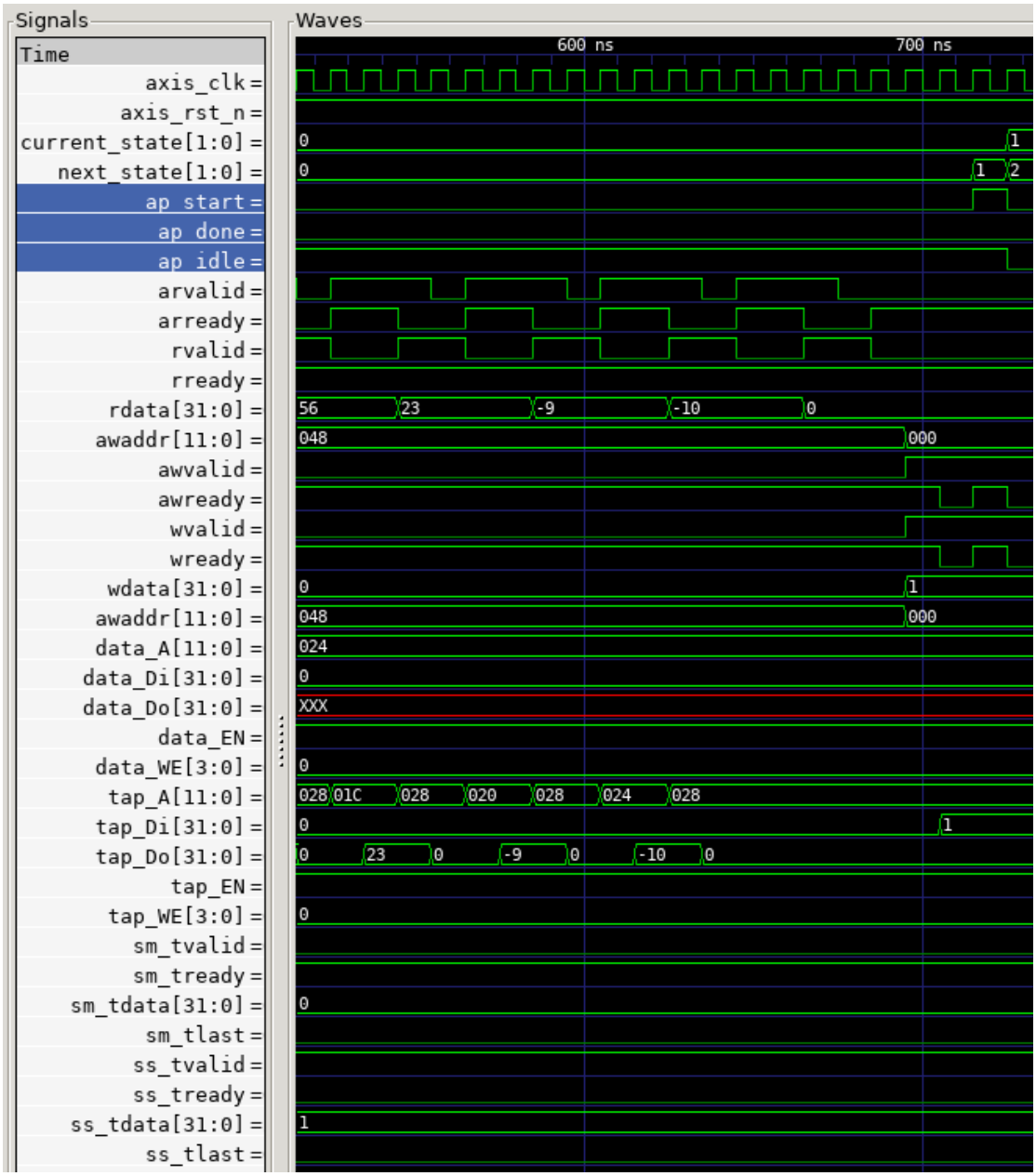


  Data Bram:

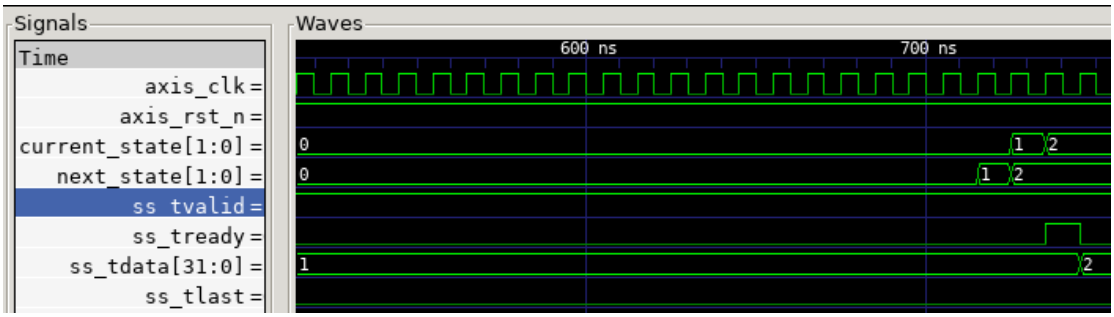


- FSM

S_IDLE (Wait for ap_start):



S_DATA (Wait for ss_tvalid):



S_CAL (calculating until sm_tlast and back to S_IDLE):