ONetSwitch30 Hardware User Guide

1 Overview

ONetSwitch30 is an All Programmable Open Network Innovation Platform.

ONetSwitch30 is based on the Xilinx Zynq™-7000 SoC, and mainly adopts the Gigabit ports. It can achieve a comprehensive experiment platform integrating computing, network and storage. Both its software and hardware can realize custom programming. Its reference designs are abundant and flexible, can be used to various researches on the evolution of network prototypes, and the development of customized network products. Especially, the features of the miniaturization and low power are adapted to the multi-node network tests and deployments.

1.1 Key Features

Table 1 ONetSwitch30 Key Features

General	
Core Silicon	XC7Z030-2SBG485
Power Supply	DC 12V
Programming Source	QSPI Flash / TF Card
Processing System	
Processor	Dual ARM Cortex-A9@800MHz
Cache	L1: 32KB Instruction + 32KB Data per processor; L2: 512KB; OCM: 256KB
DRAM	DDR3 1GBytes
Flash	Quad SPI Flash 256Mb
DMA	8 channel(4 for Programmable Logic)
Ethernet Port	1x 1000BASE-T
Peripheral	USB / USB-UART / USB JTAG / TF Card
Programmable Logic	
Programmable Logic Equivalent	125K Logic Cells, Kintex-7 FPGA, Approximate ASIC Gates 1.9M
PS to PL Interconnect	AMBA AXI4 interconnect, maximum 100Gbps
DRAM	DDR3 2GBytes
Ethernet Port	4x GE RJ45 10/100/1000M Ethernet
Wireless Access	Mini PCIe Slot
Peripheral	2x PMOD
User I/O	User LEDs/Pushbuttons/DIP Switch

1.2 Board Block Diagram

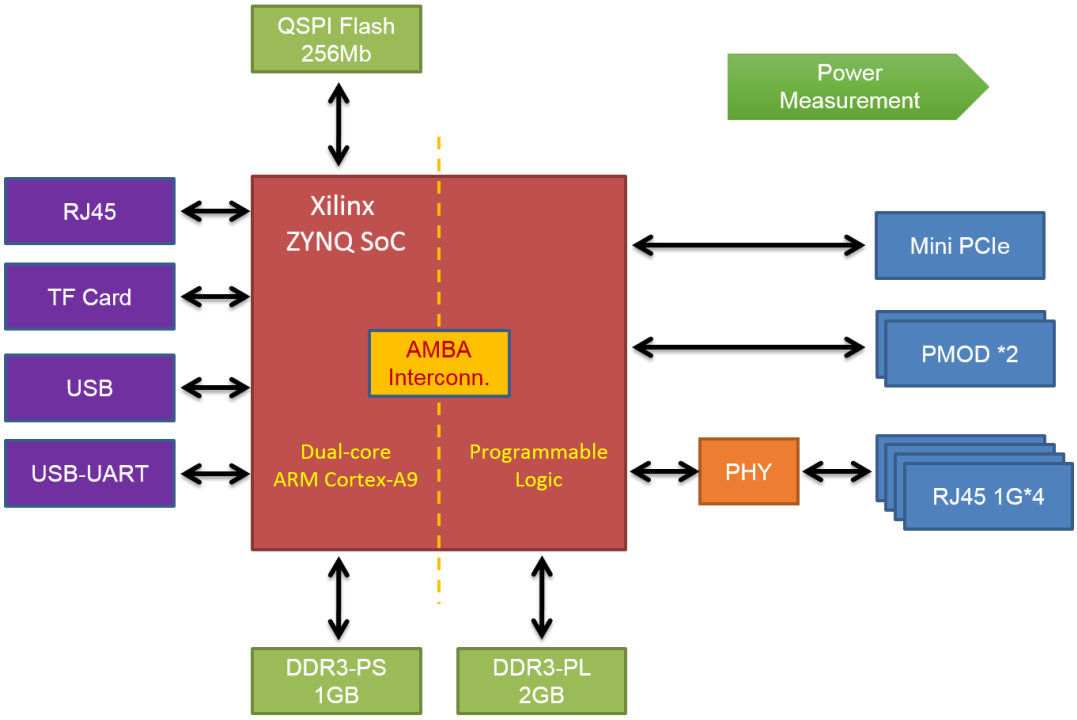

Figure 1 ONetSwitch30 Board Block Diagram

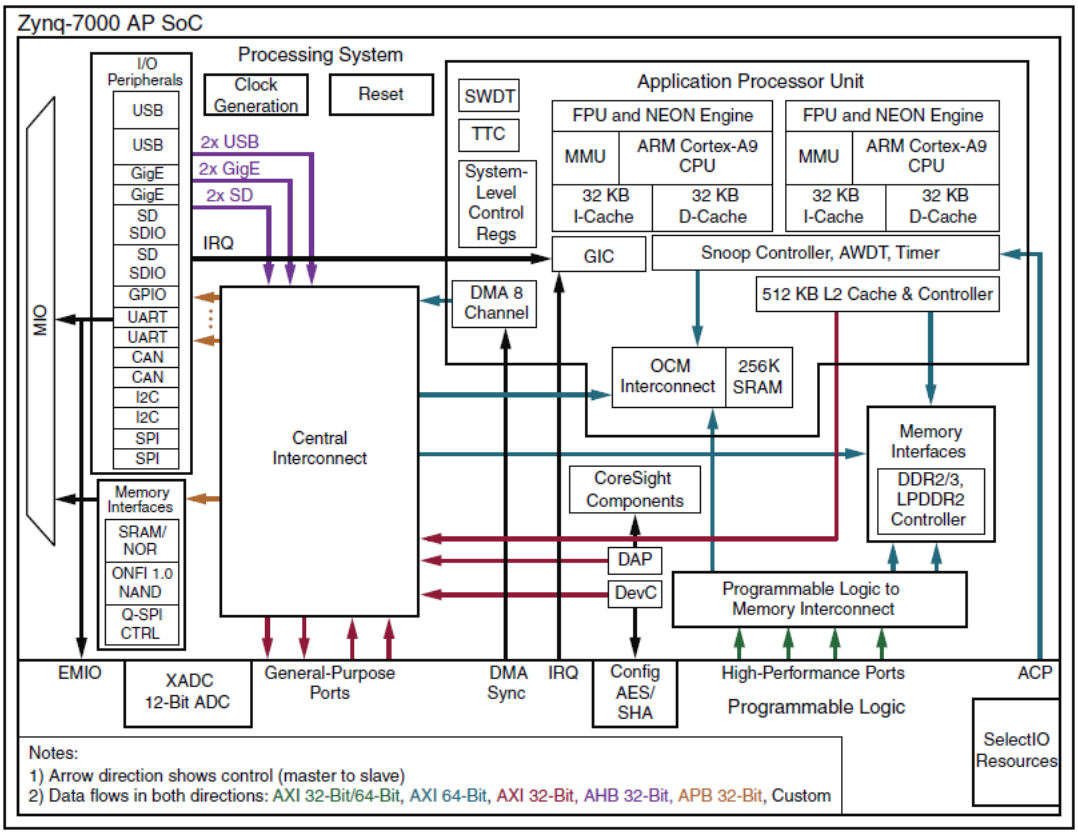

Figure 2 Xilinx Zynq-7000 Block Diagram

1.3 Components Overview

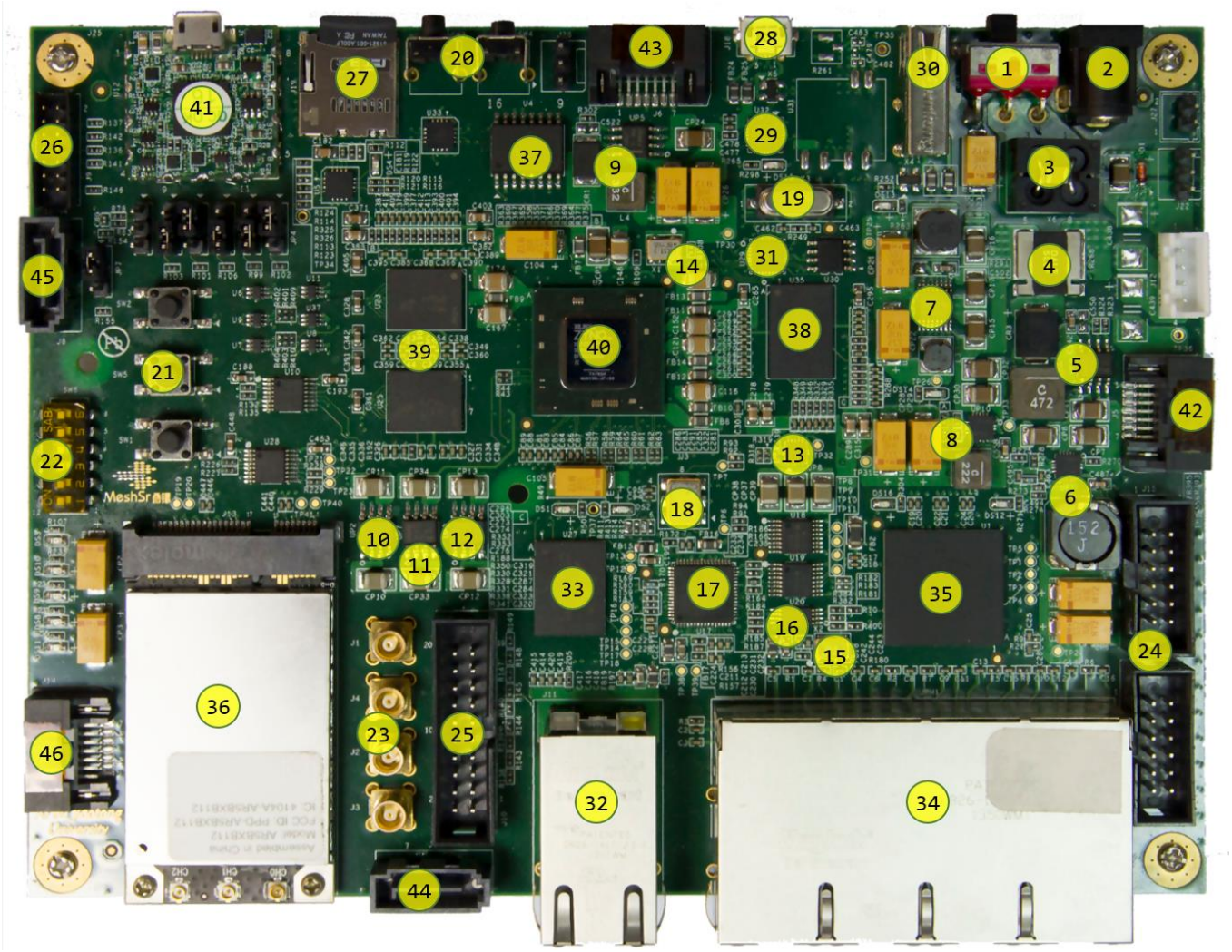

Figure 3 ONetSwitch30 Board Compent Locations

Table 2 ONetSwitch30 Components Descriptions

Callout	Component Description	Reference Designator	Notes
1	Power On/Off Switch	J21	SIP_PWR_SW_3P
2	12V Power input connector	J20	2.5mm 12V DC10B
3	Power filter	X6	BNX016
4	Power Metal Strip Resistors	R268	WSL36375L000FEB 0.005Ω
5	DC-DC Converter 5V	UP9	TPS54531
6	DC-DC Converter 1.0V	UP1	TPS54620
7	DC-DC Converter 1.8V,2.5V	UP4	TPS54294
8	DC-DC Converter 1.5V	UP10	TPS54620
9	DC-DC Converter 3.3V	UP5	TPS54531
10	LDO 1.1V for GTX	UP2	TPS7A7001DDA

11	LDO 1.8V for GTX	UP7	TPS7A7001DDA
12	LDO 1.2V for GTX	UP3	TPS7A7001DDA
13	DDR Termination 0.75V	UP8	TPS51200DRCT
14	Oscillator 33MHz	X1	33.33MHz PS work clock
15	Oscillator 25MHz	X2	25MHz Data-plane Source Clock
16	Single-end Clock Buffer	U20	CDCV304, 25MHz clock distribute
17	Clock Generator	U17	AD9516-3, multi-output clock generator
18	Oscillator for GTX	U3	156.25MHz GTX Reference Clock
19	Oscillator 24MHz	X3	24MHz, USB3320 Reference Clock
20	Reset Key	SW3,4	Push Button x2 (POR_B/SRST_B)
21	User Key	SW1,2,5	Push Button x3
22	DIP Switch	SW6	6bits DIP switch
23	SMA Connector	J1,2,3,4	Clock input/output
24	PMOD Connector	J15, J16	12 pin
25	PJTAG Connector	J10	20 pin
26	JTAG-14pin Connector	J9	14 pin
27	TF Card Connector	J19	47334-0001
28	USB UART	J18	47589-0001 USB Micro B port
29	USB-to-UART Bridge	U32	CP2103
30	USB Connector	J17	48204-0001 USB A port
31	USB Transceiver	U29	USB3320
32	PS RJ45 1G*1	J11	0826-1X1T-23-F MegJack 10/100/1000 LAN
33	PS PHY	U27	88E1111 PHY
34	PL RJ45 1G*4	JPH1	0826-1X4T-23-F MegJack 10/100/1000 LAN
35	PL PHY	U1	VSC8574 PHY
36	Mini PCIe Slot	J13	Atheros AR9380 AR5BXB112
37	SPI Flash	U4	N25Q256A13ESF40G
38	PS DRAM	U35,36	DDR3 MT41K256M16HA-125 x2
39	PL DRAM	U23,24,25,26	DDR3 MT41K512M8RH-125 x2
40	Zynq	U2	XC7Z030
41	USB JTAG	U12	Digilent USB JTAG SMT2
42	GTX Connector	J5	SATA connector, interface to PL-side GTX2
43	GTX Connector	J6	SATA connector, interface to PL-side GTX0
44	GTX Connector	J7	SATA connector, interface to PL-side GTX1
45	GTX Connector	J8	SATA connector, interface to PL-side GTX3
46	GTX Connector	J14	SATA connector, interface to Mini PCIe connector

1.4 Bank Description

Table 3 Zynq Bank Assignments

Bank	I/O Power supply	Feature
500(MIO 0)	3.3V	QSPI, Reset
501(MIO 1)	2.5V	USB-UART, PS RJ45, USB, SD, GPIO(AD9516-3 programming)
502(DDR)	1.5V	DDR3
13(High Range)	2.5V	SGMII,PMOD,PJTAG
34(High Perf.)	1.5V	DDR3,Push button, DIP switch
35(High Perf.)	1.5V	DDR3
112(GTX)		6.6G SERDES

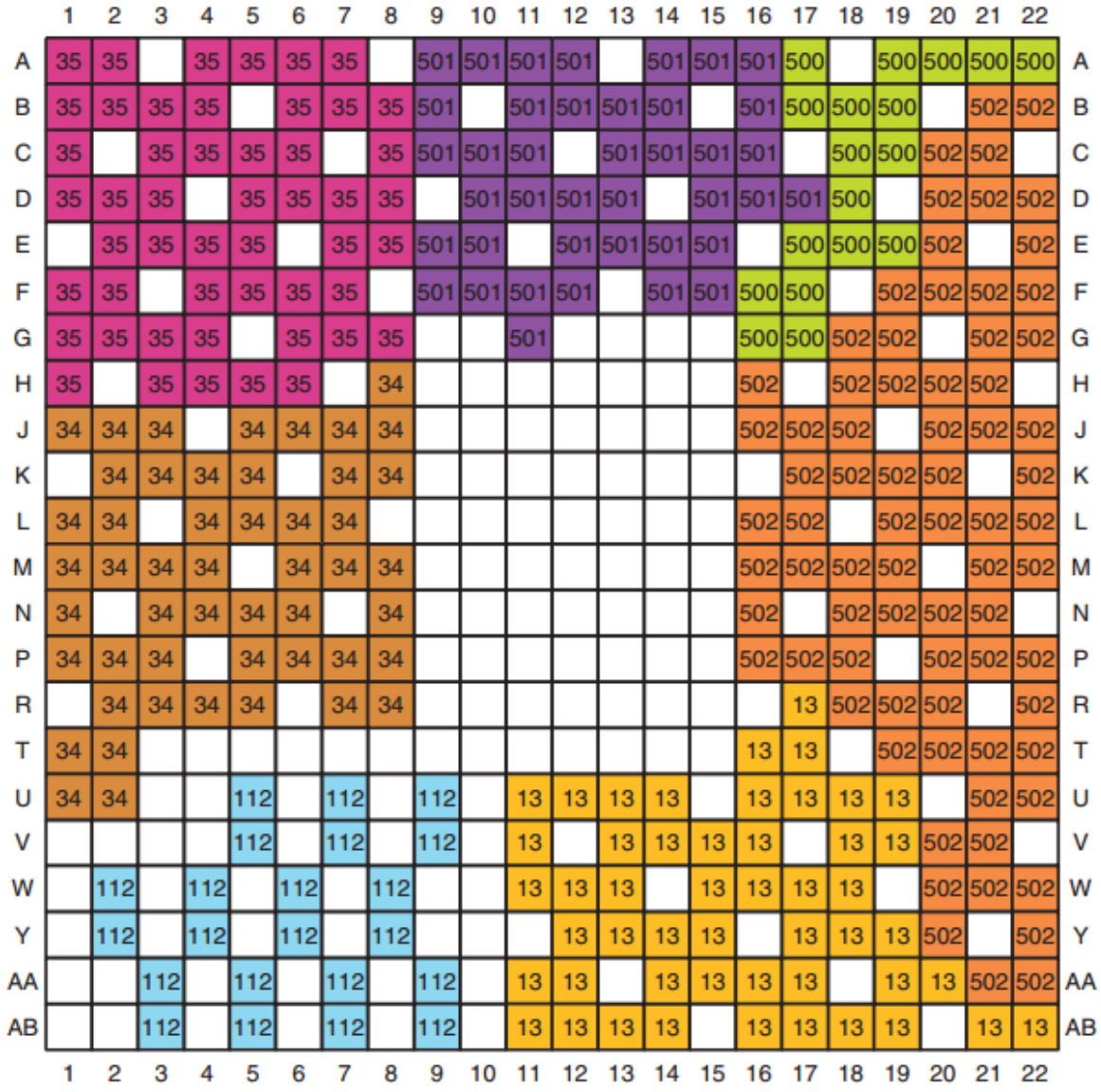

Figure 4 Xilinx Zynq SoC Package(XC7Z030-2SBG485)

2 Feature Descriptions

2.1 Xilinx Zynq SoC

The ONetSwitch30 is populated with the Xilinx Zynq™-7000 XC7Z030-2SBG485 AP SoC.

The XC7Z030 AP SoC consists of an integrated processing system (PS) an programmable logic (PL), on a single die.

Information for the Xilinx Zynq AP SoC specification can be found at the documents released by Xilinx.

2.1.1 Device Configuration

The ONetSwitch30 supports two configuration options:

- ✓ QSPI flash memory, PS Configuration, Master Mode Boot;
- ✓ TF Card, PS Configuration, Master Mode Boot.

The JP2 and JP6 maintain '0'(connect pin2 and pin3) by default. The JP3, JP4 and JP5 will be set depending on the desire boot mode, QSPI Flash or TF Card.

Table 4 Configuration Option Settings

Pin-signal	**MIO[8]**	**MIO[7]**	**MIO[6]**	**MIO[5]**	**MIO[4]**	**MIO[3]**	**MIO[2]**
Mode	**vmode[1]**	**vmode[0]**	**boot_mode[4]**	**boot_mode[0]**	**boot_mode[2]**	**boot_mode[1]**	**boot_mode[3]**
Boot Mode				1 (JP3 1-2)	1 (JP4 1-2)	1 (JP5 1-2)	
				0 (JP3 2-3)	0 (JP4 2-3)	0 (JP5 2-3)	
Mode for all 3 PLLs							
PLL Enable			1 (JP2 1-2)				
PLL Bypassed			0 (JP2 2-3)				
MIO Bank Voltage							
2.5V,3.3V	GND	GND					
JTAG Chain Routing							
Cascade Mode							1 (JP6 1-2)
Independent Mode							0 (JP6 2-3)

2.1.2 Debugging

The ONetSwitch30 provides 3 options for debugging. The USB JTAG and the JTAG-14pin are selected by JP7 for PL debug. The PJTAG is used for ARM debug

- ✓ USB JTAG, PL JTAG;
- ✓ JTAG-14pin, PL JTAG;
- ✓ PJTAG-20pin, EMIO PJTAG.

Table 5 Debugging options and settings

Debugging Option	**Jumper**	**Description**
USB JTAG	JP7 1-2	Micro USB port
JTAG-14pin	JP7 2-3	Xilinx Platform Cable
PJTAG-20pin	-	ARM Debug

2.2 Clock Source

The ONetSwitch30 has six Clock sources.

Table 6 Clock Sources

#	Device	Reference	Description
1	Oscillator 33MHz	X1	33.33MHz PS work clock
2	Oscillator 25MHz	X2	25MHz Data-plane Source Clock
3	Crystal 24MHz	X3	24MHz USB 3320 Reference Clock
4	Oscillator GTX	U3	156.25MHz GTX Reference Clock
5	Single-end clock buffer	U20	CDCV304, 25MHz clock distribute
6	Multi-output clock generator	U17	AD9156-3

Table 7 Clock connections

#	Clock Generator:Pin	Net Name	Destiny Device:Pin	Description
1	X1.3	PS_CLK_33M	U2C.F16	33.33MHz PS work clock
2	X2.3	CRYSTAL_25M_CLK	U20.1	Data-plane Source Clock
3	U20.3	AD9516_25M_CLK	U17.64	25MHz AD9516-3 Reference Clock
4	U20.5	SYS_25M_CLK	U2A.Y18	FPGA system clock
5	U20.7	PS_PHY_REF_25M_CLK	U27.H9	25MHz 88E1111 PHY
6	U20.9	PL_PHY_REF_25M_CLK	U1E.D1	Backups 25MHz VSC8574 PHY
7	X3.1	REFCLK_26	U29.26	24MHz USB 3320 Reference Clock
	X3.2	XO_25	U29.25	
8	U3.4	CLK_156M_SI57x_P	U2B.U9	156.25MHz GTX Reference Clock
	U3.5	CLK_156M_SI57x_N	U2B.V9	
9	U17.56	FPGA_SGMII_REF125M_CLK_P	U2A.Y14	OUT0: Zynq AP SoC SGMII Reference Clock
	U17.55	FPGA_SGMII_REF125M_CLK_N	U2A.Y15	
	U17.48	PCIE_REFCLK_100M_P	J13.13	OUT6: Mini PCIe Slot Reference Clock
	U17.47	PCIE_REFCLK_100M_N	J13.11	
	U17.46	GTX_PCIE_CLK_100M_P	U2B.U5	OUT7: PCIe GTX Reference Clock
	U17.45	GTX_PCIE_CLK_100M_N	U2B.V5	
	U17.33	PL_PHY_1588_125M_CLK_P	U1E.J15	OUT8: 125MHz VSC8574 1588
	U17.34	PL_PHY_1588_125M_CLK_N	U1E.J16	
	U17.35	PL_PHY_REF125M_CLK_P	U1E.D1	OUT9: 125MHz VSC8574 PHY
	U17.36	PL_PHY_REF125M_CLK_N	U1E.C1	

2.2.1 PS work clock

The Processing System (PS) clock source is a 3.3V LVCMOS single-ended fixed 33.333MHz oscillator at X1.

- ✓ Part number: ASFLMB-33.3-LY-T
- ✓ Frequency: 33.333MHz
- ✓ Stability: 10ppm
- ✓ Output Standard: 3.3V LVCMOS

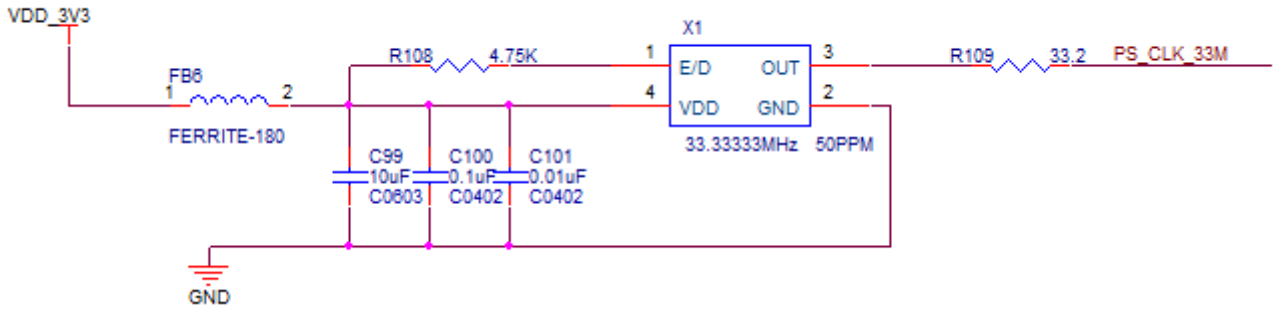

Figure 5 X1 Oscillator circuit

2.2.2 Data plane source clock

The X2 oscillator is used as data-plane source clock, connect to single-end clock buffer U20.

- ✓ Part number: ASFLMB-25-XY-T
- ✓ Frequency: 25MHz
- ✓ Stability: 30ppm
- ✓ Output Standard: 3.3V LVCMOS

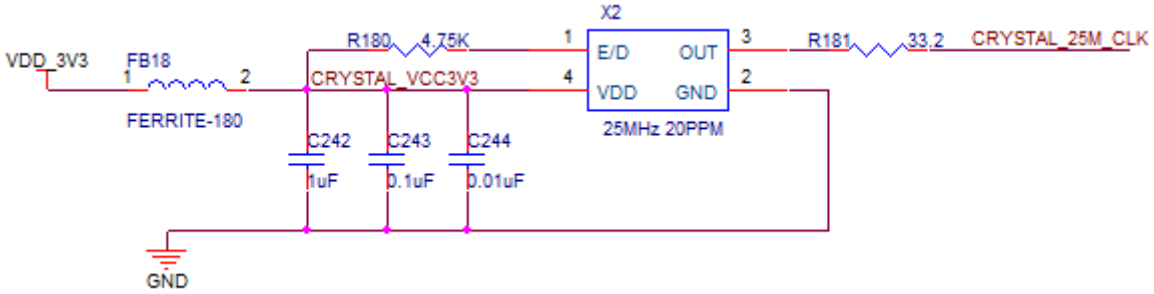

Figure 5 X3 Oscillator circuit

2.2.3 USB 3320 Reference Clock

The X3 oscillator is the reference clock of USB 3320.

- ✓ Part number: HCM49-24.000MABJ-UT
- ✓ Frequency: 24MHz
- ✓ Stability: 50ppm
- ✓ Output Standard: Depend on host chip

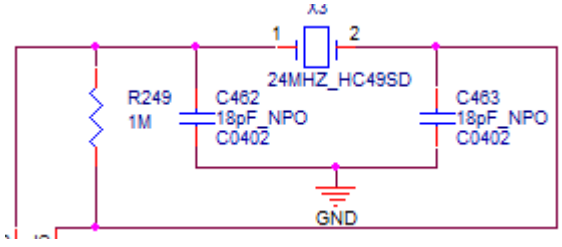

Figure 6 X3 Crystal circuit

2.2.4 GTX Reference Clock

The GTX transceiver has two reference clock inputs. One is connect to PCIe reference clock from AD9516-3, another is feed by a low-jitter LVPECL differential oscillator U3.

- ✓ Part number: KC7050P156.250L30E00
- ✓ Frequency: 156.25MHz
- ✓ Stability: 50ppm
- ✓ Output Standard: LVPECL

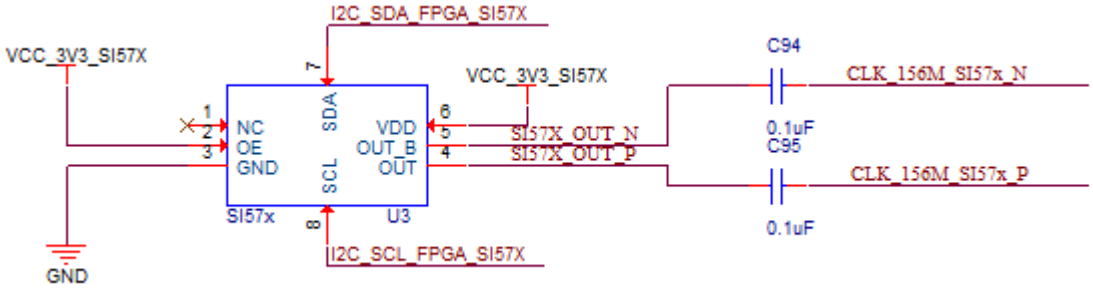

Figure 8 U3 Oscillator circuit

2.2.5 Single-end Clock Buffer

The CDCV304 is a single-end clock buffer. It distributes one input 25MHz clock to four output. Reference U20.

- ✓ Part number: CDCV304PWR
- ✓ Frequency: Depend on input
- ✓ Output Standard: 3.3V LVCMOS

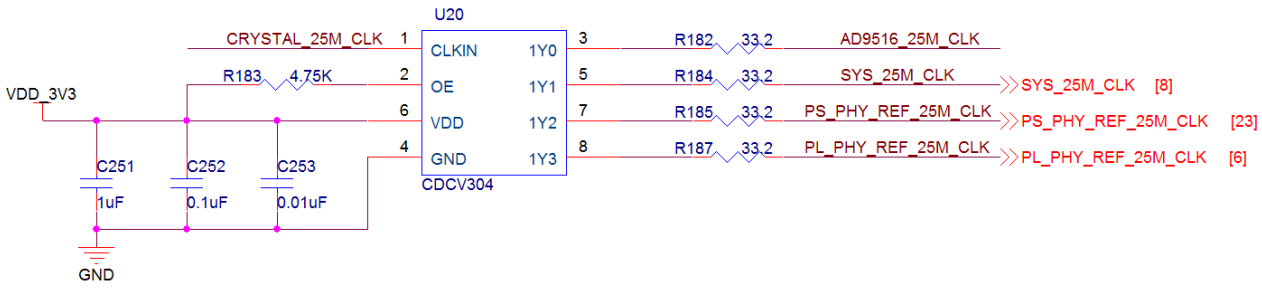

Figure 9

U20 Single-end clock buffer circuit

2.2.6 AD9516-3 multi-output clock Generator

The most important clock generator of ONetSwitch30 is AD9516-3 (U17). Its reference clock is 25MHz single-end clock from clock buffer U20. The AD9516-3 generates several low jitter differential clock to clocking XC7Z030 AP SoC, such as SGMII 125MHz, PCIe 100MHz, etc. It also provides the reference clock for VSC8574 (125MHz) and mini PCIe Slot (100MHz).

The AD9516-3 should be programmed through serial control port which interfaces to the Processing System. For more detailed information, please refer to AD9516-3 DATASHEET.

Table 8 AD9516-3 Serial Control Port Connections, to XC7Z030 AP SoC

Bank	Net Name	Zynq Pin	Direction	Description
501	MIO_46_AD9516_SDI	E17	INOUT	GPIO
501	MIO_47_AD9516_SDO	B19	INOUT	GPIO
501	MIO_48_AD9516_SCLK	B21	INOUT	GPIO
501	MIO_49_AD9516_CS_N	A18	INOUT	GPIO

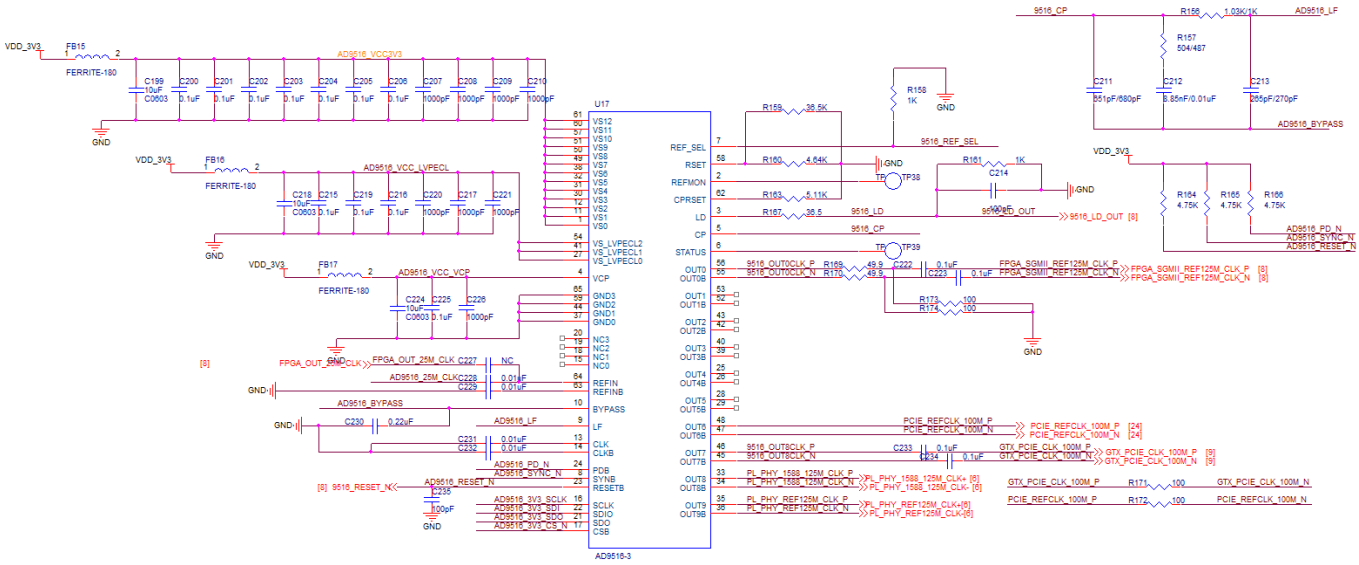

Figure 10 AD9156-3 circuit

2.3 QSPI Flash

The ONetSwitch30 features a QSPI serial NOR Flash. The SPI Flash memory is used to provide non-volatile code, and data storage. It can be used to initialize the PS subsystem as well as configure the PL subsystem.

- ✓ Part number: N25Q128A11ESF40
- ✓ Operating voltage: 3.3V
- ✓ Datapath with: 4bits
- ✓ Data rate: Various depending on x1,x2,and x4 mode

Table 9 QSPI Flash Pin Assignment

Bank	Net Name	Zynq Pin	Direction	Description
500	MIO_1_QSPI_0_CS_B	A22	OUT	Chip Select
500	MIO_2_QSPI_0_IO0	A21	INOUT	Data0
500	MIO_3_QSPI_0_IO1	F17	INOUT	Data1
500	MIO_4_QSPI_0_IO2	E19	INOUT	Data2
500	MIO_5_QSPI_0_IO3	A20	INOUT	Data3
500	MIO_6_QSPI_0_CLK	A19	OUT	Serial Data Clock
500	MIO_8_QSPI_FB_CLK	E18	OUT	QSPI Feedback

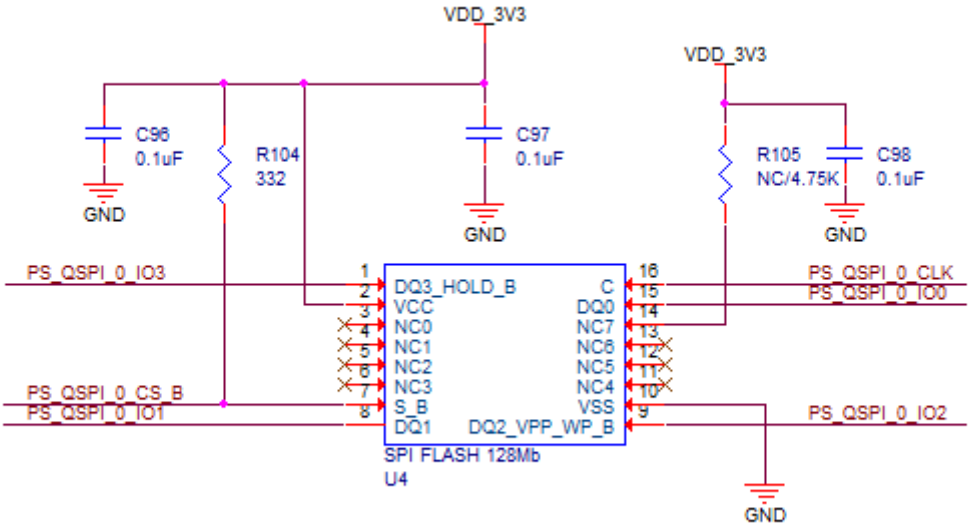

Figure 11 QSPI circuit

2.4 PS DDR3

The 1 GB,32-bit wide DDR3 component memory system is comprised of two 512Mb x16 DDR3 SDRAMs (MT41K256M16HA-125).This memory system is connected to the XC7Z030 AP SoC Processing System (PS) memory interface bank 502. The connections between the DDR3 component memory and XC7Z030 AP SoC bank 502 are listed in Table 10.

Table 10 DDR3 Memory Connections to PS

Bank	Net Name	Zynq Pin	Direction	Description
502	DDR3_DQ_0	D22	INOUT	I/O Data
502	DDR3_DQ_1	C20	INOUT	I/O Data
502	DDR3_DQ_2	B21	INOUT	I/O Data
502	DDR3_DQ_3	D20	INOUT	I/O Data
502	DDR3_DQ_4	E20	INOUT	I/O Data
502	DDR3_DQ_5	E22	INOUT	I/O Data
502	DDR3_DQ_6	F21	INOUT	I/O Data
502	DDR3_DQ_7	F22	INOUT	I/O Data
502	DDR3_DQ_8	G21	INOUT	I/O Data
502	DDR3_DQ_9	G22	INOUT	I/O Data
502	DDR3_DQ_10	L22	INOUT	I/O Data
502	DDR3_DQ_11	L21	INOUT	I/O Data
502	DDR3_DQ_12	L20	INOUT	I/O Data
502	DDR3_DQ_13	K22	INOUT	I/O Data
502	DDR3_DQ_14	J22	INOUT	I/O Data
502	DDR3_DQ_15	K20	INOUT	I/O Data
502	DDR3_DQ_16	M22	INOUT	I/O Data
502	DDR3_DQ_17	T20	INOUT	I/O Data
502	DDR3_DQ_18	N20	INOUT	I/O Data
502	DDR3_DQ_19	T22	INOUT	I/O Data
502	DDR3_DQ_20	R20	INOUT	I/O Data
502	DDR3_DQ_21	T21	INOUT	I/O Data
502	DDR3_DQ_22	M21	INOUT	I/O Data
502	DDR3_DQ_23	R22	INOUT	I/O Data
502	DDR3_DQ_24	Y20	INOUT	I/O Data
502	DDR3_DQ_25	U22	INOUT	I/O Data
502	DDR3_DQ_26	AA22	INOUT	I/O Data
502	DDR3_DQ_27	U21	INOUT	I/O Data
502	DDR3_DQ_28	W22	INOUT	I/O Data
502	DDR3_DQ_29	W20	INOUT	I/O Data
502	DDR3_DQ_30	V20	INOUT	I/O Data
502	DDR3_DQ_31	Y22	INOUT	I/O Data
502	DDR3_A_0	M19	OUT	Address
502	DDR3_A_1	M18	OUT	Address
502	DDR3_A_2	K19	OUT	Address
502	DDR3_A_3	L19	OUT	Address

502	DDR3_A_4	K17	OUT	Address
502	DDR3_A_5	K18	OUT	Address
502	DDR3_A_6	J16	OUT	Address
502	DDR3_A_7	J17	OUT	Address
502	DDR3_A_8	J18	OUT	Address
502	DDR3_A_9	H18	OUT	Address
502	DDR3_A_10	J20	OUT	Address
502	DDR3_A_11	G18	OUT	Address
502	DDR3_A_12	H19	OUT	Address
502	DDR3_A_13	F19	OUT	Address
502	DDR3_A_14	G19	OUT	Address
502	DDR3_BA_0	L16	OUT	Bank Address
502	DDR3_BA_1	L17	OUT	Bank Address
502	DDR3_BA_2	M17	OUT	Bank Address
502	DDR3_DQS_0_P	C21	INOUT	I/O Differential data strobe
502	DDR3_DQS_0_N	D21	INOUT	I/O Differential data strobe
502	DDR3_DQS_1_P	H21	INOUT	I/O Differential data strobe
502	DDR3_DQS_1_N	J21	INOUT	I/O Differential data strobe
502	DDR3_DQS_2_P	N21	INOUT	I/O Differential data strobe
502	DDR3_DQS_2_N	P21	INOUT	I/O Differential data strobe
502	DDR3_DQS_3_P	V21	INOUT	I/O Differential data strobe
502	DDR3_DQS_3_N	W21	INOUT	I/O Differential data strobe
502	DDR3_DM_0	B22	OUT	Data mask
502	DDR3_DM_1	H20	OUT	Data mask
502	DDR3_DM_2	P22	OUT	Data mask
502	DDR3_DM_3	AA21	OUT	Data mask
502	DDR3_RESET_B	F20	OUT	Reset
502	DDR3_CLK_P	N19	OUT	Differential clock output
502	DDR3_CLK_N	N18	OUT	Differential clock output
502	DDR3_CKE	T19	OUT	Clock enable
502	DDR3_CS_B	P17	OUT	Chip select
502	DDR3_WE_B	R19	OUT	Write enable
502	DDR3_CAS_B	P20	OUT	RAS column address select
502	DDR3_RAS_B	R18	OUT	RAS row address select
502	DDR3_ODT	P18	OUT	Output dynamic termination
502	DDR3_VRP	N16	OUT	I/O Used to calibrate input termination
502	DDR3_VRN	M16	OUT	I/O Used to calibrate input termination
502	DDR3_VREF0	H16		I/O Reference voltage
502	DDR3_VREF1	P16		I/O Reference voltage

2.5 PS Ethernet

The ONetSwitch30 uses the Marvell Alaska PHY device 88E1111 for Ethernet communications at 10/100/1000 Mb/s. The PHY connects to MIO Bank 501 and interfaces to the Processing System (PS) via RGMII. The connections from the XC7Z030 AP SoC to 88E1111 are listed in Table 11.

Table 11 PS Ethernet Connections, XC7Z030 AP SoC to PHY

Bank	Net Name	Zynq Pin	Direction	Description
500	MIO_10_PS_PHY_RST_N	G16	OUT	Reset
501	MIO_16_PHY_RGMII_TX_CLK	D17	OUT	TX
501	MIO_17_PHY_RGMII_TXD_0	E14	OUT	
501	MIO_18_PHY_RGMII_TXD_1	A16	OUT	
501	MIO_19_PHY_RGMII_TXD_2	E13	OUT	
501	MIO_20_PHY_RGMII_TXD_3	A15	OUT	
501	MIO_21_PHY_RGMII_TX_CTRL	F12	OUT	
501	MIO_22_PHY_RGMII_RX_CLK	A9	IN	RX
501	MIO_23_PHY_RGMII_RXD_0	E12	IN	
501	MIO_24_PHY_RGMII_RXD_1	B16	IN	
501	MIO_25_PHY_RGMII_RXD_2	F11	IN	
501	MIO_26_PHY_RGMII_RXD_3	A10	IN	
501	MIO_27_PHY_RGMII_RX_CTRL	D16	IN	
501	MIO_52_PHY_MDC	D13	OUT	MDIO
501	MIO_53_PHY_MDIO	C11	INOUT	

2.6 TF Card

The ONetSwitch30 includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards (Micro SD-TF Card). The SDIO signals are connected to XC7Z030 AP SoC PS bank 501 which has its VCCMIO set to 2.5V. A MAX13035E high-speed logic-level translator is used between XC7Z030 AP SoC 2.5V PS bank 501 and the 3.3V TF card connector.

Table 12 lists the TF card interface connections to the XC7Z030 AP SoC.

Table 12 SDIO Connections to the XC7Z03 AP SoC

Bank	Net Name	Zynq Pin	Direction	Description
501	MIO_40_SD_CLK	E9	OUT	Clock
501	MIO_41_SD_CMD	C15	OUT	Command
501	MIO_42_SD_DAT_0	D15	INOUT	Data
501	MIO_43_SD_DAT_1	B12	INOUT	
501	MIO_44_SD_DAT_2	E10	INOUT	
501	MIO_45_SD_CD_DAT_3	B14	INOUT	

2.7 USB

The ONetSwitch30 uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver to support a USB connection to the host computer. The USB peripheral is used on the PS, connected in MIO Bank 501.

The connections between the USB Transceiver and the XC7Z030 AP SoC are listed in Table 13.

Table 13 USB Transceiver Connections to the XC7Z030 AP SoC

Bank	Net Name	Zynq Pin	Direction	Description
501	MIO_32_USB_DATA_0	C16	INOUT	USB Data lines
501	MIO_33_USB_DATA_1	G11	INOUT	
501	MIO_34_USB_DATA_2	B11	INOUT	
501	MIO_35_USB_DATA_3	F9	INOUT	
501	MIO_28_USB_DATA_4	A11	INOUT	
501	MIO_37_USB_DATA_5	B9	INOUT	
501	MIO_38_USB_DATA_6	F10	INOUT	
501	MIO_39_USB_DATA_7	C10	INOUT	
501	MIO_29_USB_DIR	E15	IN	ULPI DIR signal
501	MIO_30_USB_STP	A12	OUT	ULPI STR signal
501	MIO_31_USB_NXT	F14	IN	ULPI NXT signal
501	MIO_36_USB_CLKOUT	A14	IN	USB Clock

2.8 USB-UART

The ONetSwitch30 contains a Silicon Labs CP2103GM USB-to-UART bridge device which allows a connection to a host computer with a USB port. The CP2103GM TX and RX pins are wired to the UART_1 IP block within the XC70Z30 AP SoC PS I/O Peripherals set.

Table 14 lists the USB connections between the XC7Z030 AP SoC PS Bank 501 and the CP2103 UART bridge.

Table 14 XC7Z030 AP SoC to CP2103 Connections

Bank	Net Name	Zynq Pin	Direction	Description
501	MIO_50_USB_UART_RX	D10	IN	Data in
501	MIO_51_USB_UART_TX	C13	OUT	Data out

2.9 JTAG

The ONetSwitch30 JTAG chain is shown in Figure 12. The PL JTAG chain can be programmed by two methods, controlled by jumper JP4.

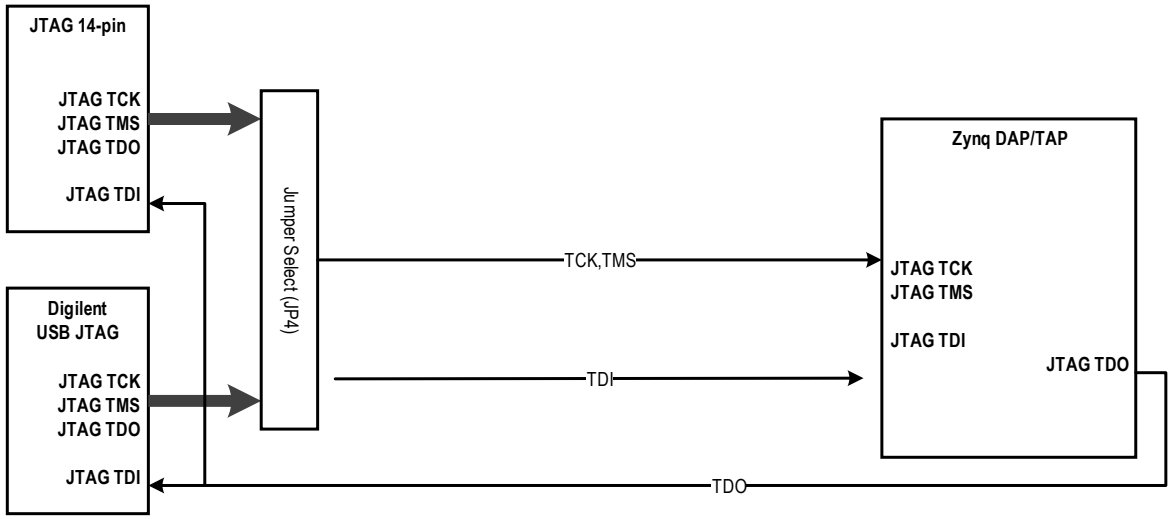

Figure 72 JTAG Chain Block Diagram

PJTAG is used for ARM debug, located at PL-Side.

Table 15 EMIO PJTAG

Bank	Net Name	Zynq Pin	Direction	Description
13	PJTAG_PS_BUF_TCK	T16	IN	
13	PJTAG_PS_BUF_TMS	V14	IN	
13	PJTAG_PS_BUF_TDO	V13	OUT	
13	PJTAG_PS_BUF_TDI	V15	IN	

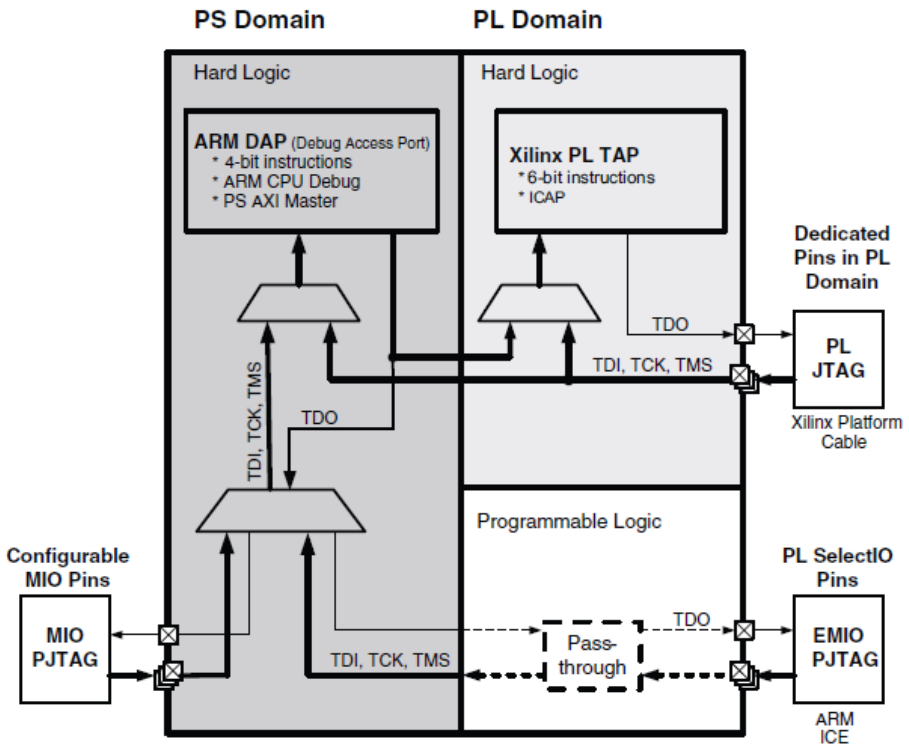

Figure 83 JTAG Debug Trace Port

Key features of the JTAG debug interface are:

- ✓ JTAG 1149.1 boundary scan support
- ✓ Two 1149.1 compliance TAP controllers:One JTAG TAP controller and one ARM DAP
- ✓ Single unique IDCODE from the xilinx TAP for each of the Zynq 7000 family of devices
- ✓ IEEE 1532 programming in-system configurable (ISC) devices support
- ✓ QSPI flash programming
- ✓ Xilinx ISE Chipscope and Vivado Hardware Manager debug support
- ✓ ARM CoreSight debug center control using ARM DAP
- ✓ Indirect PS address space access through DAP-AP port

2.10 PL DDR3

The 2GB, 32-bit wide DDR3 component memory system is comprised of four 512Mb x 8 SDRAMs (MT41K512M8RH-125). It provides volatile synchronous dynamic random access memory (SDRAM) for storing user code and data. The DDR3 interface is implemented across the PL-side I/O banks. Bank 34 and Bank 35 have a dedicated DCI VRP/N resistor connection. An external 0.75V reference VTT_REF_PL_0V75 is provided for data interface banks.

The connections between the DDR3 memory and XC7Z030 AP SoC are listed in Table 16.

Table 16 DDR-PL Connections to the XC7Z030 AP SoC

Bank	Net Name	Zynq Pin	Direction	Description
34	PL_DDR3_A0	J6	OUT	SSTL15
34	PL_DDR3_A1	M1	OUT	SSTL15
34	PL_DDR3_A2	J8	OUT	SSTL15
34	PL_DDR3_A3	K8	OUT	SSTL15
34	PL_DDR3_A4	P1	OUT	SSTL15
34	PL_DDR3_A5	N1	OUT	SSTL15
34	PL_DDR3_A6	M8	OUT	SSTL15
34	PL_DDR3_A7	M6	OUT	SSTL15
34	PL_DDR3_A8	P8	OUT	SSTL15
34	PL_DDR3_A9	M2	OUT	SSTL15
34	PL_DDR3_A10	J3	OUT	SSTL15
34	PL_DDR3_A11	R2	OUT	SSTL15
34	PL_DDR3_A12	L7	OUT	SSTL15
34	PL_DDR3_A13	P3	OUT	SSTL15
34	PL_DDR3_A14	R3	OUT	SSTL15
34	PL_DDR3_A15	K5	OUT	SSTL15
34	PL_DDR3_BA0	L6	OUT	SSTL15
34	PL_DDR3_BA1	J7	OUT	SSTL15
34	PL_DDR3_BA2	J5	OUT	SSTL15
34	PL_DDR3_RESET_B	N8	OUT	SSTL15
34	PL_DDR3_ODT	J2	OUT	SSTL15
34	PL_DDR3_RAS_B	J1	OUT	SSTL15
34	PL_DDR3_CAS_B	L1	OUT	SSTL15
34	PL_DDR3_WE_B	L2	OUT	SSTL15
34	PL_DDR3_CS_B	K4	OUT	SSTL15
34	PL_DDR3_CKE	K2	OUT	SSTL15
34	PL_DDR3_CLK_P	U2	OUT	DIFF_SSTL15
34	PL_DDR3_CLK_N	U1	OUT	DIFF_SSTL15
34	VTT VREF PL 0V75	M7	N/A	LVCMOS15
34	VTT VREF PL 0V75	N5	N/A	LVCMOS15
35	PL_DDR3_DQS0_P	E8	INOUT	DIFF_SSTL15
35	PL_DDR3_DQS0_N	D8	INOUT	DIFF_SSTL15
35	PL_DDR3_DQS1_P	A7	INOUT	DIFF_SSTL15
35	PL_DDR3_DQS1_N	A6	INOUT	DIFF_SSTL15
35	PL_DDR3_DQS2_P	A2	INOUT	DIFF_SSTL15
35	PL_DDR3_DQS2_N	A1	INOUT	DIFF_SSTL15
35	PL_DDR3_DQS3_P	E4	INOUT	DIFF_SSTL15
35	PL_DDR3_DQS3_N	E3	INOUT	DIFF_SSTL15
35	PL_DDR3_DM0	G6	OUT	SSTL15

Bank	Net Name	Zynq Pin	Direction	Description
35	PL_DDR3_DM1	D5	OUT	SSTL15
35	PL_DDR3_DM2	B2	OUT	SSTL15
35	PL_DDR3_DM3	H4	OUT	SSTL15
35	PL_DDR3_DQ0	E7	INOUT	SSTL15
35	PL_DDR3_DQ1	D6	INOUT	SSTL15
35	PL_DDR3_DQ2	F7	INOUT	SSTL15
35	PL_DDR3_DQ3	G7	INOUT	SSTL15
35	PL_DDR3_DQ4	D7	INOUT	SSTL15
35	PL_DDR3_DQ5	F5	INOUT	SSTL15
35	PL_DDR3_DQ6	G8	INOUT	SSTL15
35	PL_DDR3_DQ7	E5	INOUT	SSTL15
35	PL_DDR3_DQ8	B6	INOUT	SSTL15
35	PL_DDR3_DQ9	B7	INOUT	SSTL15
35	PL_DDR3_DQ10	A5	INOUT	SSTL15
35	PL_DDR3_DQ11	C6	INOUT	SSTL15
35	PL_DDR3_DQ12	A4	INOUT	SSTL15
35	PL_DDR3_DQ13	C8	INOUT	SSTL15
35	PL_DDR3_DQ14	C5	INOUT	SSTL15
35	PL_DDR3_DQ15	B8	INOUT	SSTL15
35	PL_DDR3_DQ16	C3	INOUT	SSTL15
35	PL_DDR3_DQ17	C1	INOUT	SSTL15
35	PL_DDR3_DQ18	B3	INOUT	SSTL15
35	PL_DDR3_DQ19	E2	INOUT	SSTL15
35	PL_DDR3_DQ20	D3	INOUT	SSTL15
35	PL_DDR3_DQ21	D1	INOUT	SSTL15
35	PL_DDR3_DQ22	B4	INOUT	SSTL15
35	PL_DDR3_DQ23	D2	INOUT	SSTL15
35	PL_DDR3_DQ24	G2	INOUT	SSTL15
35	PL_DDR3_DQ25	F2	INOUT	SSTL15
35	PL_DDR3_DQ26	H1	INOUT	SSTL15
35	PL_DDR3_DQ27	F1	INOUT	SSTL15
35	PL_DDR3_DQ28	G1	INOUT	SSTL15
35	PL_DDR3_DQ29	F4	INOUT	SSTL15
35	PL_DDR3_DQ30	G4	INOUT	SSTL15
35	PL_DDR3_DQ31	G3	INOUT	SSTL15
35	PL_DDR_VRP	H5	OUT	SSTL15
35	PL_DDR_VRN	H6	OUT	SSTL15
35	QDR_VRP	K12		
35	QDR_VRN	H16		
35	VTT VREF PL 0V75	F6		
35	VTT VREF PL 0V75	H3		

2.11 PL Ethernet 1G

One Vitesse VSC8574 Ethernet transceiver (PHY) are provided to interface to network connections via a Belfuse 0826-1X4T-23-F RJ-45 connector with built-in magnetics. The PHY MUST be programmed via a MDIO bus to work appropriate.

VSC8574 supports four dual media copper ports with SGMII interfaces. For more detailed information, please refer to VSC8571 datasheet.

- ✓ PHY address setting: PHYA[4:2]='100', start address is '10', increase.
- ✓ Mode setting is made by MDIO configuration.

For more detailed information about PL HDL coding, please refer to Xilinx LogiCORE IP AXI Ethernet related documents on the Xilinx website.

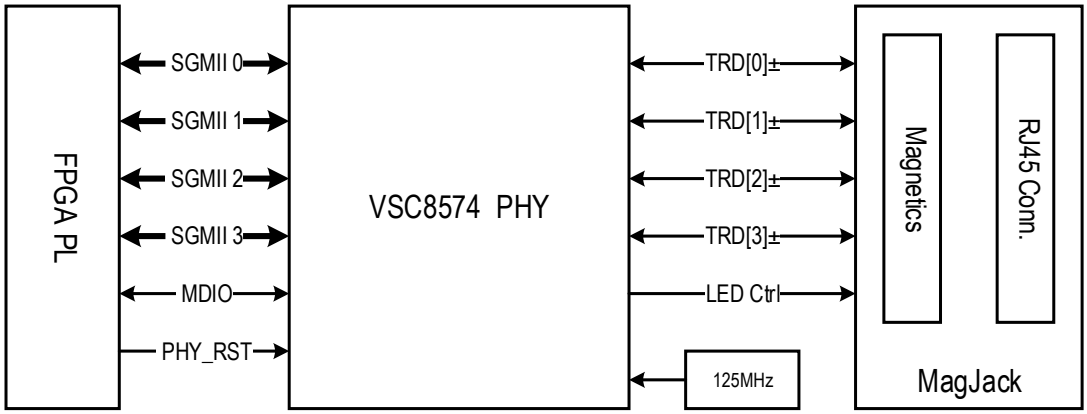

Figure 94 PL Ethernet 1G Block Diagram

The Ethernet connections from the XC7Z030 AP SoC PL to the VSC8574 PHY device are listed in Table 17.

Table 17 PL Ethernet 1G Connections, XC7Z030 AP SoC to VSC8574 PHY

Bank	Net Name	Zynq Pin	Direction	Description
12	SGMII_0_RDPRE_P	AA12	IN	LVDS_25
12	SGMII_0_RDPRE_N	AB12	IN	LVDS_25
12	PHY_SGMII_0_TD_P	AA11	OUT	LVDS_25
12	PHY_SGMII_0_TD_N	AB11	OUT	LVDS_25
12	SGMII_1_RDPRE_P	AB13	IN	LVDS_25
12	SGMII_1_RDPRE_N	AB14	IN	LVDS_25
12	PHY_SGMII_1_TD_P	Y12	OUT	LVDS_25
12	PHY_SGMII_1_TD_N	Y13	OUT	LVDS_25
12	SGMII_2_RDPRE_P	AB18	IN	LVDS_25
12	SGMII_2_RDPRE_N	AB19	IN	LVDS_25
12	PHY_SGMII_2_TD_P	AB16	OUT	LVDS_25
12	PHY_SGMII_2_TD_N	AB17	OUT	LVDS_25
12	SGMII_3_RDPRE_P	AB21	IN	LVDS_25
12	SGMII_3_RDPRE_N	AB22	IN	LVDS_25
12	PHY_SGMII_3_TD_P	AA19	OUT	LVDS_25
12	PHY_SGMII_3_TD_N	AA20	OUT	LVDS_25
12	FPGA_SGMII_REF125M_CLK_P	Y14	IN	LVDS_25
12	FPGA_SGMII_REF125M_CLK_N	Y15	IN	LVDS_25
12	PL_PHY_FLNKFAIL	W15	IN	LVCMOS25
12	PL_PHY_RCVRD_CLK	AA14	IN	LVCMOS25
12	PL_PHY_1588_LS	AA17	IN	LVCMOS25
12	PL_PHY_MDC	W16	OUT	LVCMOS25
12	PL_PHY_MDIO	W17	INOUT	LVCMOS25

2.12 Mini PCIe

The ONetSwitch30 has a Mini PCIe Slot interface to XC7Z030 AP SoC PL-side GTX transceiver for wireless access (such as Atheros AR9380 3x3 MIMO 802.11 b/g/n WIFI module) or storage install (SSD). The XC7Z030 AP SoC integrated PCIe IP which could be set to PCIe Root Complex mode to communicate with external PCIe Endpoints.

The Mini PCIe WLAN mounted on ONetSwitch30 is shown in Figure 15. The GTX transceiver is configured to be PCIe x1 Gen2.0.

For more detailed information about PL HDL coding, please refer to Xilinx 7 Series FPGAs Integrated Block for PCI Express and LogiCORE IP AXI Bridge for PCI Express related documents on the Xilinx website.

The ONetSwitch30 need to connect GTX transceiver and Mini PCIe Slot with a SATA3.0 cable. Please refer to 2.13 GTX Transceiver.

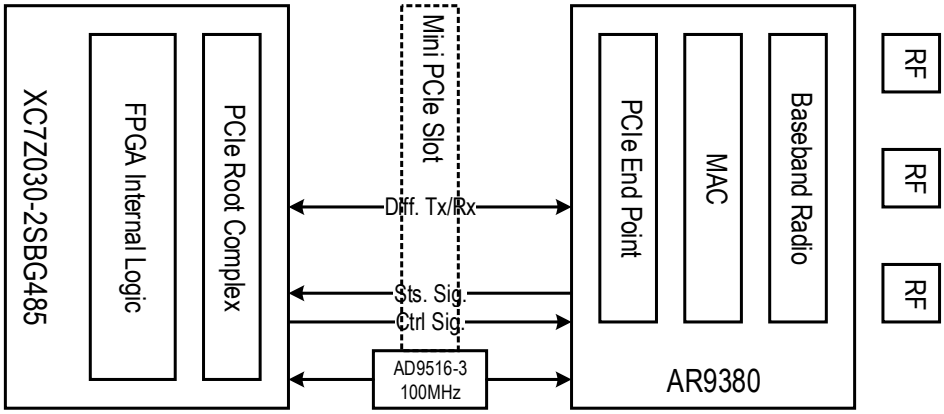

Figure 105 Mini PCIe WLAN Connections

Table 18 Mini PCIe Connections

Bank	Net Name	Zynq Pin	Direction	Description
34	PL_PCIE_WAKE_B	M4	IN	LVCMOS15
34	PL_PCIE_PERST_B	R5	OUT	LVCMOS15
34	MINIPCIE_CLKREQ_B	M3	IN	LVCMOS15
34	MINIPCIE_W_DISABLE_B	R4	OUT	LVCMOS15
	PCIE_TXP		OUT	J14, refer to GTX Transceiver
	PCIE_TXN		OUT	J14, refer to GTX Transceiver
	PCIE_RXP		IN	J14, refer to GTX Transceiver
	PCIE_RXN		IN	J14, refer to GTX Transceiver

2.13 GTX Transceiver

The ONetSwitch30 provides access to 4 6.6Gbps GTX transceivers, wired to the 4 SATA connectors at the edge of board. It could be used to connect the on board Mini PCIe, or board-to-board connectives. The SATA connectors are grouped according to their pinouts, 2 Masters (A group) and 2 Slaves (B group). The connection must be between a Master port and a Slave port.

Please connect the GTXs by SATA 3.0 Cable for reliable communicate.

To enable the Mini PCIe, please connect J14 to one of the B group (Slave) SATA connector.

Table 19 GTX Transceiver connections

Bank	Net Name	Zynq Pin	Direction	Description
112	ZYNQ_GTP0_TX_P	AA3	OUT	MGTX-TXP#0
112	ZYNQ_GTP0_TX_N	AB3	OUT	MGTX-TXN#0
112	ZYNQ_GTP0_RX_P	AA7	IN	MGTX-RXP#0
112	ZYNQ_GTP0_RX_N	AB7	IN	MGTX-RXN#0
112	ZYNQ_GTP1_TX_P	W4	OUT	MGTX-TXP#1
112	ZYNQ_GTP1_TX_N	Y4	OUT	MGTX-TXN#1
112	ZYNQ_GTP1_RX_P	W8	IN	MGTX-RXP#1
112	ZYNQ_GTP1_RX_N	Y8	IN	MGTX-RXN#1
112	ZYNQ_GTP2_TX_P	AA5	OUT	MGTX-TXP#2
112	ZYNQ_GTP2_TX_N	AB5	OUT	MGTX-TXN#2
112	ZYNQ_GTP2_RX_P	AA9	IN	MGTX-RXP#2
112	ZYNQ_GTP2_RX_N	AB9	IN	MGTX-RXN#2
112	ZYNQ_GTP3_TX_P	W2	OUT	MGTX-TXP#3
112	ZYNQ_GTP3_TX_N	Y2	OUT	MGTX-TXN#3
112	ZYNQ_GTP3_RX_P	W6	IN	MGTX-RXP#3
112	ZYNQ_GTP3_RX_N	Y6	IN	MGTX-RXN#3
112	CLK_156M_SI57x_P	U9	IN	MGTX-REFCLK#1P
112	CLK_156M_SI57x_N	V9	IN	MGTX-REFCLK#1N
112	GTX_PCIE_CLK_100M_P	U5	IN	MGTX-REFCLK#1P
112	GTX_PCIE_CLK_100M_N	V5	IN	MGTX-REFCLK#1N

Table 20 GTX connector groups

Group	GTX Name	Connector Reference	Location	Description
A	ZYNQ_GTP0	J6	Upper edge	
B	ZYNQ_GTP1	J7	Lower edge	Connected J14 to enable Mini PCIe
A	ZYNQ_GTP2	J5	Right edge	
B	ZYNQ_GTP3	J8	Left edge	Connected J14 to enable Mini PCIe

2.14 PMOD Connector

The ONetSwitch30 has two Digilent PMOD compatible headers (2x6), J15, J16. These are 2.54mm headers that include eight user I/O plus 3.3V and ground signals. PMOD connectors interface to Bank 13 locate at PL-side of the XC7Z030 AP SoC.

Table 21 PMODE connections, XC7Z030 AP SoC to PMOD connector

Bank	Net Name	Zynq Pin	Direction	Description
13	PL_PMOD_A_0	R17	INOUT	User I/O
13	PL_PMOD_A_1	U19	INOUT	User I/O
13	PL_PMOD_A_2	V19	INOUT	User I/O
13	PL_PMOD_A_3	U18	INOUT	User I/O
13	PL_PMOD_A_4	W18	INOUT	User I/O
13	PL_PMOD_A_5	V18	INOUT	User I/O
13	PL_PMOD_A_6	U17	INOUT	User I/O
13	PL_PMOD_A_7	V16	INOUT	User I/O
13	PL_PMOD_B_0	Y19	INOUT	User I/O
13	PL_PMOD_B_1	U13	INOUT	User I/O
13	PL_PMOD_B_2	U12	INOUT	User I/O
13	PL_PMOD_B_3	W13	INOUT	User I/O
13	PL_PMOD_B_4	W12	INOUT	User I/O
13	PL_PMOD_B_5	U11	INOUT	User I/O
13	PL_PMOD_B_6	V11	INOUT	User I/O
13	PL_PMOD_B_7	W11	INOUT	User I/O

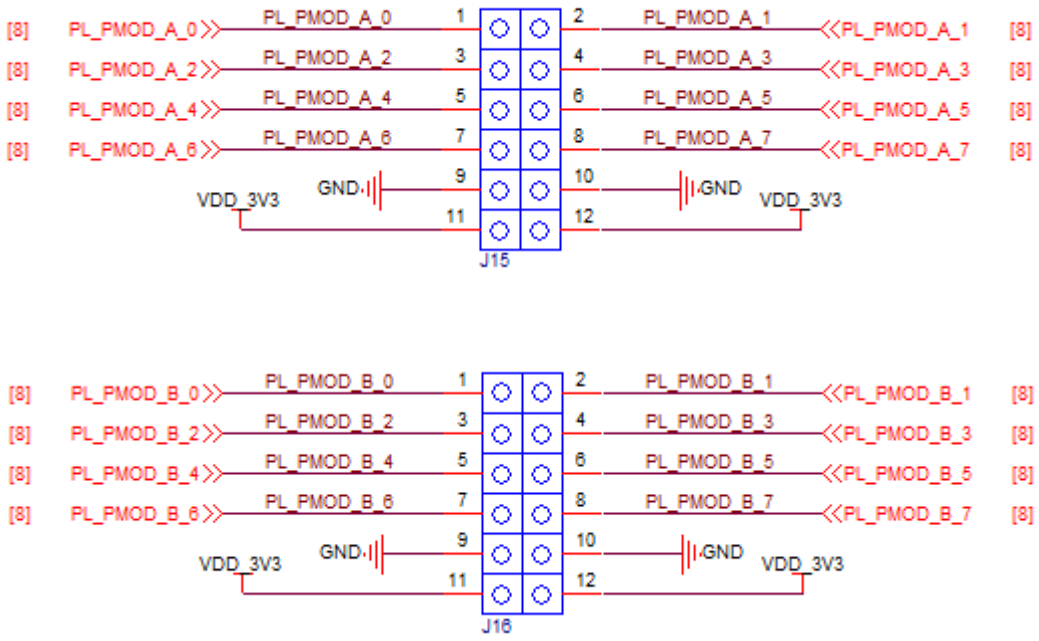

Figure 16 PMOD circuit

2.15 Power Management

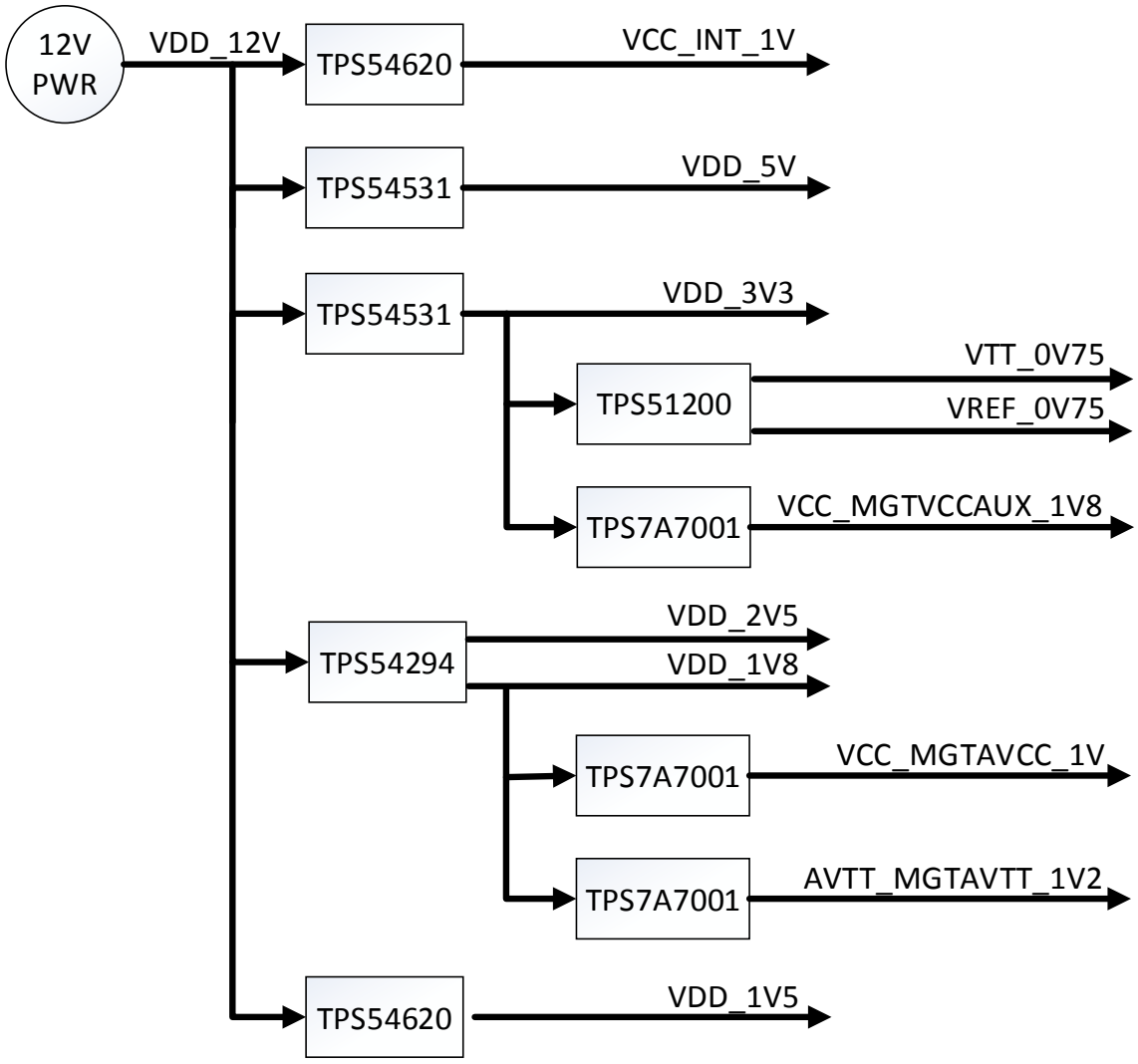

Figure 17 Onboard Power Regulators

2.16 Pushbutton, DIP Switch and LED

Table 22 User Pushbutton Connections to XC7Z030 AP SoC

#	Pushbutton Reference	Type	Zynq Pin	Description
1	SW1	System	V10	PROG_B: AP SoC program
2	SW2	User	D18	Pull low, output '1' when press the button
3	SW3	System	B18	POR_B: board reset
4	SW4	System	C14	SRST_B: PS reset
5	SW5	User	P2	Pull high, output '0' when press the button

Table 23 DIP Switch Connections to XC7Z030 AP SoC

#	Switch Reference: Pin	Type	Zynq Pin	Description
1	SW6:1	User	P6	Custom
2	SW6:2	User	P5	Custom
3	SW6:3	User	N4	Custom
4	SW6:4	User	N3	Custom
5	SW6:5	User	K3	Custom
6	SW6:6	User	N6	Custom

Table 24 LED Connections

#	LED Reference	Type	Zynq Pin	Description
1	DS1	System	T8	INIT_B: AP SoC initiate
2	DS2	System	T10	DONE: FPGA program done
3	DS3	User	G17	Indicate HIGH
4	DS4	System		Resetting
5	DS8	User	B1	Indicate HIGH output
6	DS9	User	C4	Indicate HIGH output
7	DS10	User	R17	Indicate HIGH output
8	DS11	User	U19	Indicate HIGH output
9	DS12	System		Indicate VCC_INT_1V
10	DS13	System		Indicate VDD_1V8
11	DS14	System		Indicate VDD_2V5
12	DS15	System		Indicate VDD_3V3
13	DS16	System		Indicate VDD_1V5

3 Board Setting

3.1 Jumper Settings

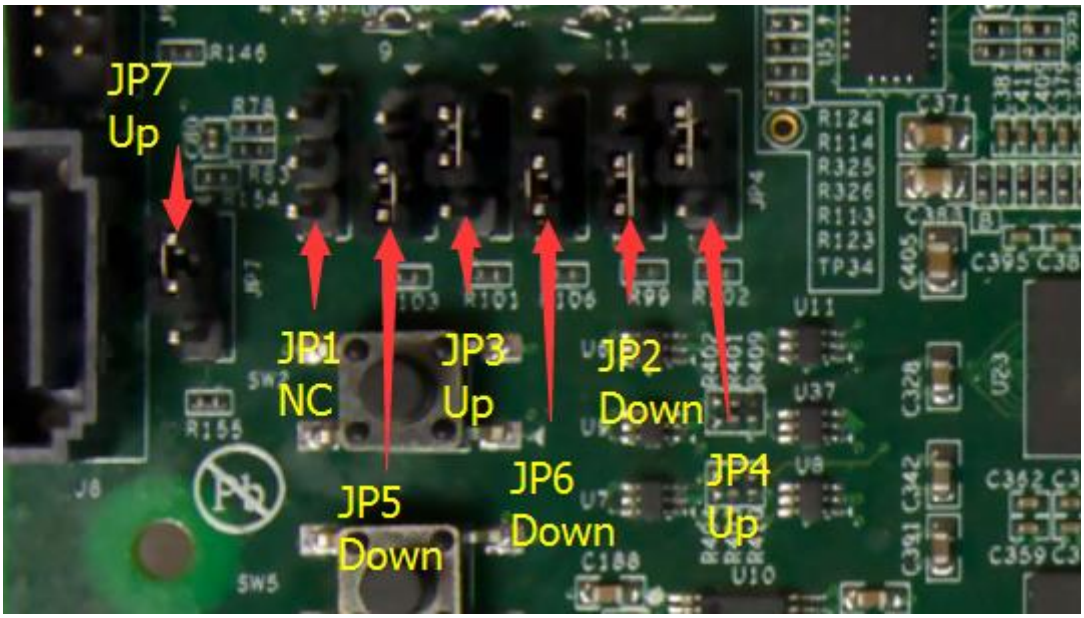

Figure 18 Default Jumper Settings (Boot Mode: TF Card)

Table 25 Jumper Setting

#	Jumper Reference	Connection	Location	Description
1	JP1	X		XADC Setting, No Connect
2	JP2	2-3	Upper	PLL Mode
3	JP3	1-2	Upper	Boot Mode, Toggle TF Card
4	JP4	1-2	Upper	Boot Mode, Toggle TF Card
5	JP5	2-3	Lower	Boot Mode, Toggle TF Card
6	JP6	2-3	Lower	JTAG mode
7	JP7	1-2	Upper	Toggle USB JTAG

4 Additional Resources

- ✓ MeshSr ONetSwitch30 http://www.meshsr.com/product/ONetSwitch30
- ✓ Xilinx Zynq AP SoC http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm
  Xilinx FMC Std. http://www.xilinx.com/products/boards_kits/fmc.htm
- ✓ Xilinx LogiCORE IP Using Xilinx DocNav for Vivado 2013.4
  - PG138 LogiCORE IP AXI Ethernet v6.0
  - PG051 LogiCORE IP Tri-Mode Ethernet MAC v8.1
  - PG059 LogiCORE IP AXI Interconnect v2.1
  - PG164 LogiCORE IP Processor System Reset Module v5.0
  - PG082 LogiCORE IP Processing System 7 v5.3
  - PG068 LogiCORE IP 10-Gigabit Ethernet PCS/PMA v4.1
  - PG072 LogiCORE IP 10-Gigabit Ethernet MAC v13.0
  - PG054 7 Series FPGAs Integrated Block for PCI Express v3.0
  - PG021 LogiCORE IP AXI Bridge for PCI Express v2.3
  - PG132 LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers v3.0
  - UG586 Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions v2.0
- ✓ ARM AMBA
  - AXI4-Lite IHI0022E AMBA® AXI™ and ACE™ Protocol Specification
  - AXI4-Stream IHI0051A AMBA® 4 AXI4-Stream Protocol

5 Revision History

Date	Version	Description
2015-1-20	1.00	Initial MeshSr release