ONetSwitch45 Hardware User Guide

1 Overview

ONetSwitch45 is an All Programmable Open Network Innovation Platform.

ONetSwitch45 is based on the Xilinx XC7Z045 Zynq SoC, adopts the Gigabit ports and the 10G ports, and can extend wireless or storage. Both its software and hardware can realize custom programming. Its reference designs are abundant and flexible, can be used to various researches on the evolution of network prototypes, and the development of customized network products. Especially, the features of the miniaturization and low power are adapted to the multi-node network tests and deployments.

1.1 Key Features

Table 1 ONetSwitch45 Key Features

General	
Core Silicon	XC7Z045-2FFG676
Power Supply	DC 12V
Programming Source	QSPI Flash / SD Card
Processing System	
Processor	Dual ARM Cortex-A9@800MHz
Cache	L1: 32KB Instruction + 32KB Data per processor; L2: 512KB; OCM: 256KB
DRAM	DDR3 1GBytes
Flash	Quad SPI Flash 256Mb
DMA	8 channel (4 for Programmable Logic)
Ethernet Port	1x 1000BASE-T
Peripheral	USB / USB-UART / USB JTAG / SD Card
Programmable Logic	
Programmable Logic Equivalent	350K Logic Cells, Logic Cells, Kintex-7 FPGA, Approximate ASIC Gates 5.2M
PS to PL Interconnect	AMBA AXI4 interconnect, maximum 100Gbps
SRAM	QDRII+ 72Mb, 57.6Gbps@400MHz
Ethernet Port	4x GE RJ45 10/100/1000M Ethernet , 4x 10GE SFP+
Wireless Access	Mini PCIe Slot
Peripheral	FMC HPC connector, include 3x 10Gbps GTX
User I/O	User LEDs/Pushbuttons/DIP Switch

1.2 Board Block Diagram

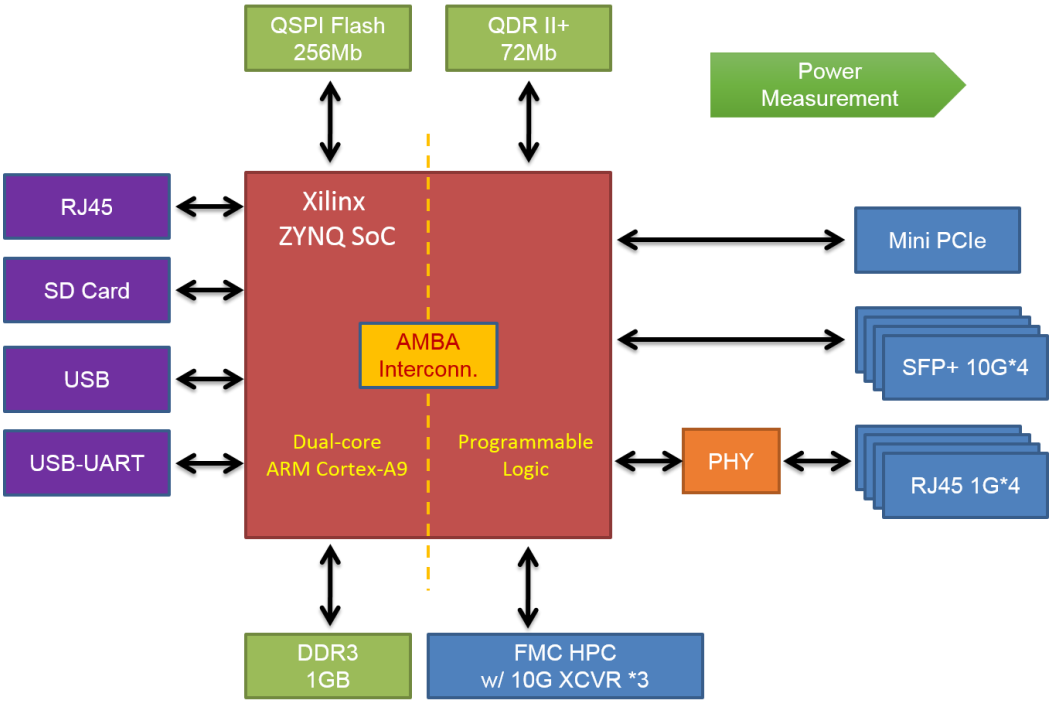

Figure 1 ONetSwitch45 Board Block Diagram

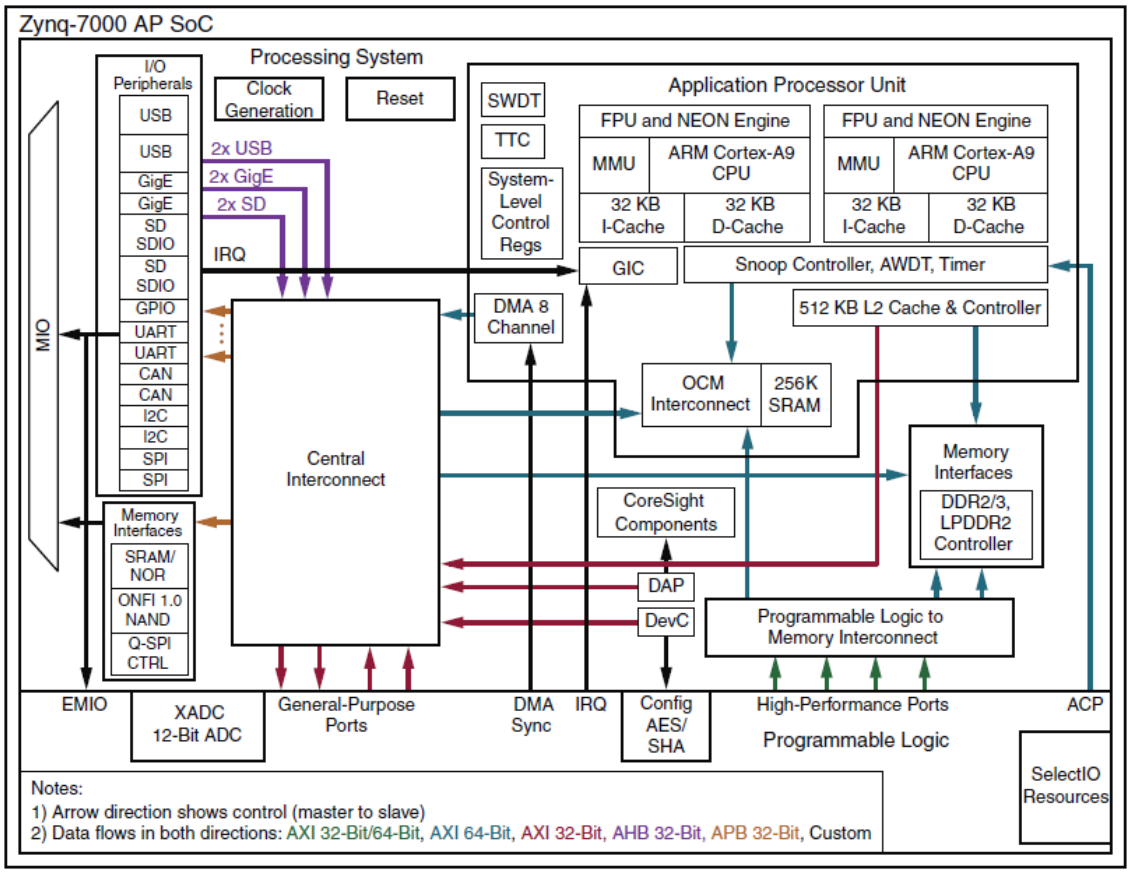

Figure 2 Xilinx Zynq-7000 Block Diagram

1.3 Components Overview

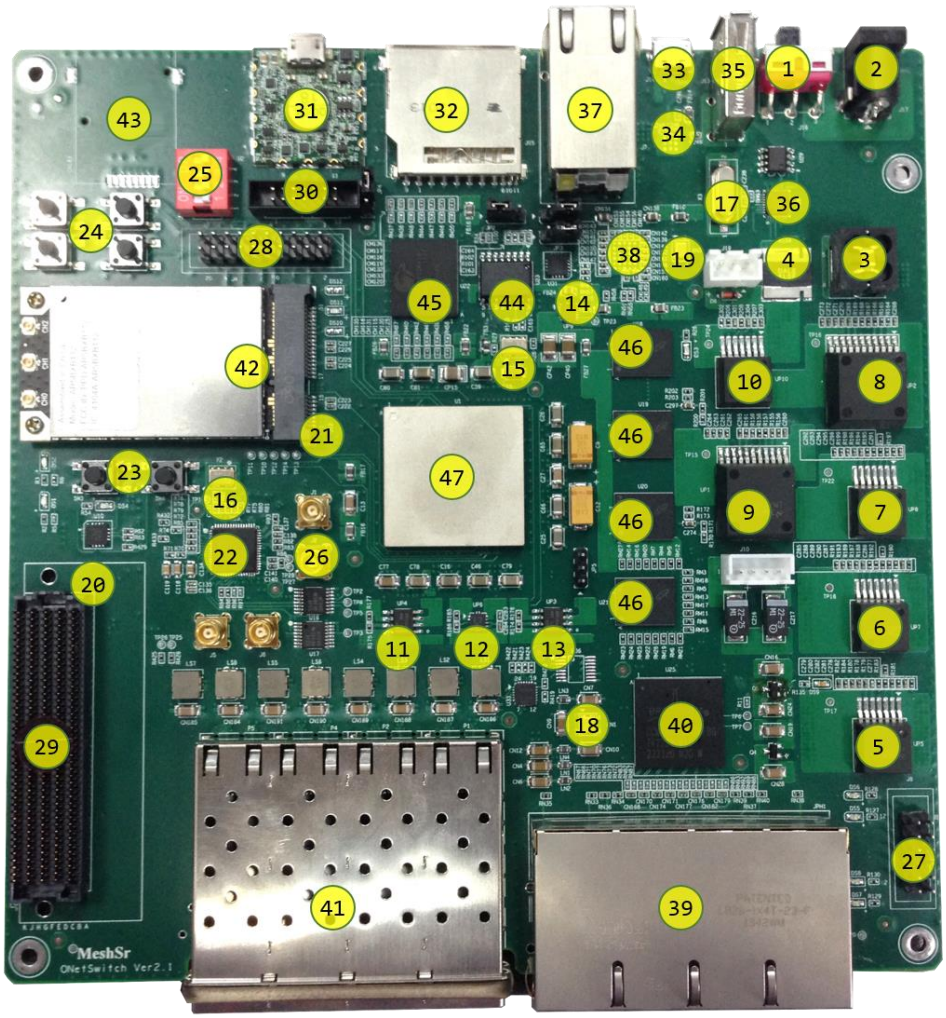

Figure 3 ONetSwitch45 Board Compent Locations

Table 1 ONetSwitch45 Components Descriptions

Callout	Component Description	Reference Designator	Notes
1	Power On/Off Switch	J18	SIP_PWR_SW_3P
2	12V Power input connector	J17	2.5mm 12V DC10B
3	Power filter	X6	BNX016
4	Power Metal Strip Resistors	R154	WSL36375L000FEB 0.005Ω
5	DC-DC Converter 3.3V	UP5	LMZ22005TZ
6	DC-DC Converter 2.5V	UP7	LMZ22005TZ
7	DC-DC Converter 1.5V	UP8	LMZ22005TZ
8	DC-DC Converter 1.8V	UP3	LMZ12008TZ
9	DC-DC Converter 1.0V	UP1	LMZ12008TZ
10	DC-DC Converter 5V	UP10	LMZ12002TZ

11	LDO 1.2V for GTX	UP4	TPS7A7001DDA
12	LDO 1.8V for GTX	UP6	TPS7A8001DRBT
13	LDO 1.0V for GTX	UP3	TPS7A7001DDA
14	DDR Termination 0.75V	UP9	TPS51200DRCT
15	Oscillator 33MHz	X1	33.33MHz PS work clock
16	Oscillator 25MHz	X2	25MHz, AD9516-3 reference clock
17	Oscillator 24MHz	X3	24MHz, USB 3320 reference clock
18	Oscillator PL PHY	XN1	25MHz, BCM5464SR PHY reference clock
19	Oscillator PS PHY	XN3	25MHz, 88E1116R PHY reference clock
20	Oscillator SFP+	U34(Bottom)	156.25MHz, SFP+ 10G reference clock
21	Oscillator SMA	U35(Bottom)	156.25MHz, SMA reserve clock
22	Clock Generator	U15	AD9156-3
23	Reset Key	SW3,4	Push Button x2 (POR_B/SRST_B)
24	User Key	SW1,2,5,6	Push Button x4
25	DIP Switch	SW9	DIP4
26	SMA Connector	J1,2,5,6	J1-J2 U35 output clock, J5-J6 U15 input clock
27	PMOD Connector	J8	12 pin
28	PJTAG Connector	J4	20 pin
29	FMC HPC	J21	ASP-134486-01
30	JTAG-14pin	J3	14 pin
31	USB JTAG	U2	Digilent USB JTAG SMT2
32	SD Card Connector	J15	2041021-3
33	USB UART	J14	47589-0001 USB Micro B port
34	USB-to-UART Bridge	U30(Bottom)	CP2103
35	USB Connector	J13	48204-0001 USB A port
36	USB Transceiver	U28	USB3320
37	PS RJ45 1G*1	J7	0826-1X1T-23-F MegJack 10/100/1000 LAN
38	PS PHY	U27(Bottom)	88E1116R PHY
39	PL RJ45 1G*4	JPH1	0826-1X4T-23-F MegJack 10/100/1000 LAN
40	PL PHY	U25	BCM5464 PHY
41	SFP+ 10G*4	P1,2,4,5	74441-0010 10G SFP+
42	Mini PCIe Slot	J12	Atheros AR9380 AR5BXB112
43	SIM Slot	CN183	SIM card reserved for Mini PCIe Slot
44	SPI Flash	U23,24	QSPI Flash N25Q128A11ESF40 x2
45	SRAM	U22	QDRII+ CY7C25652KV18
46	DRAM	U18,19,20,21	DDR3 MT41J256M8HX-15E x4
47	Zynq	U1	XC7Z045-2FFG676

1.4 Bank Description

Table 3 Zynq Bank Assignments

Bank	I/O Power supply	Feature
500(MIO 0)	1.8V	QSPI, SD
501(MIO 1)	1.8V	USB-UART, PS RJ45, USB, SD, GPIO(AD9516-3 programming)
502(DDR)	1.5V	DDR3
12(High Range)	2.5V	RGMII(RJ45 1G*4)
13(High Range)	3.3V	PJTAG, I2C, LED, PMOD, FMC, SFP+ Control and Status, PCIe Control and Status
33(High Perf.)	1.5V	QDR, FMC
34(High Perf.)	1.5V	QDR
35(High Perf.)	1.5V	QDR, Push button, DIP switch
111(GTX)		SFP+
112(GTX)		PCIe, FMC

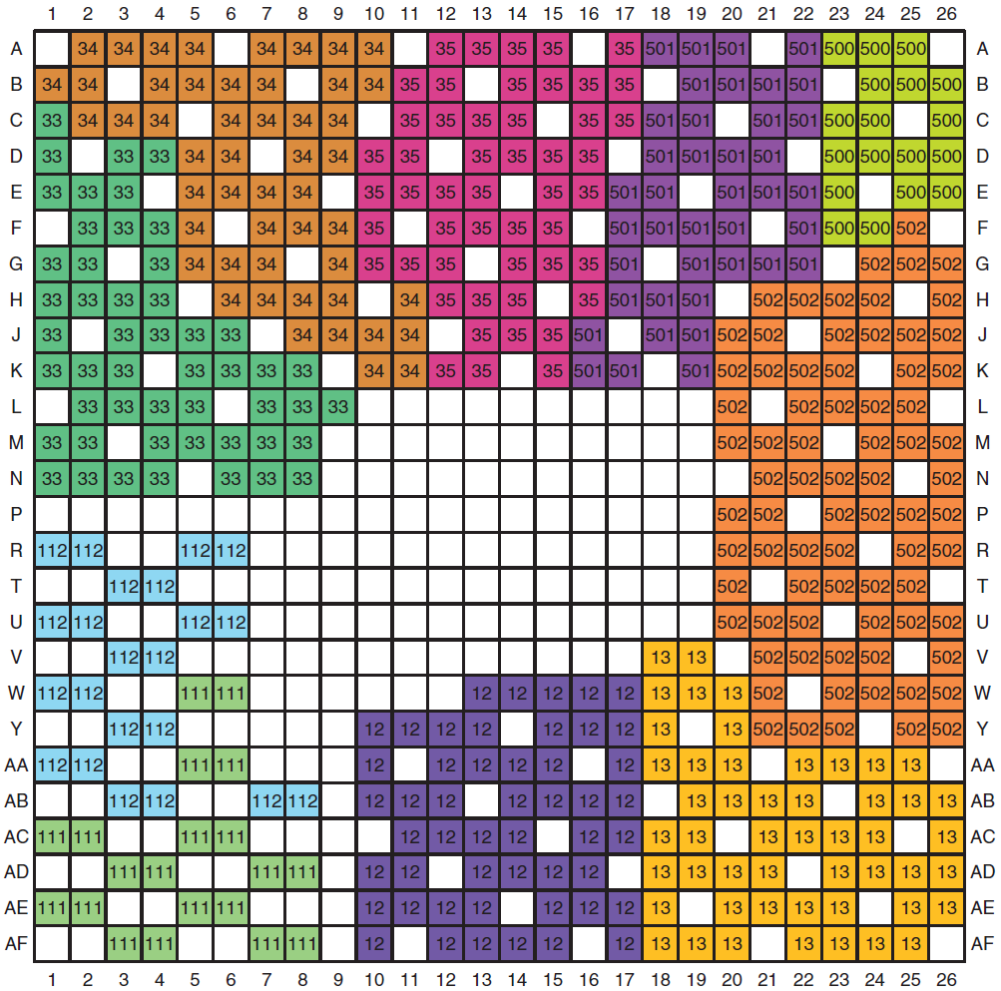

Figure 4 Xilinx Zynq SoC Package (XC7Z045-2FFG676)

Feature Descriptions

2.1 Xilinx Zynq SoC

The ONetSwitch45 is populated with the Xilinx ZynqTM-7000 XC7Z045-2FFG676 AP SoC.

The XC7Z045 AP SoC consists of an integrated processing system (PS) a programmable logic (PL), on a single die.

Information for the Xilinx Zynq AP SoC specification can be found at the documents released by Xilinx.

2.1.1 Device Configuration

The ONetSwitch45 supports two configuration options:

- ✓ QSPI flash memory, PS Configuration, Master Mode Boot;
- ✓ SD Card, PS Configuration, Master Mode Boot.

The JP1 and JP3 maintain '0'(connect pin2 and pin3) by default. The JP2 will be set depending on the desire boot mode, QSPI Flash or SD Card.

Table 2 Configuration Option Settings

管脚	**MIO[8]**	**MIO[7]**	**MIO[6]**	**MIO[5]**	**MIO[4]**	**MIO[3]**	**MIO[2]**
模式	**vmode[1]**	**vmode[0]**	**boot_mode[4]**	**boot_mode[0]**	**boot_mode[2]**	**boot_mode[1]**	**boot_mode[3]**
QSPI				VDD	0 (JP2 2-3)	GND	
SD					**1 (JP2 1-2)**		
Mode for all 3 PLLs							
PLL Enable			**0 (JP3 2-3)**				
PLL Bypassed			1 (JP3 1-2)				
MIO Bank Voltage							
1.8V	VDD	VDD					
JTAG Chain Routing							
Cascade Mode							**0 (JP1 2-3)**
Independent Mode							1 (JP1 1-2)

2.1.2 Debugging

The ONetSwitch45 provides 3 options for debugging. The USB JTAG and the JTAG-14pin are selected by JP7 for PL debug. The PJTAG is used for ARM debug

- ✓ USB JTAG, PL JTAG;
- ✓ JTAG-14pin, PL JTAG;
- ✓ PJTAG-20pin, EMIO PJTAG.

✓ Table 3 Debugging options and settings

Debugging Option	**Jumper**	**Description**
USB JTAG	**JP4 1-2**	Micro USB port
JTAG-14pin	JP4 2-3	Xilinx Platform Cable
PJTAG-20pin	-	ARM Debug

2.2 Clock Source

The ONetSwitch45 has eight Clock sources.

Table 4 Clock Sources

#	Device	Reference	Description
1	时钟 33MHz	X1	33.33MHz PS work clock
2	时钟 25MHz	X2	25MHz, AD9516-3 reference clock
3	时钟 24MHz	X3	24MHz, USB 3320 reference clock
4	时钟 PL PHY	XN1	25MHz, BCM5464SR PHY reference clock
5	时钟 PS PHY	XN3	25MHz, 88E1116R PHY reference clock
6	时钟 SFP+	U34(Bottom)	156.25MHz, SFP+ 10G reference clock
7	时钟 SMA	U35(Bottom)	156.25MHz, SMA reserve clock
8	多路时钟	U15	AD9156-3

Table 5 Clock connections

#	Clock Generator:Pin	Net Name	Destiny Device:Pin	Description
1	X1.3	PS_CLK_33M	U1I.B24	33.33MHz PS work clock
2	X2.3	AD9516_25MCLK	U15.REFIN	25MHz AD9516-3 reference clock
3	X3.1	REFCLK_26	U28.26	24MHz, USB 3320 reference clock
	X3.2	XO_25	U28.25	
4	XN1.1	XTALI	U25C.H3	25MHz, BCM5464SR PHY reference clock
	XN1.3	XTALO	U25C.H4	
5	XN3.1	PS_XTAL_IN	U27.38	25MHz, 88E1116R PHY reference clock
	XN3.3	PS_XTAL_OUT	U27.39	
6	U34.4	CLK_156M_SI57x_P	U1G.AA6	156.25MHz, SFP+ 10G reference clock
	U34.5	CLK_156M_SI57x_N	U1G.AA5	
7	U35.4	GTX_SMA_CLK_125M_N	U1G.W5/J2	156.25MHz, SMA reserve clock
	U35.5	GTX_SMA_CLK_125M_P	U1G.W6/J1	
8	U15.56	PL_SGMII_REFCLK_125M_P	U1C.AD20	OUT0: Zynq AP SoC SGMII Reference Clock
	U15.55	PL_SGMII_REFCLK_125M_N	U1C.AD21	
	U15.43	QDR2P_SYS_CLK_200M_P	U1D.M6	OUT2: Zynq AP SoC QDR Reference Clock
	U15.42	QDR2P_SYS_CLK_200M_N	U1D.M5	
	U15.25	9516_SMA_CLK_125M_P	J5	OUT4: SMA reserve clock
	U15.26	9516_SMA_CLK_125M_N	J6	
	U15.28	9516_FMC_CLK_125M_P	J21G.G30	OUT5: FMC reserve clock
	U15.29	9516_FMC_CLK_125M_N	J21G.G31	
	U15.48	PCIE_REFCLK_100M_P	J12.13	OUT6: Mini PCIe Slot Reference Clock
	U15.47	PCIE_REFCLK_100M_N	J12.11	
	U15.46	GTX_PCIE_CLK_100M_P	U1H.R6	OUT7: PCIe GTX Reference Clock
	U15.45	GTX_PCIE_CLK_100M_N	U1H.R5	
	U15.35	GTX_SATA_CLK_150M_P	TP27	OUT9: Test Clock
	U15.36	GTX_SATA_CLK_150M_N	TP28	

2.2.1 PS work clock

The Processing System (PS) clock source is a 1.8V LVCMOS single-ended fixed 33.333MHz oscillator at X1.

- ✓ Part number: SIT8103AC-23-18E-33.33
- ✓ Frequency: 33.33MHz
- ✓ Stability: 50ppm
- ✓ Output Standard: 1.8V LVCMOS

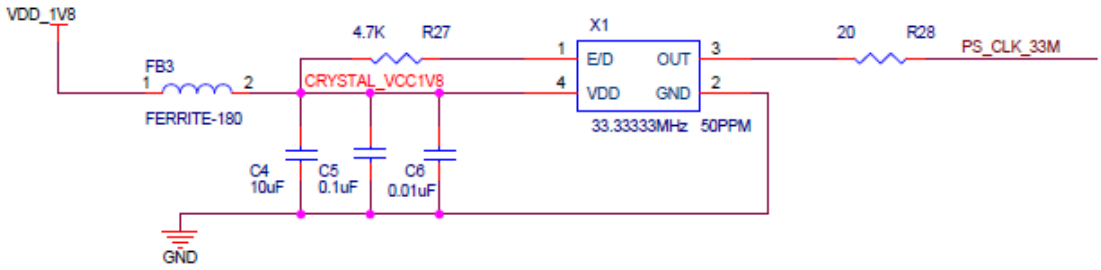

Figure 5 X1 Oscillator circuit

2.2.2 AD9516-3 reference clock

The X2 oscillator is used as reference clock of AD9516-3 U15.

- ✓ Part number: ASFL1-25.000MHZ-EK-T
- ✓ Frequency: 25MHz
- ✓ Stability: 30ppm
- ✓ Output Standard: 3.3V LVCMOS

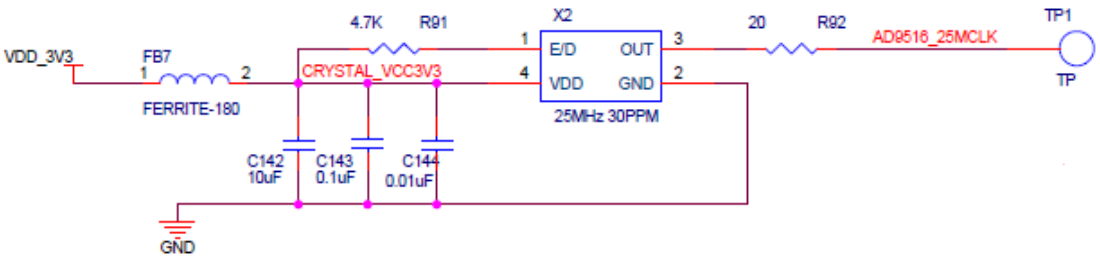

Figure 5 X2 Oscillator circuit

2.2.3 USB 3320 Reference Clock

The X3 oscillator is the reference clock of USB 3320.

- ✓ Part number: HCM49-24.000MABJ-UT
- ✓ Frequency: 24MHz
- ✓ Stability: 50ppm
- ✓ Output Standard: Depend on host chip

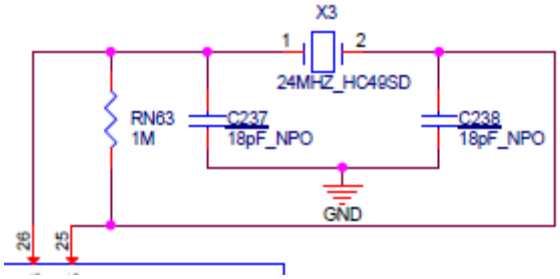

Figure 6 X3 Crystal circuit

2.2.4 PL PHY Reference Clock

The XN1 oscillator is the reference clock of BCM5464SR.

- ✓ Part number: ABM8-25.000MHZ-B2-T
- ✓ Frequency: 25MHz
- ✓ Stability: 50ppm

Output Standard: Depend on host chip

2.2.5 PS PHY Reference Clock

The XN3 oscillator is the reference clock of 88E1116R PHY.

- ✓ Part number: ABM8-25.000MHZ-B2-T
- ✓ Frequency: 25MHz
- ✓ Stability: 50ppm
- ✓ Output Standard: Depend on host chip

2.2.6 SFP+ Reference Clock

The U34 oscillator is the reference clock of 10G BASE LAN, connected to GTX transceiver.

- ✓ Part number: KC7050P156.250L30E00
- ✓ Frequency: 156.25MHz
- ✓ Stability: 50ppm
- ✓ Output Standard: LVDS

2.2.7 SMA Reserve Clock

The U35 oscillator is the reserve clock of GTX. This clock could be supplied by SMA connector either.

- ✓ Part number: BF-156.250MBE-T
- ✓ Frequency: 156.25MHz
- ✓ Stability: 50ppm
- ✓ Output Standard: LVDS

2.2.8 AD9516-3 multi-output clock Generator

The most important clock generator of ONetSwitch45 is AD9516-3 (U15). Its reference clock is 25MHz single-end clock from oscillator X2. The AD9516-3 generates several low jitter differential clock to clocking XC7Z045 AP SoC, such as SGMII 125MHz, QDRII+ 200MHz, PCIe 100MHz, etc. It also provides the reference clock for mini PCIe Slot (100MHz), SMA clock and FMC clock.

The AD9516-3 should be programmed through serial control port which interfaces to the Processing System. For more detailed information, please refer to AD9516-3 DATASHEET.

Table 6 AD9516-3 Serial Control Port Connections, to XC7Z045 AP SoC

Bank	Net Name	Zynq Pin	Direction	Description
501	MIO_46_AD9516_SDI	E17	INOUT	GPIO
501	MIO_47_AD9516_SDO	B19	INOUT	GPIO
501	MIO_48_AD9516_SCLK	B21	INOUT	GPIO
501	MIO_49_AD9516_CS_N	A18	INOUT	GPIO

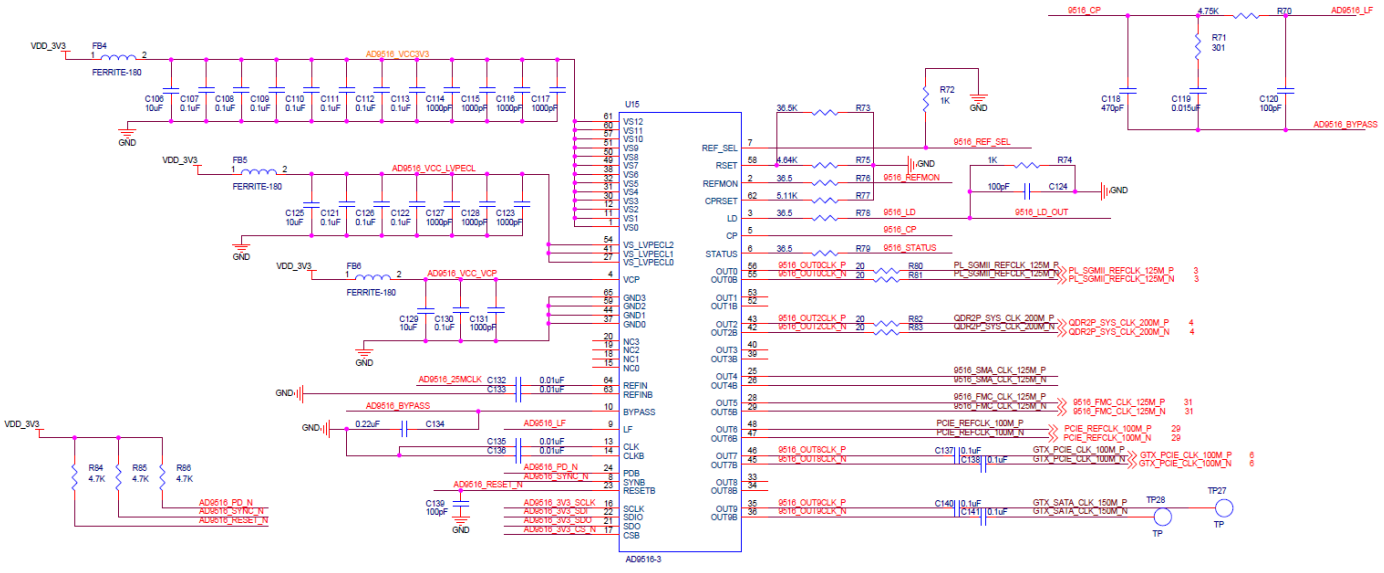

Figure 8 AD9156-3 circuit

2.3 QSPI Flash

The Quad-SPI flash memory located at U23 and U24 provides 2 x 128 Mb of nonvolatile storage that can be used for configuration and data storage.

- ✓ Part number: N25Q128A11ESF40
- ✓ Operating voltage: 3.3V
- ✓ Datapath with: 4bits
- ✓ Data rate: Various depending on x1,x2,and x4 mode

Table 7 QSPI Flash Pin Assignment

Bank	Net Name	Zynq Pin	Direction	Description
500	MIO_0_QSPI_1_CS_B	E26	OUT	
500	MIO_1_QSPI_0_CS_B	D26	OUT	
500	MIO_2_QSPI_0_IO0	E25	INOUT	
500	MIO_3_QSPI_0_IO1	D25	INOUT	
500	MIO_4_QSPI_0_IO2	F24	INOUT	
500	MIO_5_QSPI_0_IO3	C26	INOUT	
500	MIO_6_QSPI_0_CLK	F23	OUT	
500	MIO_8_QSPI_FB_CLK	A24	OUT	
500	MIO_9_QSPI_1_CLK	D24	OUT	
500	MIO_10_QSPI_1_IO0	A25	INOUT	
500	MIO_11_QSPI_1_IO1	B26	INOUT	
500	MIO_12_QSPI_1_IO2	A23	INOUT	
500	MIO_13_QSPI_1_IO3	B25	INOUT	

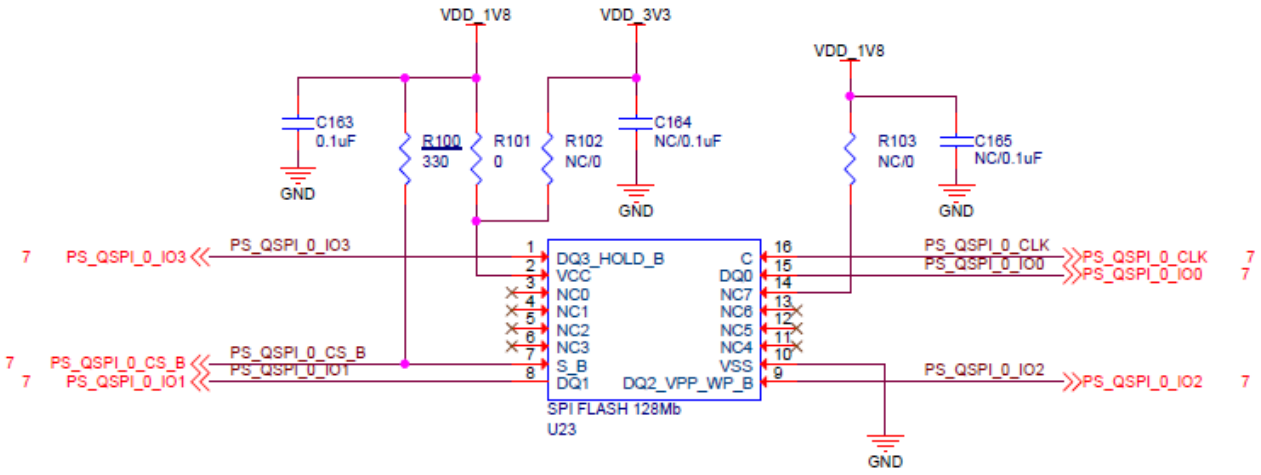

Figure 9 QSPI circuit

2.4 DDR3

The 1 GB,32-bit wide DDR3 component memory system is comprised of four 512Mb x8 DDR3 SDRAMs (MT41J256M8HX-15E).This memory system is connected to the XC7Z045 AP SoC Processing System (PS) memory interface bank 502. The connections between the DDR3 component memory and XC7Z045 AP SoC bank 502 are listed in Table 10.

Table 8 DDR3 Memory Connections

Bank	Net Name	Zynq Pin	Direction	Description
502	DDR3_DQ_0	H23	INOUT	I/O Data
502	DDR3_DQ_1	J26	INOUT	I/O Data
502	DDR3_DQ_2	J23	INOUT	I/O Data
502	DDR3_DQ_3	F25	INOUT	I/O Data
502	DDR3_DQ_4	J24	INOUT	I/O Data
502	DDR3_DQ_5	H26	INOUT	I/O Data
502	DDR3_DQ_6	G26	INOUT	I/O Data
502	DDR3_DQ_7	J25	INOUT	I/O Data
502	DDR3_DQ_8	L23	INOUT	I/O Data
502	DDR3_DQ_9	K23	INOUT	I/O Data
502	DDR3_DQ_10	K26	INOUT	I/O Data
502	DDR3_DQ_11	M25	INOUT	I/O Data
502	DDR3_DQ_12	N24	INOUT	I/O Data
502	DDR3_DQ_13	M26	INOUT	I/O Data
502	DDR3_DQ_14	N23	INOUT	I/O Data
502	DDR3_DQ_15	M24	INOUT	I/O Data
502	DDR3_DQ_16	R26	INOUT	I/O Data
502	DDR3_DQ_17	P24	INOUT	I/O Data
502	DDR3_DQ_18	N26	INOUT	I/O Data
502	DDR3_DQ_19	P23	INOUT	I/O Data
502	DDR3_DQ_20	T24	INOUT	I/O Data
502	DDR3_DQ_21	T25	INOUT	I/O Data
502	DDR3_DQ_22	T23	INOUT	I/O Data
502	DDR3_DQ_23	R23	INOUT	I/O Data
502	DDR3_DQ_24	U26	INOUT	I/O Data
502	DDR3_DQ_25	U24	INOUT	I/O Data
502	DDR3_DQ_26	U25	INOUT	I/O Data
502	DDR3_DQ_27	V24	INOUT	I/O Data
502	DDR3_DQ_28	W26	INOUT	I/O Data
502	DDR3_DQ_29	Y25	INOUT	I/O Data
502	DDR3_DQ_30	Y26	INOUT	I/O Data
502	DDR3_DQ_31	W23	INOUT	I/O Data
502	DDR3_A_0	K22	OUT	Address
502	DDR3_A_1	K20	OUT	Address
502	DDR3_A_2	N21	OUT	Address
502	DDR3_A_3	L22	OUT	Address

502	DDR3_A_4	M20	OUT	Address
502	DDR3_A_5	N22	OUT	Address
502	DDR3_A_6	L20	OUT	Address
502	DDR3_A_7	J21	OUT	Address
502	DDR3_A_8	T20	OUT	Address
502	DDR3_A_9	U20	OUT	Address
502	DDR3_A_10	M22	OUT	Address
502	DDR3_A_11	H21	OUT	Address
502	DDR3_A_12	P20	OUT	Address
502	DDR3_A_13	J20	OUT	Address
502	DDR3_A_14	R20	OUT	Address
502	DDR3_BA_0	U22	OUT	Bank Address
502	DDR3_BA_1	T22	OUT	Bank Address
502	DDR3_BA_2	R22	OUT	Bank Address
502	DDR3_DQS_0_P	H24	INOUT	I/O Differential data strobe
502	DDR3_DQS_0_N	G25	INOUT	I/O Differential data strobe
502	DDR3_DQS_1_P	L24	INOUT	I/O Differential data strobe
502	DDR3_DQS_1_N	L25	INOUT	I/O Differential data strobe
502	DDR3_DQS_2_P	P25	INOUT	I/O Differential data strobe
502	DDR3_DQS_2_N	R25	INOUT	I/O Differential data strobe
502	DDR3_DQS_3_P	W24	INOUT	I/O Differential data strobe
502	DDR3_DQS_3_N	W25	INOUT	I/O Differential data strobe
502	DDR3_DM_0	G24	OUT	Data mask
502	DDR3_DM_1	K25	OUT	Data mask
502	DDR3_DM_2	P26	OUT	Data mask
502	DDR3_DM_3	V26	OUT	Data mask
502	DDR3_RESET_B	H22	OUT	Reset
502	DDR3_CLK_P	R21	OUT	Differential clock output
502	DDR3_CLK_N	P21	OUT	Differential clock output
502	DDR3_CKE	U21	OUT	Clock enable
502	DDR3_CS_B	Y21	OUT	Chip select
502	DDR3_WE_B	V22	OUT	Write enable
502	DDR3_CAS_B	Y23	OUT	RAS column address select
502	DDR3_RAS_B	V23	OUT	RAS row address select
502	DDR3_ODT	Y22	OUT	Output dynamic termination
502	DDR3_VRP	W21	OUT	I/O Used to calibrate input termination
502	DDR3_VRN	V21	OUT	I/O Used to calibrate input termination
502	DDR3_VREF0	K21		I/O Reference voltage
502	DDR3_VREF1	M21		I/O Reference voltage

2.5 PS Ethernet

The ONetSwitch45 uses the Marvell Alaska PHY device 88E1116R for Ethernet communications at 10/100/1000 Mb/s. The PHY connects to MIO Bank 501 and interfaces to the Processing System (PS) via RGMII. The connections from the XC7Z045 AP SoC to 88E1116R are listed in Table 11.

Table 9 PS Ethernet Connections, XC7Z045 AP SoC to PHY

Bank	Net Name	Zynq Pin	Direction	Description
500	MIO_7_PHY_RST	E23	OUT	Reset
501	MIO_16_PHY_RGMII_TX_CLK	G21	OUT	TX
501	MIO_17_PHY_RGMII_TXD_0	G17	OUT	
501	MIO_18_PHY_RGMII_TXD_1	G20	OUT	
501	MIO_19_PHY_RGMII_TXD_2	G19	OUT	
501	MIO_20_PHY_RGMII_TXD_3	H19	OUT	
501	MIO_21_PHY_RGMII_TX_CTRL	F22	OUT	
501	MIO_22_PHY_RGMII_RX_CLK	G22	IN	RX
501	MIO_23_PHY_RGMII_RXD_0	F20	IN	
501	MIO_24_PHY_RGMII_RXD_1	J19	IN	
501	MIO_25_PHY_RGMII_RXD_2	F19	IN	
501	MIO_26_PHY_RGMII_RXD_3	H17	IN	
501	MIO_27_PHY_RGMII_RX_CTRL	F18	IN	
501	MIO_52_PHY_MDC	A20	OUT	MDIO
501	MIO_53_PHY_MDIO	A19	INOUT	

2.6 SD Card

The ONetSwitch45 includes a secure digital input/output (SDIO) interface to provide user-logic access to general purpose nonvolatile SDIO memory cards. The SDIO signals are connected to XC7Z045 AP SoC PS bank 501 which has its VCCMIO set to 1.8V. A MAX13035E high-speed logic-level translator is used between XC7Z045 AP SoC 1.8V PS bank 501 and the 3.3V SD card connector.

Table 12 lists the SD card interface connections to the XC7Z045AP SoC.

Table 10 SDIO Connections to the XC7Z03 AP SoC

Bank	Net Name	Zynq Pin	Direction	Description
500	MIO_14_SD_DETECT	D23	IN	DETECT
500	MIO_15_SD_PROTECT	C24	IN	PROTECT
501	MIO_40_SD_CLK	C22	OUT	CLK
501	MIO_41_SD_CMD	C19	INOUT	CMD
501	MIO_42_SD_DAT_0	F17	INOUT	DAT0
501	MIO_43_SD_DAT_1	D18	INOUT	DAT1
501	MIO_44_SD_DAT_2	E18	INOUT	DAT2
501	MIO_45_SD_CD_DAT_3	C18	INOUT	CD_DAT3

2.7 USB

The ONetSwitch45 uses a Standard Microsystems Corporation USB3320 USB 2.0 ULPI Transceiver to support a USB connection to the host computer. The USB peripheral is used on the PS, connected in MIO Bank 501.

The connections between the USB Transceiver and the XC7Z045 AP SoC are listed in Table 13.

Table 11 USB Transceiver Connections to the XC7Z045 AP SoC

Bank	Net Name	Zynq Pin	Direction	Description
501	MIO_32_USB_DATA_0	K17	INOUT	USB Data lines
501	MIO_33_USB_DATA_1	E22	INOUT	
501	MIO_34_USB_DATA_2	J16	INOUT	
501	MIO_35_USB_DATA_3	D19	INOUT	
501	MIO_28_USB_DATA_4	J18	INOUT	
501	MIO_37_USB_DATA_5	D20	INOUT	
501	MIO_38_USB_DATA_6	D21	INOUT	
501	MIO_39_USB_DATA_7	C21	INOUT	
501	MIO_29_USB_DIR	E20	IN	ULPI DIR signal
501	MIO_30_USB_STP	K19	OUT	ULPI STR signal
501	MIO_31_USB_NXT	E21	IN	ULPI NXT signal
501	MIO_36_USB_CLKOUT	K16	IN	USB Clock

2.8 USB-UART

The ONetSwitch45 contains a Silicon Labs CP2103GM USB-to-UART bridge device which allows a connection to a host computer with a USB port. The CP2103GM TX and RX pins are wired to the UART_1 IP block within the XC70Z45 AP SoC PS I/O Peripherals set.

Table 14 lists the USB connections between the XC7Z045 AP SoC PS Bank 501 and the CP2103 UART bridge.

Table 12 XC7Z045 AP SoC to CP2103 Connections

Bank	Net Name	Zynq Pin	Direction	Description
501	MIO_50_USB_UART_RX	B22	IN	Data in
501	MIO_51_USB_UART_TX	B20	OUT	Data out

2.9 JTAG

The PL JTAG chain can be programmed by two different methods, controlled by jumper JP4.
When an FPGA mezzanine card (FMC) is attached to HPC it is automatically added to the JTAG chain.

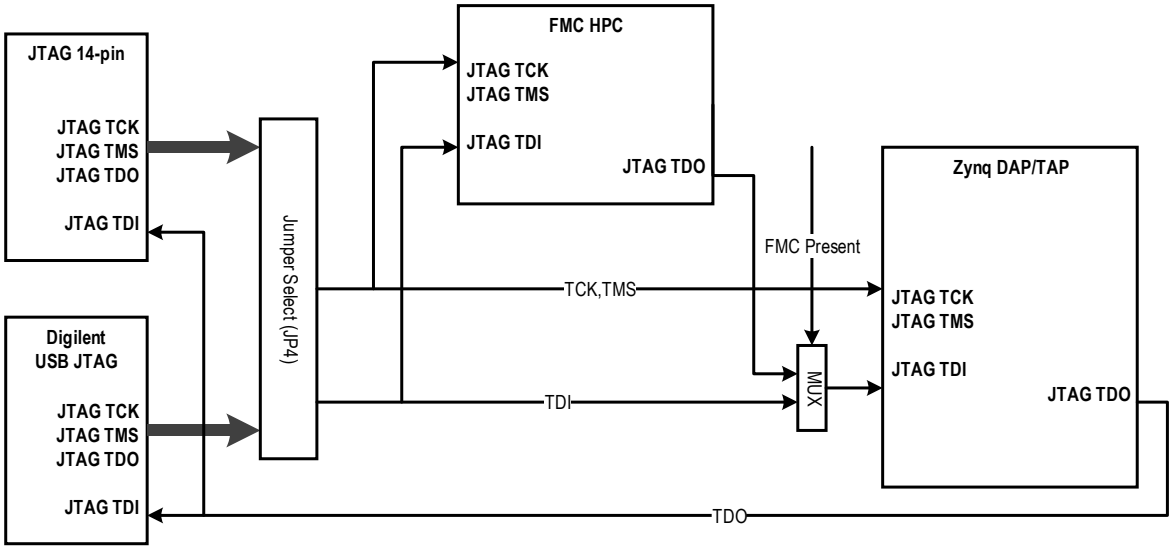

Figure 70 JTAG Chain Block Diagram

PJTAG is used for ARM debug, located at PL-Side.

Table 13 EMIO PJTAG

Bank	Net Name	Zynq Pin	Direction	Description
13	PJTAG_TCK	AA25	IN	
13	PJTAG_TMS	AB25	IN	
13	PJTAG_TDO	V19	OUT	
13	PJTAG_TDI	AB26	IN	

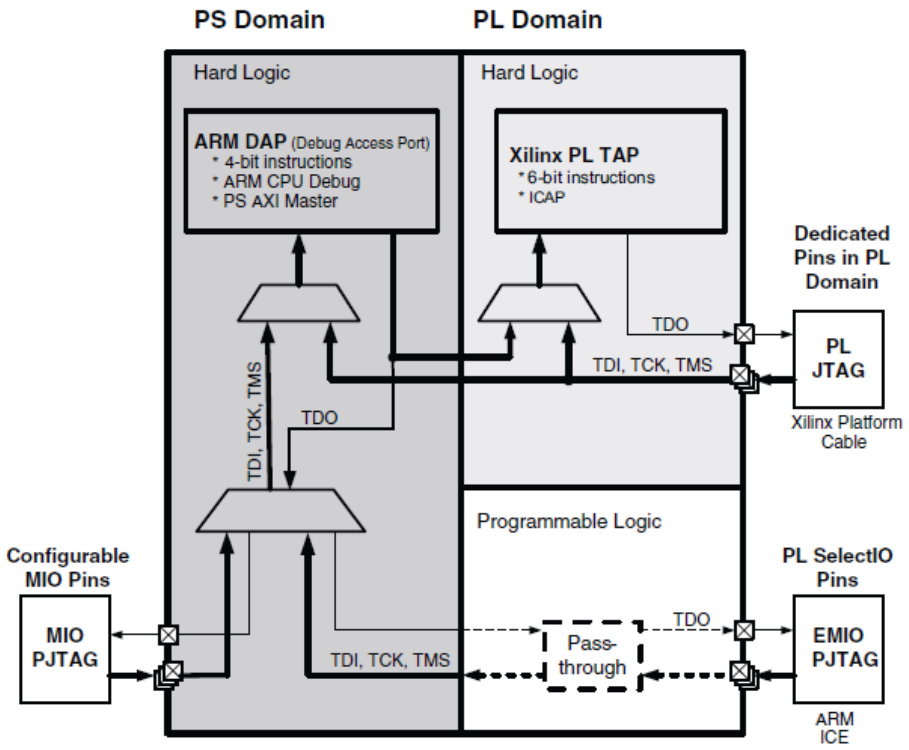

Figure 81 JTAG Debug Trace Port

Key features of the JTAG debug interface are:

- ✓ JTAG 1149.1 boundary scan support
- ✓ Two 1149.1 compliance TAP controllers:One JTAG TAP controller and one ARM DAP
- ✓ Single unique IDCODE from the xilinx TAP for each of the Zynq 7000 family of devices
- ✓ IEEE 1532 programming in-system configurable (ISC) devices support
- ✓ QSPI flash programming
- ✓ Xilinx ISE Chipscope and Vivado Hardware Manager debug support
- ✓ ARM CoreSight debug center control using ARM DAP
- ✓ Indirect PS address space access through DAP-AP port

2.10 QDRII+

The ONetSwitch45 contains a 400 MHz QDRII+ SRAM interface using a CY7C25652KV18-400BZC components (x36) with baud rate up to 57.6Gbps, in response to the demand for higher bandwidth memories at networking and telecommunications applications. The QDRII+ interface is implemented across the PL-side I/O bank 33, bank 34 and bank 35.

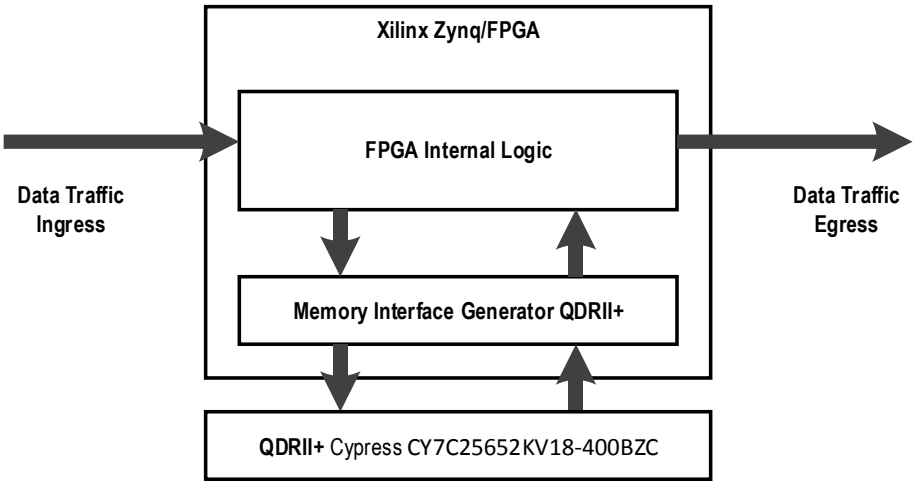

Figure 9 QDRII+ Demonstration

Table 106 QDRII+ Connections to the Bank 33

Bank	Net Name	Zynq Pin	Direction	Description
33	QDR_SA_0	H3	OUT	HSTL_I
33	QDR_SA_1	K1	OUT	HSTL_I
33	QDR_SA_2	H4	OUT	HSTL_I
33	QDR_SA_3	E2	OUT	HSTL_I
33	QDR_SA_4	G4	OUT	HSTL_I
33	QDR_SA_5	D4	OUT	HSTL_I
33	QDR_SA_6	F3	OUT	HSTL_I
33	QDR_SA_7	F2	OUT	HSTL_I
33	QDR_SA_8	H1	OUT	HSTL_I
33	QDR_SA_9	E1	OUT	HSTL_I
33	QDR_SA_10	G1	OUT	HSTL_I
33	QDR_SA_11	J1	OUT	HSTL_I
33	QDR_SA_12	H2	OUT	HSTL_I
33	QDR_SA_13	C1	OUT	HSTL_I
33	QDR_SA_14	D1	OUT	HSTL_I
33	QDR_SA_15	G2	OUT	HSTL_I
33	QDR_SA_16	K2	OUT	HSTL_I
33	QDR_SA_17	D3	OUT	HSTL_I
33	QDR_SA_18	L3	OUT	HSTL_I
33	QDR_SA_19	F4	OUT	HSTL_I
33	QDR_WPSN	K3	OUT	HSTL_I
33	QDR_RPSN	J3	OUT	HSTL_I
33	QDR_SYS_CLK_200M_P	M6	IN	DIFF_HSTL_I
33	QDR_SYS_CLK_200M_N	M5	IN	DIFF_HSTL_I

Table 117 QDRII+ Connections to the Bank 34

Bank	Net Name	Zynq Pin	Direction	Description
34	QDR_D_0	J11	IN	HSTL_I
34	QDR_D_1	H11	IN	HSTL_I
34	QDR_D_2	J8	IN	HSTL_I
34	QDR_D_3	J10	IN	HSTL_I
34	QDR_D_4	J9	IN	HSTL_I
34	QDR_D_5	H7	IN	HSTL_I
34	QDR_D_6	G5	IN	HSTL_I
34	QDR_D_7	H6	IN	HSTL_I
34	QDR_D_8	G6	IN	HSTL_I
34	QDR_D_9	F9	IN	HSTL_I
34	QDR_D_10	F8	IN	HSTL_I
34	QDR_D_11	E8	IN	HSTL_I
34	QDR_D_12	D9	IN	HSTL_I
34	QDR_D_13	D8	IN	HSTL_I
34	QDR_D_14	E7	IN	HSTL_I
34	QDR_D_15	E6	IN	HSTL_I
34	QDR_D_16	D5	IN	HSTL_I
34	QDR_D_17	G7	IN	HSTL_I
34	QDR_D_18	B6	IN	HSTL_I
34	QDR_D_19	A5	IN	HSTL_I
34	QDR_D_20	B5	IN	HSTL_I
34	QDR_D_21	A4	IN	HSTL_I
34	QDR_D_22	B4	IN	HSTL_I
34	QDR_D_23	A3	IN	HSTL_I
34	QDR_D_24	C3	IN	HSTL_I
34	QDR_D_25	C2	IN	HSTL_I
34	QDR_D_26	B1	IN	HSTL_I
34	QDR_D_27	A7	IN	HSTL_I
34	QDR_D_28	A8	IN	HSTL_I
34	QDR_D_29	B7	IN	HSTL_I
34	QDR_D_30	A9	IN	HSTL_I
34	QDR_D_31	A10	IN	HSTL_I
34	QDR_D_32	B9	IN	HSTL_I
34	QDR_D_33	B10	IN	HSTL_I
34	QDR_D_34	D6	IN	HSTL_I
34	QDR_D_35	C6	IN	HSTL_I
34	QDR_CLK_K_P	H9	OUT	DIFF_HSTL_I
34	QDR_CLK_K_N	G9	OUT	DIFF_HSTL_I
34	QDR_BWSN_0	F5	OUT	HSTL_I
34	QDR_BWSN_1	E5	OUT	HSTL_I
34	QDR_BWSN_2	C4	OUT	HSTL_I
34	QDR_BWSN_3	C9	OUT	HSTL_I
34	QDR_QVLD	B2	IN	HSTL_I

Table 18 QDRII+ Connections to the Bank 35

Bank	Net Name	Zynq Pin	Direction	Description
35	QDR_Q_0	E12	IN	HSTL_I_DCI
35	QDR_Q_1	E10	IN	HSTL_I_DCI
35	QDR_Q_2	G10	IN	HSTL_I_DCI
35	QDR_Q_3	F10	IN	HSTL_I_DCI
35	QDR_Q_4	E11	IN	HSTL_I_DCI
35	QDR_Q_5	D10	IN	HSTL_I_DCI
35	QDR_Q_6	D11	IN	HSTL_I_DCI
35	QDR_Q_7	F12	IN	HSTL_I_DCI
35	QDR_Q_8	G12	IN	HSTL_I_DCI
35	QDR_Q_9	G16	IN	HSTL_I_DCI
35	QDR_Q_10	G15	IN	HSTL_I_DCI
35	QDR_Q_11	K15	IN	HSTL_I_DCI
35	QDR_Q_12	J15	IN	HSTL_I_DCI
35	QDR_Q_13	K13	IN	HSTL_I_DCI
35	QDR_Q_14	J13	IN	HSTL_I_DCI
35	QDR_Q_15	H12	IN	HSTL_I_DCI
35	QDR_Q_16	H14	IN	HSTL_I_DCI
35	QDR_Q_17	H13	IN	HSTL_I_DCI
35	QDR_Q_18	D14	IN	HSTL_I_DCI
35	QDR_Q_19	B15	IN	HSTL_I_DCI
35	QDR_Q_20	B16	IN	HSTL_I_DCI
35	QDR_Q_21	A17	IN	HSTL_I_DCI
35	QDR_Q_22	B17	IN	HSTL_I_DCI
35	QDR_Q_23	C17	IN	HSTL_I_DCI
35	QDR_Q_24	C16	IN	HSTL_I_DCI
35	QDR_Q_25	D16	IN	HSTL_I_DCI
35	QDR_Q_26	E16	IN	HSTL_I_DCI
35	QDR_Q_27	A14	IN	HSTL_I_DCI
35	QDR_Q_28	B14	IN	HSTL_I_DCI
35	QDR_Q_29	D13	IN	HSTL_I_DCI
35	QDR_Q_30	B12	IN	HSTL_I_DCI
35	QDR_Q_31	C12	IN	HSTL_I_DCI
35	QDR_Q_32	B11	IN	HSTL_I_DCI
35	QDR_Q_33	C14	IN	HSTL_I_DCI
35	QDR_Q_34	C11	IN	HSTL_I_DCI
35	QDR_Q_35	A15	IN	HSTL_I_DCI
35	QDR_DOFFN	G11	OUT	HSTL_I
35	QDR_CLK_CQ_P	J14	IN	HSTL_I_DCI
35	QDR_CLK_CQ_N	D15	IN	HSTL_I_DCI
35	QDR_VRP	K12		
35	QDR_VRN	H16		
35	QDR_VREF_0	E13		
35	QDR_VREF_1	C13		

2.11 PL Ethernet 1G

One Broadcom BCM5464SR Ethernet transceiver (PHY) are provided to interface to network connections via a Belfuse 0826-1X4T-23-F RJ-45 connector with built-in magnetics.

The BCM5464SR transceiver consists of four triple-speed 10/100/1000BASE-T Ethernet transceivers with RGMII interfaces. The PHY could be programmed via a MDIO bus to work appropriate. For more detailed information, please refer to BCM5464SR datasheet.

- ✓ Mode setting: INTF_SEL[3:0]='0001', RGMII to Copper, 2.5V OVDD
- ✓ PHY address setting: PHYA_REV=0,PHYA[4:0]='00000', start address is '00', increase
- ✓ MDIO setting: MDIO_SEL[1:0]='00', MDIO/MDC[1] access all 4
- ✓ Speed Select: ANEN=1, F1000=1, SPD0=0, Auto-negotiate advertise: 10/100/1000BASE-T

For more detailed information about PL HDL coding, please refer to Xilinx LogiCORE IP AXI Ethernet related documents on the Xilinx website.

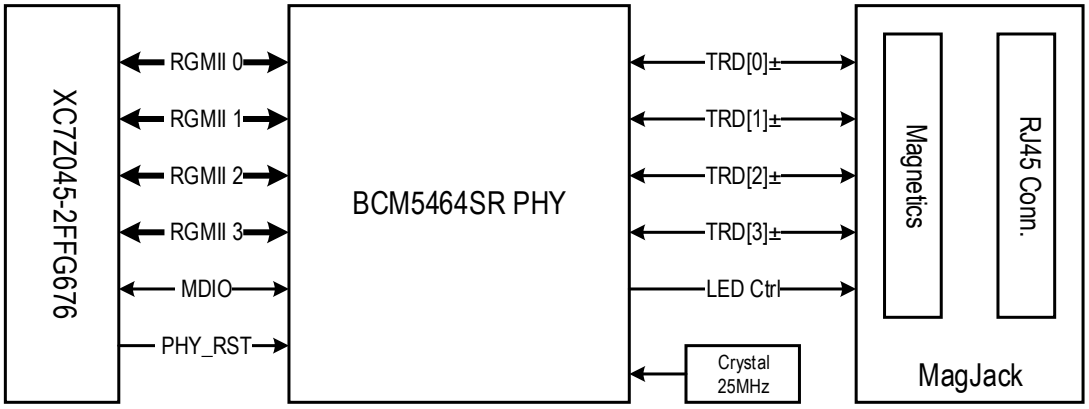

Figure 13 PL Ethernet 1G Block Diagram

The Ethernet connections from the XC7Z045 AP SoC PL to the BCM5464SR PHY device are listed in Table 19.

Table 149 PL Ethernet 1G Connections, XC7Z045 AP SoC to BCM5464SR PHY

Bank	Net Name	Zynq Pin	Direction	Description
12	PHY_0_RXC	AB15	IN	LVCMOS25
12	PHY_0_GTXCLK	Y13	OUT	LVCMOS25
12	PHY_0_TX_EN	W13	OUT	LVCMOS25
12	PHY_0_TXD_0	W15	OUT	LVCMOS25
12	PHY_0_TXD_1	Y15	OUT	LVCMOS25
12	PHY_0_TXD_2	Y17	OUT	LVCMOS25
12	PHY_0_TXD_3	AA17	OUT	LVCMOS25
12	PHY_0_RX_DV	AB16	IN	LVCMOS25
12	PHY_0_RXD_0	AB17	IN	LVCMOS25
12	PHY_0_RXD_1	AA15	IN	LVCMOS25
12	PHY_0_RXD_2	Y16	IN	LVCMOS25
12	PHY_0_RXD_3	W16	IN	LVCMOS25
12	PHY_1_RXC	AC14	IN	LVCMOS25
12	PHY_1_GTXCLK	AA14	OUT	LVCMOS25
12	PHY_1_TX_EN	AC16	OUT	LVCMOS25

12	PHY_1_TXD_0	AA13	OUT	LVCMOS25
12	PHY_1_TXD_1	AA12	OUT	LVCMOS25
12	PHY_1_TXD_2	Y12	OUT	LVCMOS25
12	PHY_1_TXD_3	AC17	OUT	LVCMOS25
12	PHY_1_RX_DV	AF17	IN	LVCMOS25
12	PHY_1_RXD_0	AD16	IN	LVCMOS25
12	PHY_1_RXD_1	AE17	IN	LVCMOS25
12	PHY_1_RXD_2	AD15	IN	LVCMOS25
12	PHY_1_RXD_3	AE16	IN	LVCMOS25
12	PHY_2_RXC	AC13	IN	LVCMOS25
12	PHY_2_GTXCLK	AB11	OUT	LVCMOS25
12	PHY_2_TX_EN	AF14	OUT	LVCMOS25
12	PHY_2_TXD_0	AF15	OUT	LVCMOS25
12	PHY_2_TXD_1	AE13	OUT	LVCMOS25
12	PHY_2_TXD_2	AD13	OUT	LVCMOS25
12	PHY_2_TXD_3	Y11	OUT	LVCMOS25
12	PHY_2_RX_DV	AD14	IN	LVCMOS25
12	PHY_2_RXD_0	AE15	IN	LVCMOS25
12	PHY_2_RXD_1	AB14	IN	LVCMOS25
12	PHY_2_RXD_2	AF13	IN	LVCMOS25
12	PHY_2_RXD_3	AB12	IN	LVCMOS25
12	PHY_3_RXC	AC12	IN	LVCMOS25
12	PHY_3_GTXCLK	AC11	OUT	LVCMOS25
12	PHY_3_TX_EN	AE12	OUT	LVCMOS25
12	PHY_3_TXD_0	AB10	OUT	LVCMOS25
12	PHY_3_TXD_1	AE10	OUT	LVCMOS25
12	PHY_3_TXD_2	Y10	OUT	LVCMOS25
12	PHY_3_TXD_3	AA10	OUT	LVCMOS25
12	PHY_3_RX_DV	AF12	IN	LVCMOS25
12	PHY_3_RXD_0	AD10	IN	LVCMOS25
12	PHY_3_RXD_1	AF10	IN	LVCMOS25
12	PHY_3_RXD_2	AD11	IN	LVCMOS25
12	PHY_3_RXD_3	AE11	IN	LVCMOS25
12	PHY_MDC0	W14	IN	LVCMOS25
12	PHY_MDIO0	W17	INOUT	LVCMOS25

2.12 PL Ethernet 10G

The ONetSwitch45 supports one x4 form-factor pluggable (SFP+) connector and cage that accept SFP or SFP+ modules. The part number of SFP+ connector is Molex 74441-001.

Four of the GTX transceivers (Bank 111) are wired to the SFP+ connector to interface to 10G BASE LAN. The SFP+ module control and status singles are connected to the PL Bank 13.

For more detailed information about PL HDL coding, please refer to Xilinx LogiCORE IP 10-Gigabit Ethernet PCS/PMA and LogiCORE IP 10-Gigabit Ethernet MAC related documents on the Xilinx website.

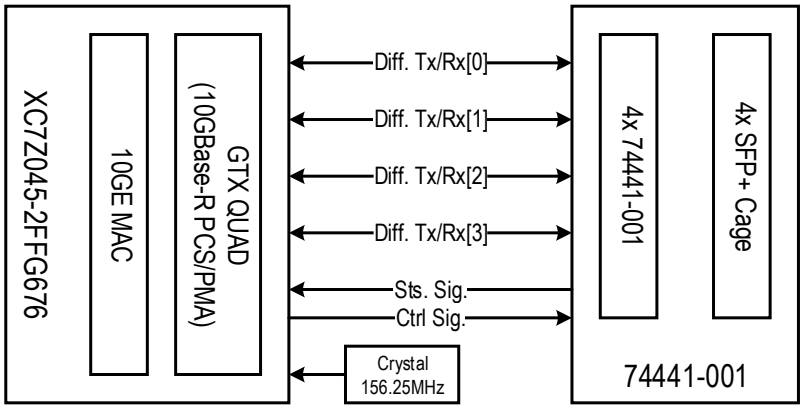

Figure 124 PL Ethernet 10G Block Diagram

Table 20 PL Ethernet 10G Connections, XC7Z045 AP SoC to x4 SFP+

Bank	Net Name	Zynq Pin	Direction	Description
13	SFP_0_LOS	AE21	IN	
13	SFP_0_TX_FAULT	AE20	IN	
13	SFT_0_MOD_DETECT	AC22	IN	MOD_ABS
13	SFP_1_LOS	AB22	IN	
13	SFP_1_TX_FAULT	AE18	IN	
13	SFT_1_MOD_DETECT	AC21	IN	MOD_ABS
13	SFP_2_LOS	AD19	IN	
13	SFP_2_TX_FAULT	AB21	IN	
13	SFT_2_MOD_DETECT	AD18	IN	MOD_ABS
13	SFP_3_LOS	AB20	IN	
13	SFP_3_TX_FAULT	W20	IN	
13	SFT_3_MOD_DETECT	AA20	IN	MOD_ABS
111	SFP_0_TX_P	AF8	OUT	MGTX-TXP#0
111	SFP_0_TX_N	AF7	OUT	MGTX-TXN#0
111	SFP_0_RX_P	AD8	IN	MGTX-RXP#0
111	SFP_0_RX_N	AD7	IN	MGTX-RXN#0
111	SFP_1_TX_P	AF4	OUT	MGTX-TXP#1
111	SFP_1_TX_N	AF3	OUT	MGTX-TXN#1
111	SFP_1_RX_P	AE6	IN	MGTX-RXP#1
111	SFP_1_RX_N	AE5	IN	MGTX-RXN#1
111	SFP_2_TX_P	AE2	OUT	MGTX-TXP#2
111	SFP_2_TX_N	AE1	OUT	MGTX-TXN#2
111	SFP_2_RX_P	AC6	IN	MGTX-RXP#2
111	SFP_2_RX_N	AC5	IN	MGTX-RXN#2
111	SFP_3_TX_P	AC2	OUT	MGTX-TXP#3
111	SFP_3_TX_N	AC1	OUT	MGTX-TXN#3
111	SFP_3_RX_P	AD4	IN	MGTX-RXP#3
111	SFP_3_RX_N	AD3	IN	MGTX-RXN#3
111	CLK_156M_SI57X_P	AA6	IN	MGTX-REFCLK#1P
111	CLK_156M_SI57X_N	AA5	IN	MGTX-REFCLK#1N

2.13 Mini PCIe

The ONetSwitch45 has a Mini PCIe Slot interface to XC7Z045 AP SoC PL-side GTX transceiver for wireless access (such as Atheros AR9380 3x3 MIMO 802.11 b/g/n WIFI module) or storage install (SSD). The XC7Z045 AP SoC integrated PCIe IP which could be set to PCIe Root Complex mode to communicate with external PCIe Endpoints.

The Mini PCIe WLAN mounted on ONetSwitch45 is shown in Figure 15. The GTX transceiver is configured to be PCIe x1 Gen2.0.

For more detailed information about PL HDL coding, please refer to Xilinx 7 Series FPGAs Integrated Block for PCI Express and LogiCORE IP AXI Bridge for PCI Express related documents on the Xilinx website.

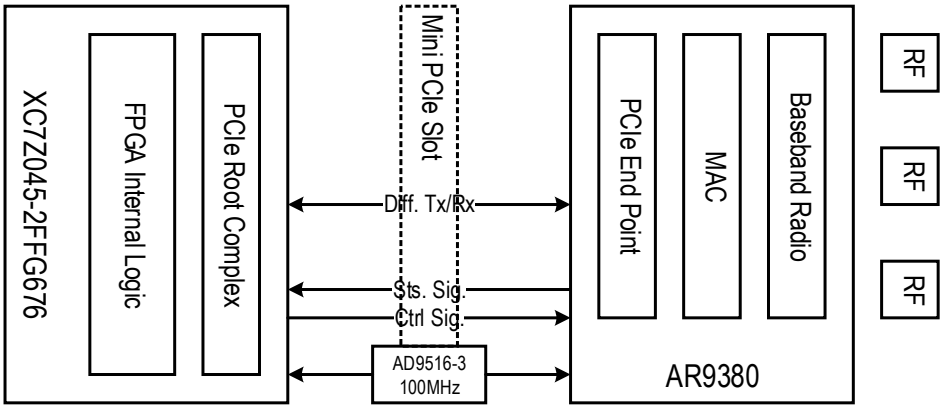

Figure 135 Mini PCIe WLAN Connections

Table 20 Mini PCIe Connections

Bank	Net Name	Zynq Pin	Direction	Description
13	PCIE_WAKE_B	AF19	IN	Req. to wake, open-drain
13	PCIE_PERST_B	AF22	OUT	Power-on Reset
13	PCIE_CLKREQ_B	AF20	IN	Req. for ref clock, open-drain
13	PCIE_W_DISABLE_B	AF18	OUT	
13	SFP_1_TX_FAULT	AE18	IN	
13	SFT_1_MOD_DETECT	AC21	IN	MOD_ABS
13	SFP_2_LOS	AD19	IN	
13	SFP_2_TX_FAULT	AB21	IN	
13	SFT_2_MOD_DETECT	AD18	IN	MOD_ABS
13	SFP_3_LOS	AB20	IN	
13	SFP_3_TX_FAULT	W20	IN	
13	SFT_3_MOD_DETECT	AA20	IN	MOD_ABS
112	GTX_PCIE_TX0_P	R2	OUT	MGTX-TXP#3
112	GTX_PCIE_TX0_N	R1	OUT	MGTX-TXN#3
112	GTX_PCIE_RX0_P	T4	IN	MGTX-RXP#3
112	GTX_PCIE_RX0_N	T3	IN	MGTX-RXN#3
112	GTX_PCIE_CLK_100M_P	R6	IN	MGTX-REFCLK#0P
112	GTX_PCIE_CLK_100M_N	R5	IN	MGTX-REFCLK#0N

2.14 FMC HPC

Figure 16 shows the pinout of the FPGA mezzanine card (FMC) high pin count (HPC) connector defined by the VITA 57.1 FMC specification. The part number of FMC connector is ASP-134486-01.

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK1_C2M_P	PRSNT_M2C_L	CLK0_C2M_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK1_C2M_N	GND	CLK0_C2M_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK1_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK1_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND
			LPC Connector	LPC Connector			LPC Connector	LPC Connector		

Figure 16 FMC LPC Connector Pinout

Table 15 FMC HPC connections

Bank	Net Name	Zynq Pin	Direction	Description
13	FMC_HA_00_A	AC18	INOUT	HA00_P_CC
13	FMC_HA_00_B	AC19	INOUT	HA00_N_CC
13	FMC_HA_01_A	AA19	INOUT	HA01_P_CC
13	FMC_HA_01_B	AB19	INOUT	HA01_N_CC
13	FMC_HA_02_A	W18	INOUT	HA02_P
13	FMC_HA_02_B	W19	INOUT	HA02_N
13	FMC_HA_03_A	Y18	INOUT	HA03_P
13	FMC_HA_03_B	AA18	INOUT	HA03_N
33	FMC_LA_0_A	L5	INOUT	LA00_P_CC
33	FMC_LA_0_B	L4	INOUT	LA00_N_CC
33	FMC_LA_1_A	N3	INOUT	LA01_P_CC
33	FMC_LA_1_B	N2	INOUT	LA01_N_CC
33	FMC_LA_2_A	M2	INOUT	LA02_P
33	FMC_LA_2_B	L2	INOUT	LA02_N

33	FMC_LA_3_A	N4	INOUT	LA03_P
33	FMC_LA_3_B	M4	INOUT	LA03_N
33	FMC_LA_4_A	N1	INOUT	LA04_P
33	FMC_LA_4_B	M1	INOUT	LA04_N
33	FMC_LA_5_A	M7	INOUT	LA05_P
33	FMC_LA_5_B	L7	INOUT	LA05_N
33	FMC_LA_6_A	K5	INOUT	LA06_P
33	FMC_LA_6_B	J5	INOUT	LA06_N
33	FMC_LA_7_A	M8	INOUT	LA07_P
33	FMC_LA_7_B	L8	INOUT	LA07_N
33	FMC_LA_8_A	K6	INOUT	LA08_P
33	FMC_LA_8_B	J6	INOUT	LA08_N
33	FMC_LA_9_A	N7	INOUT	LA09_P
33	FMC_LA_9_B	N6	INOUT	LA09_N
33	FMC_LA_10_A	K8	INOUT	LA10_P
33	FMC_LA_10_B	K7	INOUT	LA10_N
112	GTX_FMC_TX_2_P	AA2	OUT	MGTX-TXP#0 DP2_C2M_P
112	GTX_FMC_TX_2_N	AA1	OUT	MGTX-TXN#0 DP2_C2M_N
112	GTX_FMC_RX_2_P	AB4	IN	MGTX-RXP#0 DP2_M2C_P
112	GTX_FMC_RX_2_N	AB3	IN	MGTX-RXN#0 DP2_M2C_N
112	GTX_FMC_TX_1_P	W2	OUT	MGTX-TXP#1 DP1_C2M_P
112	GTX_FMC_TX_1_N	W1	OUT	MGTX-TXN#1 DP1_C2M_N
112	GTX_FMC_RX_1_P	Y4	IN	MGTX-RXP#1 DP1_M2C_P
112	GTX_FMC_RX_1_N	Y3	IN	MGTX-RXN#1 DP1_M2C_N
112	GTX_FMC_TX_0_P	U2	OUT	MGTX-TXP#2 DP0_C2M_P
112	GTX_FMC_TX_0_N	U1	OUT	MGTX-TXN#2 DP0_C2M_N
112	GTX_FMC_RX_0_P	V4	IN	MGTX-RXP#2 DP0_M2C_P
112	GTX_FMC_RX_0_N	V3	IN	MGTX-RXN#2 DP0_M2C_N
112	GTX_FMC_CLK_156M_P	U6	IN	MGTX-REFCLK#1N GBTCLK0_M2C_P
112	GTX_FMC_CLK_156M_N	U5	IN	MGTX-REFCLK#1P GBTCLK0_M2C_N

Table 162 FMC HPC pinout

FMC	Net Name	FPGA	BANK	FMC	Net Name	FPGA	BANK
C2	GTX_FMC_TX_0_P	U2	112	D1	PS_POR_B	C23	500
C3	GTX_FMC_TX_0_N	U1		D4	GTX_FMC_CLK_156M_P	U6	112
C6	GTX_FMC_RX_0_P	V4		D5	GTX_FMC_CLK_156M_N	U5	
C7	GTX_FMC_RX_0_N	V3		D8	PL_FMC_LA_1_A	N3	33
C10	PL_FMC_LA_6_A	K5	33	D9	PL_FMC_LA_1_B	N2	
C11	PL_FMC_LA_6_B	J5		D11	PL_FMC_LA_5_A	M7	
C14	PL_FMC_LA_10_A	K8		D12	PL_FMC_LA_5_B	L7	
C15	PL_FMC_LA_10_B	K7		D14	PL_FMC_LA_9_A	N7	
C30	PL_I2C_SCL_MAIN	A22	13	D15	PL_FMC_LA_9_B	N6	
C31	PL_I2C_SDA_MAIN	A23		D29	JTAG_FMC_TCK	14	U5
C34	GND	GND		D30	JTAG_FMC_TDI	18	
C35	VDD_12V	VDD_12V		D31	JTAG_FMC_TDO_FPGA_TDI	2	U26
C37	VDD_12V	VDD_12V		D32	VDD_3V3		
C39	VDD_3V3	VDD_3V3		D33	JTAG_FMC_TMS	16	U5
				D34	PS_SRST_B	10	U10
G6	PL_FMC_LA_0_A	L5	33	D35	GND		
G7	PL_FMC_LA_0_B	L4		D36	VDD_3V3		
G9	PL_FMC_LA_3_A	N4		D38	VDD_3V3		
G10	PL_FMC_LA_3_B	M4		D40	VDD_3V3		
G12	PL_FMC_LA_8_A	K6					
G13	PL_FMC_LA_8_B	J6		H2	FMC_PRSNT_M2C_B	4	U26
G30	9516_FMC_CLK_125M_P	28	U15	H7	PL_FMC_LA_2_A	M2	33
G31	9516_FMC_CLK_125M_N	29		H8	PL_FMC_LA_2_B	L2	
				H10	PL_FMC_LA_4_A	N1	
K7	PL_FMC_HA_02_A	W18	13	H11	PL_FMC_LA_4_B	M1	
K8	PL_FMC_HA_02_B	W19		H13	PL_FMC_LA_7_A	M8	
				H14	PL_FMC_LA_7_B	L8	
F4	PL_FMC_HA_00_A	AC18	13				
F5	PL_FMC_HA_00_B	AC19		A2	GTX_FMC_RX_1_P	Y4	112
				A3	GTX_FMC_RX_1_N	Y3	
E2	PL_FMC_HA_01_A	AA19	13	A6	GTX_FMC_RX_2_P	AB4	
E3	PL_FMC_HA_01_B	AB19		A7	GTX_FMC_RX_2_N	AB3	
				A22	GTX_FMC_TX_1_P	W2	
J6	PL_FMC_HA_03_A	Y18	13	A23	GTX_FMC_TX_1_N	W1	
J7	PL_FMC_HA_03_B	AA18		A26	GTX_FMC_TX_2_P	AA2	
				A27	GTX_FMC_TX_2_N	AA1	

2.15 Power Management

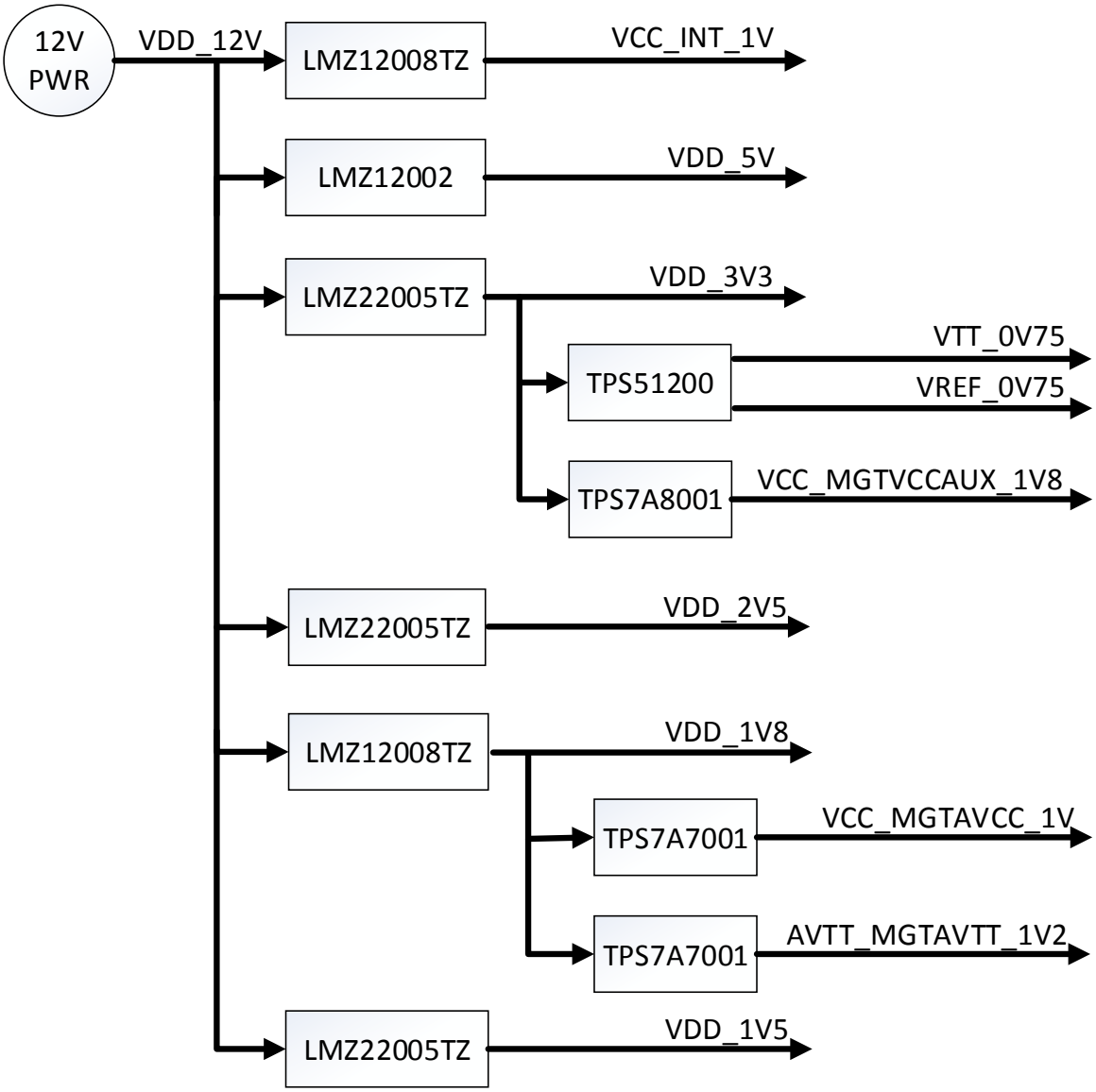

Figure 17 Onboard Power Regulators

2.16 Pushbutton, DIP Switch and LED

Table 23 User Pushbutton Connections to XC7Z045 AP SoC

#	Pushbutton Reference	Type	Zynq Pin	Description
1	SW1	System	V9	PROG_B: AP SoC program
2	SW2	System	E23	MIO_7_PHY_RST for PS Ethernet reset.
3	SW3	System	C23	POR_B: board reset
4	SW4	System	A22	SRST_B: PS reset
5	SW5	User	A13	Pull high, output '0' when press the button
6	SW6	User	A12	Pull high, output '0' when press the button

Table 24 DIP Switch Connections to XC7Z045 AP SoC

#	Switch Reference: Pin	Type	Zynq Pin	Description
1	SW9:1	User	F13	Custom
2	SW9:2	User	G14	Custom
3	SW9:3	User	F15	Custom
4	SW9:4	User	E15	Custom

Table 25 LED Connections

#	LED Reference	Type	Zynq Pin	Description
1	DS1	System	R8	INIT_B: AP SoC initiate
2	DS2	System	W9	DONE: FPGA program done
3	DS3	System		PS MIO8
4	DS4	System		Resetting
5	DS5	User	AB24	Indicate HIGH output
6	DS6	User	AA24	Indicate HIGH output
7	DS7	User	AF20	Indicate HIGH output
8	DS8	User	AE20	Indicate HIGH output
9	DS9	System	System	System
10	DS10	System	System	System
11	DS11	System	System	System
12	DS12	System	System	System

3 Board Setting

3.1 Jumper Settings

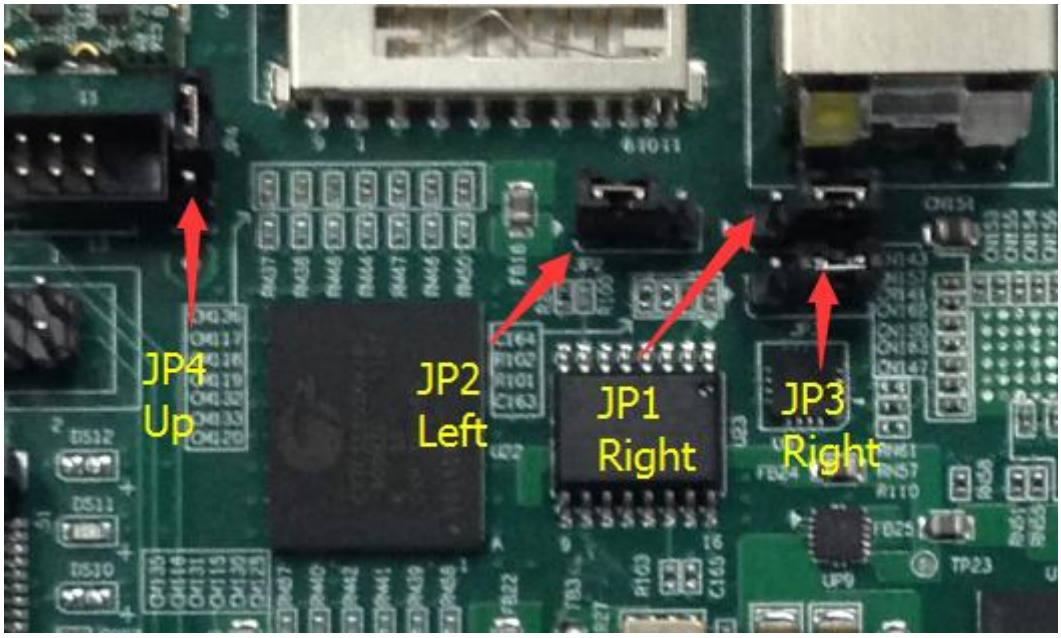

Figure 18 Default Jumper Settings (Boot Mode: SD Card)

Table 26 Jumper Setting

#	Jumper Reference	Connection	Location	Description
1	JP1	2-3	Right	JTAG Mode
2	JP2	1-2	Left	Toggle SD Card
3	JP3	2-3	Right	PLL Mode
4	JP4	1-2	Upper	Toggle USB JTAG
5	JP5	x		XADC Setting, No Connect

4 Additional Resources

- ✓ MeshSr ONetSwitch45 http://www.meshsr.com/product/onetswitch45
- ✓ Xilinx Zynq AP SoC http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm
  Xilinx FMC Std. http://www.xilinx.com/products/boards_kits/fmc.htm
- ✓ Xilinx LogiCORE IP Using Xilinx DocNav for Vivado 2013.4
  - PG138 LogiCORE IP AXI Ethernet v6.0
  - PG051 LogiCORE IP Tri-Mode Ethernet MAC v8.1
  - PG059 LogiCORE IP AXI Interconnect v2.1
  - PG164 LogiCORE IP Processor System Reset Module v5.0
  - PG082 LogiCORE IP Processing System 7 v5.3
  - PG068 LogiCORE IP 10-Gigabit Ethernet PCS/PMA v4.1
  - PG072 LogiCORE IP 10-Gigabit Ethernet MAC v13.0
  - PG054 7 Series FPGAs Integrated Block for PCI Express v3.0
  - PG021 LogiCORE IP AXI Bridge for PCI Express v2.3
  - PG132 LogiCORE IP Integrated Bit Error Ratio Tester (IBERT) for 7 Series GTX Transceivers v3.0
  - UG586 Zynq-7000 SoC and 7 Series Devices Memory Interface Solutions v2.0
- ✓ ARM AMBA
  - AXI4-Lite IHI0022E AMBA® AXI™ and ACE™ Protocol Specification
  - AXI4-Stream IHI0051A AMBA® 4 AXI4-Stream Protocol

5 Revision History

Date	Version	Description
2014-04-28	1.00	Initial MeshSr release
2014-11-20	1.10	Modified