ONetSwitch20 Hardware User Guide

1 Overview

ONetSwitch20 is an All Programmable Open Network Innovation Platform.

ONetSwitch20 adopts the Xilinx XC7Z020 Zynq AP SoC, and the Zedboard as the motherboard. And it utilizes the MeshSr FMC4GE daughter card to extend four Gigabit Ethernet interfaces. Meanwhile, ONetSwitch20 strengthens reference designs of network interfaces and network applications, and customizes the common platform for mother card to a network system node with powerful performance on network process.

1.1 Key Features

Table 1 ONetSwitch20 Key Features

General	
Core Silicon	XC7Z020-1CLG484
Power Supply	DC 12V
Programming Source	QSPI Flash / JTAG / SD Card
Processing System	
Processor	Dual ARM Cortex-A9@800MHz
Cache	L1: 32KB Instruction + 32KB Data per processor; L2: 512KB; OCM: 256KB
DRAM	DDR3 512MBytes
Flash	Quad SPI Flash 256Mb
DMA	8 channel (4 for Programmable Logic)
Ethernet Port	1x 1000BASE-T
Peripheral	USB / USB-UART / USB JTAG / SD Card
Programmable Logic	
Programmable Logic Equivalent	85K Logic Cells, Logic Cells, Artix-7FPGA, Approximate ASIC Gates 1.3M
PS to PL Interconnect	AMBA AXI4 interconnect, maximum 100Gbps
Ethernet Port	4x GE RJ45 10/100/1000M Ethernet, mounted at FMC card
Peripheral	I2S ADC / HDMI / VGA / OLED
User I/O	User LEDs/Pushbuttons/DIP Switch

1.2 Board Block Diagram

1.2.1 Board-to-Board Connection

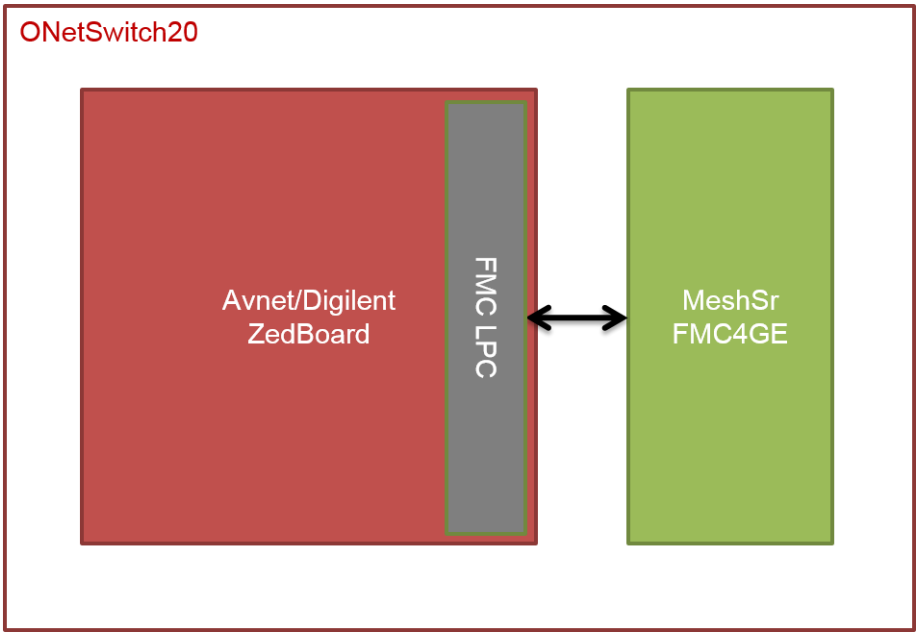

Figure 1 ONetSwitch20 Board-to-Board Block Diagram

1.2.2 ONetSwitch20 Block Diagram

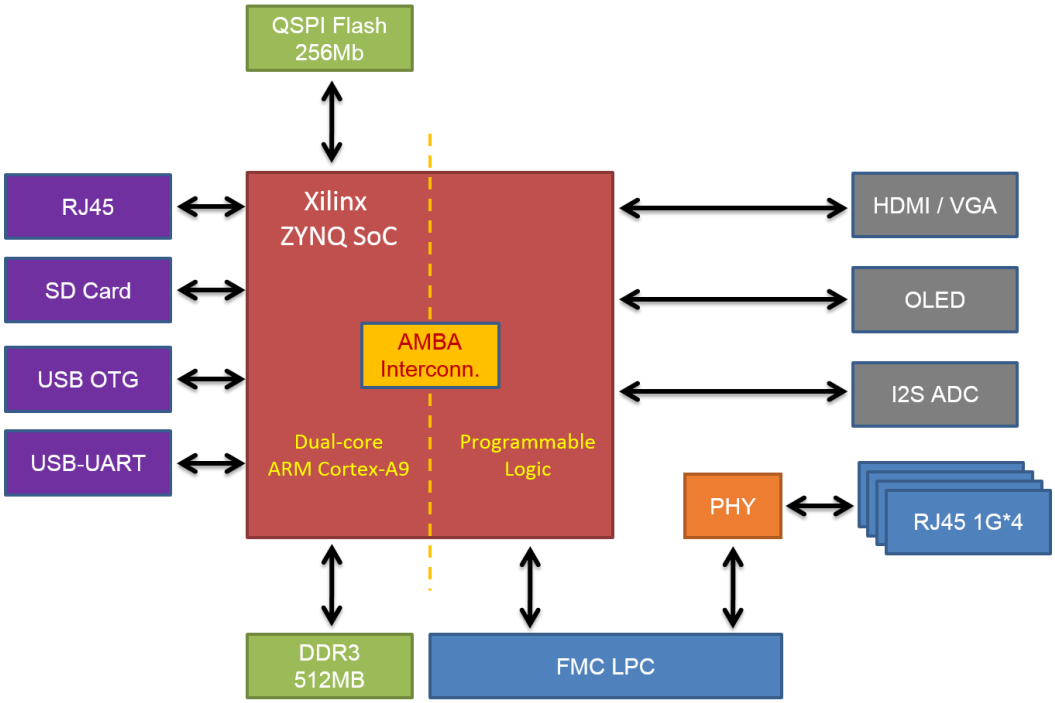

Figure 2 ONetSwitch20 Feature Block Diagram

1.3 Bank Description

1.3.1 Main Board Description

ONetSwitch20 remains the features of Zedboard except 57 pins locate at Bank34 and Bank 35, which occupied by FMC mezzanine card. Please refer to ZedBoard Hardware User Guide for more information about BANK and Pin Assignments.

Table 1 Zynq Bank Assignments

Bank	I/O Power supply	Feature
500(MIO 0)	3.3V	QSPI, PMOD
501(MIO 1)	1.8V	USB-UART, Ethernet RJ45, USB-OTG, SD
502(DDR)	1.5V	DDR3
13(High Range)	3.3V	OLED, PMODs, I2S ADC
33(High Range)	3.3V	HDMI, VGA
34(High Range)	2.5V(Adjustable)	FMC, Push button
35(High Range)	2.5V(Adjustable)	FMC, User switch

1.3.2 X4 GE Ethernet FMC

The FMC Connectivity mezzanine card is designed to provide 4 Ethernet ports which support 10/100/1000BASE-T standard PHY functions to connect XC7Z020 Zynq AP SoC on ZedBoard.

ONetSwitch20 uses the Broadcom BCM5464SR PHY (RGMII to copper) for x4 Ethernet communications. The FMC card with LPC connector interfaces the BCM5464SR to PL of Zynq AP SoC. The PHY connects to MIO Bank34 (MDIO, port #0, port #1) and Bank35 (RST, port #3, port #4).

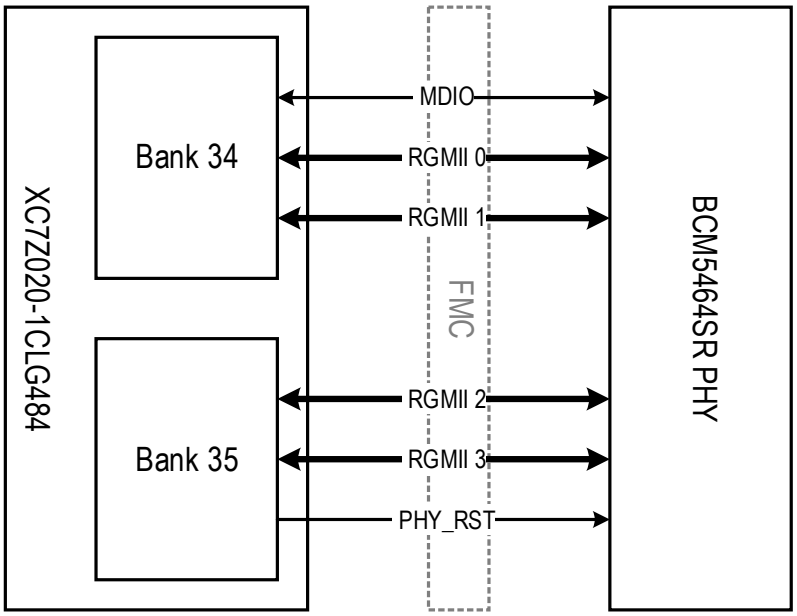

Figure 2 Quad GE PHY connections

2 Feature Descriptions

2.1 Main Board Features

The ONetSwitch20 is populated with the Xilinx Zynq XC7Z020-1CLG484 AP SoC.
The XC7Z020 AP SoC consists of an integrated processing system (PS) a programmable logic (PL), on a single die.
Information for the Main Board specification can be found at the ZedBoard Hardware User Guide.

Table 2 Main Board Features

Feature	Connection	Component part number	Detailed information from ZedBoard Hardware User Guide
DDR3	PS	MT41K128M16JT-125	Power supply, Connections,延迟
QSPI	PS	S25FL256SAGMFI00	Mode setting, Pin assignment
SD	PS	2041021-1	Connections, Pin assignment
USB-OTG	PS	TUSB1210|1981584-1	Reference Clock, Pin assignment
USB-UART	PS	CY7C64225|1981584-1	Connections, Pin assignment
USB-JTAG	PS	Digilent JTAG SMT1	Connections
Ethernet	PS	88E1518|1840750-7	Mode setting, Connections, Pin assignment
HDMI	PL	ADV7511KSTZ	Mode setting, Pin assignment 时序
VGA	PL	4-1734682-2	Pin assignment
I2S ADC	PL	ADAU1761BCPZ	Mode setting, Connections, Pin assignment
OLED	PL	UG-2832HSWEG04	Connections
Push button	PS/PL	N/A	Pin assignment
User switch	PL	N/A	Pin assignment
LED	PS/PL	N/A	Pin assignment

2.2 X4 GE Ethernet Ports

One Broadcom BCM5464SR Ethernet transceiver (PHY) are provided to interface to network connections via a Belfuse 0826-1X4T-23-F RJ-45 connector with built-in magnetics.

The BCM5464SR transceiver consists of four triple-speed 10/100/1000BASE-T Ethernet transceivers with RGMII interfaces. The PHY could be programmed via a MDIO bus to work appropriate. For more detailed information, please refer to BCM5464SR datasheet.

- ✓ Mode setting: INTF_SEL[3:0]=’0001’, RGMII to Copper, 2.5V OVDD
- ✓ PHY address setting: PHYA_REV=0,PHYA[4:0]=’00000’, start address is '00', increase
- ✓ MDIO setting: MDIO_SEL[1:0]=’00’, MDIO/MDC[1] access all 4
- ✓ Speed Select: ANEN=1, F1000=1, SPD0=0, Auto-negotiate advertise: 10/100/1000BASE-T

For more detailed information about PL HDL coding, please refer to Xilinx LogiCORE IP AXI Ethernet related documents on the Xilinx website.

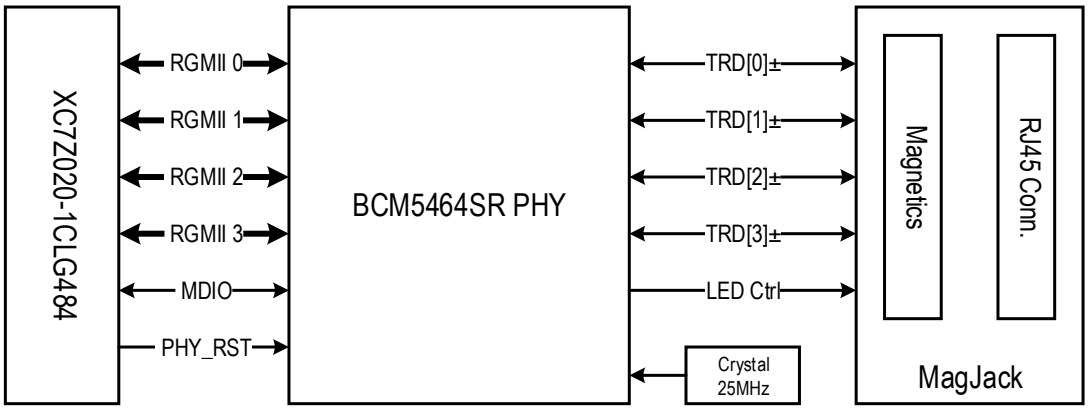

Figure 4 X4 Ethernet Block Diagram

The connections from the XC7Z020 AP SoC to BCM5464SR are listed in Table 4.

The FMC4GE card output a 125MHz reference clock to main board (L18/L19).

The trace lengths must be considered for RGMII layout. The main board trace lengths was informed at ZedBorad user guide, and the FMC card side are listed in Table 4.

Table 4 X4 GE Ethernet Connections

Grp.	Pin	BANK	LOC	FMC	Net	Etch Len. Mils
RGMII0	rgmii_0_txc	34	J17	LA15_N	PHY_0_GTXCLK	1692.747
	rgmii_0_rxc	34	M19	LA00_P_CC	PHY_0_RXC	1716.171
	rgmii_0_rd[0]	34	J18	LA05_P	PHY_0_RXD_0	1687.121
	rgmii_0_rd[1]	34	N18	LA11_N	PHY_0_RXD_1	1708.124
	rgmii_0_rd[2]	34	P21	LA12_N	PHY_0_RXD_2	1758.829
	rgmii_0_rd[3]	34	P20	LA12_P	PHY_0_RXD_3	1685.59
	rgmii_0_rx_ctl	34	K18	LA05_N	PHY_0_RX_DV	1772.593
	rgmii_0_td[0]	34	J22	LA08_N	PHY_0_TXD_0	1702.916
	rgmii_0_td[1]	34	T17	LA07_N	PHY_0_TXD_1	1697.979
	rgmii_0_td[2]	34	N17	LA11_P	PHY_0_TXD_2	1733.734
	rgmii_0_td[3]	34	L21	LA06_P	PHY_0_TXD_3	1848.894
	rgmii_0_tx_ctl	34	J16	LA15_P	PHY_0_TX_EN	1690.039
RGMII1	rgmii_1_txc	34	R21	LA09_N	PHY_1_GTXCLK	2602.528
	rgmii_1_rxc	34	N19	LA01_P_CC	PHY_1_RXC	2431.953
	rgmii_1_rd[0]	34	T16	LA07_P	PHY_1_RXD_0	2541.806
	rgmii_1_rd[1]	34	M22	LA04_N	PHY_1_RXD_1	2432.294
	rgmii_1_rd[2]	34	P17	LA02_P	PHY_1_RXD_2	2547.459
	rgmii_1_rd[3]	34	L17	LA13_P	PHY_1_RXD_3	2451.657
	rgmii_1_rx_ctl	34	R20	LA09_P	PHY_1_RX_DV	2441.992
	rgmii_1_td[0]	34	N22	LA03_P	PHY_1_TXD_0	2459.521
	rgmii_1_td[1]	34	P18	LA02_N	PHY_1_TXD_1	2450.547
	rgmii_1_td[2]	34	M20	LA00_N_CC	PHY_1_TXD_2	2448.238
	rgmii_1_td[3]	34	T19	LA10_N	PHY_1_TXD_3	2527.951
	rgmii_1_tx_ctl	34	R19	LA10_P	PHY_1_TX_EN	2432.416
RGMII2	rgmii_2_txc	35	C22	LA25_N	PHY_2_GTXCLK	2663.201

	rgmii_2_rxc	35	B19	LA17_P_CC	PHY_2_RXC	2795.669
	rgmii_2_rd[0]	35	E15	LA23_P	PHY_2_RXD_0	2729.28
	rgmii_2_rd[1]	35	C20	LA18_N_CC	PHY_2_RXD_1	2782.084
	rgmii_2_rd[2]	35	G15	LA19_P	PHY_2_RXD_2	2706.063
	rgmii_2_rd[3]	35	E21	LA27_P	PHY_2_RXD_3	2724.659
	rgmii_2_rx_ctl	35	F18	LA26_P	PHY_2_RX_DV	2672.365
	rgmii_2_td[0]	35	G21	LA20_N	PHY_2_TXD_0	2722.673
	rgmii_2_td[1]	35	A17	LA28_N	PHY_2_TXD_1	2714.414
	rgmii_2_td[2]	35	A18	LA24_P	PHY_2_TXD_2	2722.488
	rgmii_2_td[3]	35	D21	LA27_N	PHY_2_TXD_3	2687.964
	rgmii_2_tx_ctl	35	E18	LA26_N	PHY_2_TX_EN	2717.697
RGMII3	rgmii_3_txc	35	D22	LA25_P	PHY_3_GTXCLK	2650.733
	rgmii_3_rxc	35	D20	LA18_P_CC	PHY_3_RXC	2771.734
	rgmii_3_rd[0]	35	C15	LA30_P	PHY_3_RXD_0	2748.336
	rgmii_3_rd[1]	35	A16	LA28_P	PHY_3_RXD_1	2714.475
	rgmii_3_rd[2]	35	C18	LA29_N	PHY_3_RXD_2	2689.041
	rgmii_3_rd[3]	35	C17	LA29_P	PHY_3_RXD_3	2717.528
	rgmii_3_rx_ctl	35	A19	LA24_N	PHY_3_RX_DV	2768.749
	rgmii_3_td[0]	35	F19	LA22_N	PHY_3_TXD_0	2639.867
	rgmii_3_td[1]	35	E20	LA21_N	PHY_3_TXD_1	2641.387
	rgmii_3_td[2]	35	G16	LA19_N	PHY_3_TXD_2	2685.051
	rgmii_3_td[3]	35	G19	LA22_P	PHY_3_TXD_3	2633.939
	rgmii_3_tx_ctl	35	E19	LA21_P	PHY_3_TX_EN	2648.097
RST	phy_rst_n	35	B17	LA31_N	PHY_CFG_RESET_N	3522.908
MDIO	mdio_mdc	34	J21	LA08_P	PHY_MDC	1637.892
	mdio_io	34	P22	LA03_N	PHY_MDIO	1727.127
INT	phy_int[0]	34	N20	LA01_N_CC	PHY_0_INT	1995.55
	phy_int[1]	34	M21	LA04_P	PHY_1_INT	1776.663
	phy_int[2]	35	B20	LA17_N_CC	PHY_2_INT	1937.523
	phy_int[3]	35	G20	LA20_P	PHY_3_INT	2071.132
CLK	fmc_clk125m_p	34	L18	CLK0_M2C_P	CLK_LVDS_PHY_125M_P	603.848
	fmc_clk125m_n	34	L19	CLK0_M2C_N	CLK_LVDS_PHY_125M_N	603.848

3 Board Setting

3.1 Jumper Settings

For more detailed information about jumper setting, please refer to ZedBoard Hardware User Guide.

To make the 2.5V powered PHY on FMC x4 GE mezzanine card work appropriately, JP18 must be setting to 2.5V mode.

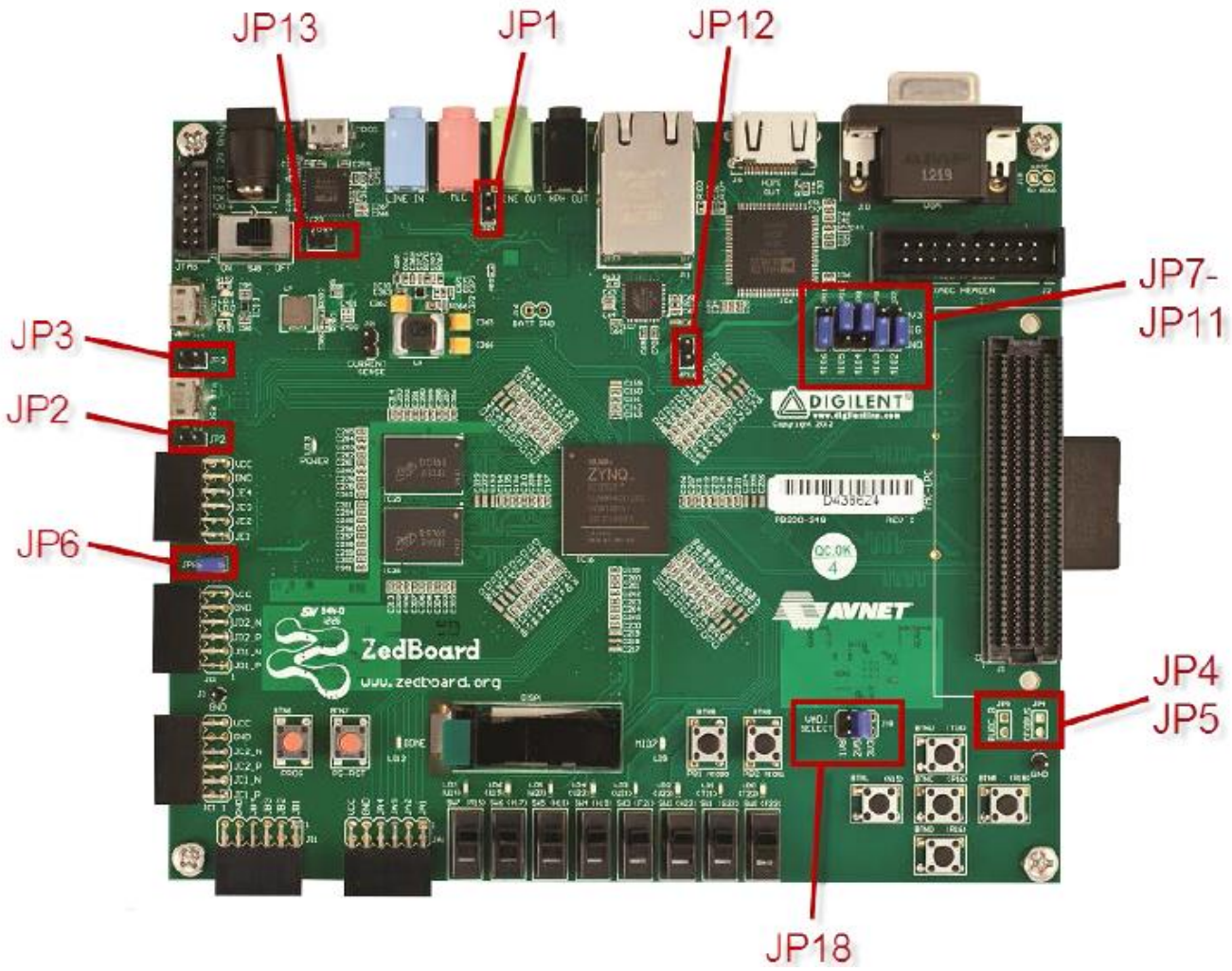

Figure 3 Main Board (ZedBoard) Jumper Locations

4 Additional Resources

- ✓ MeshSr ONetSwitch20 http://www.meshsr.com/product/onetswitch20
- ✓ Avnet/Digilent ZedBoard http://www.zedboard.org/product/zedboard
  ZedBoard Doc http://www.zedboard.org/documentation/1521
- ✓ Xilinx Zynq AP SoC http://www.xilinx.com/products/silicon-devices/soc/zynq-7000/index.htm
  Xilinx FMC Std. http://www.xilinx.com/products/boards_kits/fmc.htm

5 Revision History

Date	Version	Description
2014-04-04	1.00	Initial MeshSr release
2014-12-01	1.01	Modified