Changchun Zhou

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EDUCATION

Peking University - Beijing, China 9/2018 –12/2023 (Expected)

Doctor of Philosophy in Microelectronics and Solid-State Electronics

- Thesis Title: Research on On-Chip Neural Network Accelerators for 3D Understanding
- GPA: 3.6/4.0, 1/157 in Comprehensive Ranking
- Supervisor: Prof. Hailong Jiao

Sun Yat-sen University - Guangzhou, China 9/2014 –6/2018

Bachelor of Engineering in Microelectronics Science and Engineering

- GPA: 3.8/5.0
- Supervisor: Prof. Tao Su

RESEARCH INTERESTS

- Energy-Efficient AI Accelerator for Edge Computing
- Algorithm-Hardware Co-Design

PUBLICATION

- **C. Zhou**, M. Liu, S. Qiu, X. Cao, Y. Fu, Y. He, and H. Jiao, "Sagitta: An Energy-Efficient Sparse 3D-CNN Accelerator for Real-Time 3D Understanding," *IEEE Internet of Things Journal (**JIOT**)*, 2023, DOI: 10.1109/JIOT.2023.3306435. (IF=10.6, JCR Q1)
- **C. Zhou**, M. Liu, S. Qiu, Y. He, and H. Jiao, "An Energy-Efficient Low-Latency 3D-CNN Accelerator Leveraging Temporal Locality, Full Zero-Skipping, and Hierarchical Load Balance," in *Proc. of the IEEE/ACM Design Automation Conference (**DAC**)*, pp. 241-246, December 2021.
- **C. Zhou**, Y. Fu, M. Liu, S. Qiu, G. Li, Y. He, and H. Jiao, "An Energy-Efficient 3D Point Cloud Neural Network Accelerator with Efficient Filter Pruning, MLP Fusion, and Dual-Stream Sampling," in *Proc. of the IEEE/ACM International Conference On Computer Aided Design (**ICCAD**)*, 2023, Accepted.
- **C. Zhou***, Y. Fu*, Y. Ma, E. Han, Y. He, and H. Jiao, "Adjustable Multi-Stream Block-Wise Farthest Point Sampling Acceleration in Point Cloud Analysis," *IEEE Transactions on Circuits and Systems II: Express Briefs (**TCAS-II**)*, 2023, Under Review. (IF=4.4)
- M. Liu, **C. Zhou**, S. Qiu, Y. He, and H. Jiao, "CNN Accelerator at the Edge with Adaptive Zero Skipping and Sparsity-Driven Data Flow," *IEEE Transactions on Circuits and Systems for Video Technology(**TCSVT**)*, 2023, DOI: 10.1109/TCSVT.2023.3274964. (IF=8.4, JCR Q1)
- Y. Fu, **C. Zhou**, T. Huang, E. Han, Y. He, and H. Jiao, "SoftAct: A High-Precision Softmax Architecture for Transformers Supporting Nonlinear Functions," *IEEE Transactions on Circuits and Systems I: Regular Papers (**TCAS-I**)*, 2023, Under Review. (IF=5.1, JCR Q1)

TAPE OUT

- An energy-efficient pipelined and configurable 3D point cloud-based neural network accelerator was fabricated in TSMC 28-nm HPC technology with an area of 2.0 mm×1.5 mm (Project Leader, 8/2023)
- A 4.5 TOPS/W sparse 3D-CNN accelerator for real-time 3D understanding was fabricated in UMC 55-nm low-power CMOS technology with an area of 4.2 mm×3.6 mm (Project Leader, 8/2020)
- A 2.4 TOPS/W CNN accelerator with adaptive zero skipping and sparsity-driven dataflow was fabricated in TSMC 28-nm HPC technology with an area of 2.0 mm×1.35 mm (Module Leader, 6/2022)
- A 2.0 TOPS/W CNN accelerator skipping invalid activations was fabricated in UMC 55-nm low-power CMOS technology with an area of 3.4 mm×2.3 mm (Module Leader, 10/2019)

SKILLS

- Flows: IC Front-End, Logic Synthesis, FPGA, Neural Network Training
- Tools: Cadence, Vivado, PyTorch, TensorFlow;
- Languages: Verilog, SystemVerilog, Python, C, Shell, Makefile
- I am an easy going and self-motivated person. Personal website: https://zhouchch3.github.io

PROJECT EXPERIENCE

Nebula: An Energy-Efficient 3D Point Cloud-Based Neural Network Accelerator **(Tapeout)**

Project Leader & Main Contributor 2/2022 – Present

- A spatially-aware block-wise sampling, improving accuracy by 7.5% and reducing computations by 30.1×
- A coarse-to-fine-grained data reuse scheme, leveraging spatio-temporal locality, delayed-aggregation, and MLP fusion to increase the on-chip data reuse by 30.1×
- A hybrid 24.8× operation skipping method, combining sampling-enabled skipping with efficient pruning
- Fabricated in TSMC 28 nm with 2.0 mm×1.5 mm. Achieved energy efficiency (8-bit) exceeding 50 TOPS/W

Sagitta: An Energy-Efficient Sparse 3D-CNN Accelerator for Real-Time 3D Understanding **(Tapeout)**

Project Leader & Main Contributor 12/2019 –12/2022

- A small differential value dropout method, leveraging locality to reduce non-zero activations by 12.5×
- A full zero skipping microarchitecture to skip both zero-activations and zero-weights for a speedup of 10.5×
- A hierarchical load-balancing scheme to increase hardware utilization and energy efficiency by 2.2×
- Fabricated in UMC 55 nm with 4.2 mm×3.6 mm. Achieved energy efficiency of 4.5 TOPS/W for 3D U-Net

Libra: A 2.4 TOPS/W CNN Accelerator with Adaptive Zero Skipping and Sparsity-Driven Data Flow **(Tapeout)**

Module Leader 9/2020 –6/2022

- Co-optimized the hardware architecture and co-tapeout the accelerator
- Designed an efficient storage management module to filter out non-zero channels for PE array

SSCNN: A 2.02 TOPS/W Sparse CNN Accelerator Skipping Invalid Activations **(Tapeout)**

Module Leader 12/2018 –8/2020

- Designed a high-bandwidth asynchronous interface module for efficient off-chip storage access
- Logic synthesis for area and power optimization, and timing analysis for timing violation check

PROFESSIONAL SERVICES

Engaged as a reviewer for more than 10 esteemed journals and conferences, which encompassed notable platforms such as IEEE Transactions on Circuits and Systems II (TCAS-II), IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), IEEE International System-on-Chip Conference (SOCC)

PATENTS

- H. Jiao, M. Liu, and **C. Zhou**, "A Convolution Operation Device Based on Systolic Array", CN Patent, ZL 202010447090.4, May 5, 2020.

HONORS & AWARDS

- Leo KoGuan Scholarship (1/157), *Peking University* 10/2023
- Exceptional Award for Academic Innovation, *Peking University* 10/2023
- Merit Student, *Peking University* 10/2023
- Award for Scientific Research, *Peking University* 12/2022
- Best Presentation Award, *IEEE CASS Shanghai and Shenzhen Joint Workshop* 5/2021
- Merit Student, *Peking University* 10/2019
- National Inspirational Scholarship, *Sun Yat-sen University* 10/2016
- First Prize in the National College Students Metallography Skills Competition, *Sun Yat-sen University* 5/2016
- National Inspirational Scholarship, *Sun Yat-sen University* 10/2015
- First Class Scholarship, *Sun Yat-sen University* 10/2015